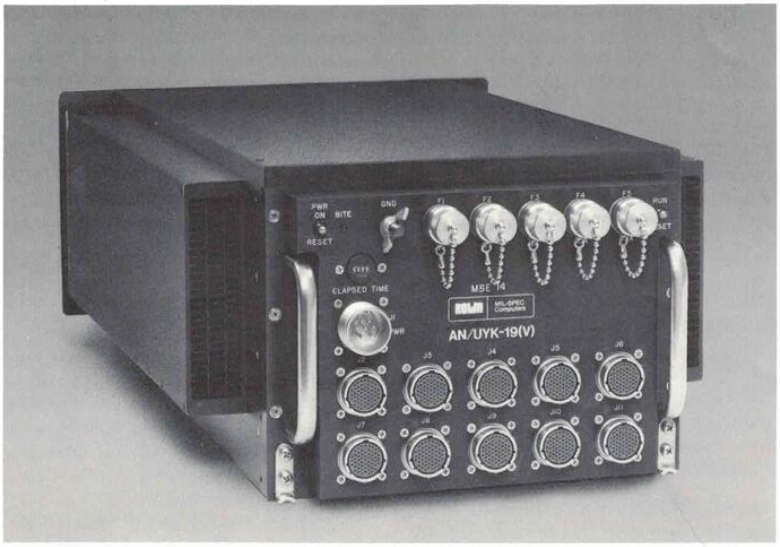
PRODUCT BRIEF

ROLM MIL-SPEC Computer Systems

MSE/14 MIL-SPEC ECLIPSE COMPUTER AN/UYK-19(V)



FEATURES

- A new member of the AN/UYK-19(V) computer family
- Full Mil-Spec version of the Data General S/140 ECLIPSE® processor with software identicality
- Compatibility with ROLM® Mil-Spec ECLIPSE/25 16-bit processor and Mil-Spec ECLIPSE/800 32-bit processor
- Designed to meet MIL-E-5400, MIL-E-16400, and MIL-E-4158 standards
- Flexible Memory System — core or semiconductor memory versions supported:

  Core
  - Basic module is 64k bytes
  - Expandable to 2048k bytes
  - Provides word parity checking

  Semiconductor
  - Basic module is 128k bytes
  - Expandable to 512k bytes
  - Provides Error Checking and Correction (ERCC) battery backup (optional)
- Single ATR chassis containing complete processing system:
  - Central Processing Unit
  - Floating-Point Unit
  - 128k-byte core or 512k-byte semiconductor memory
  - 8 I/O slots
- Semiconductor version has 2-way or 4-way interleaved memory and 400-nanosecond cycle time
- Standard Memory Management and Protection (MAP)
- Choice of two optional floating-point execution capabilities:
  - Firmware Floating-Point Instruction Set (FIS)
  - High-speed hardware Floating-Point Unit (FPU)
- Standard Character Instruction Set
- Standard Virtual Programmer's Console interface
- Standard Real-Time Clock (RTC)
- Bootstrap Load capability
- Extensive Built-In-Test (BITE):
  - Executed at power-up or callable from user program
  - Checks out CPU, FPU, and memory system
  - Isolates faults to board level
  - Failed module identified by CPU and LED display
- Hardware stack with variable frames
- Powerful hardware priority interrupt servicing
- Advanced ATR packaging:
  - Captive fasteners
  - Single-sided access
  - Plug-in power supply
- Complete software support:
  - AOS: Advanced Operating System—An operating system for software development and large system applications
  - ARTS: Advanced Real-Time System—An operating system designed exclusively for real-time applications
  - IDMS: Integrated Diagnostic Management System—An operating system designed to effectively execute diagnostic software

The ROLM MSE/14 is a new member of the AN/UYK-19(V) general-purpose military computer family providing unmatched price/performance. The MSE/14 is software identical to the Data General S/140 ECLIPSE processor, which provides for a broad selection of software to support the system. It is designed to meet MIL-E-5400 (airborne), MIL-E-16400 (shipboard), and MIL-E-4158 (land) specifications.

The MSE/14 computer offers large processor performance and system capability in a compact, severe-environment ATR package. It uses the

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powerful, proven Data General ECLIPSE instruction set, which is also compatible with the ROLM MSE/25 and MSE/800. For increased capability, it offers the Character Instruction Set as a standard feature and a choice of two optional floating-point implementations. The basic processor includes a Memory Allocation and Protection Unit (MAP) that supports up to 2048k bytes of memory. The MSE/14 is enhanced by two memory busses (Data-In and Data-Out) and a unique memory prefetch processor that maximizes memory bus utilization.

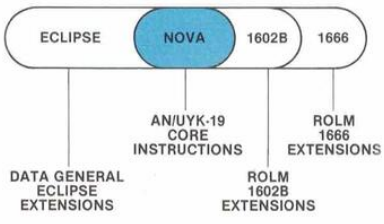
The processor can be configured with either core memory with word parity or semiconductor memory with Error Checking and Correction (ERCC). The basic core module contains 64k bytes, and two of these modules can reside within the processor chassis for a total of 128k bytes of internal memory. The core memory capacity can be expanded externally to 2048k bytes. The basic semiconductor module contains 128k bytes, and four of these modules can reside within the processor chassis for a total of 512k bytes of main memory. The semiconductor memory modules can be two-way or four-way interleaved, which dramatically reduces the effective cycle time.

DESCRIPTION

Standard Instruction Set

As all ROLM AN/UYK-19(V) processors, the MSE/14 executes the core Data General NOVA® instruction set. The complete MSE/14 Instruction Set, which is identical to Data General's ECLIPSE instruction set, (see Table 1) includes the industry's most comprehensive set of operations, data types, and addressing modes.

AN/UYK-19(V) FAMILY INSTRUCTION SET ARCHITECTURE



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TMDG/L is a trademark of Data General Corporation.

The MSE/14 is also upward compatible with ROLM's MSE/25 16-bit processor and its MSE/800 32-bit processor. This compatibility provides full family support for a wide range of applications.

Sixteen-bit single-word instructions are available for efficient memory use, and 32-bit double-word instructions are available for extended addressing range. The instruction set optimizes operating system and high-level language performance by using single-word instructions to replace software subroutines. For instance, a single BLOCK MOVE instruction transfers large data blocks between memory locations. Other instructions perform fixed-point arithmetic; word, byte, and bit manipulation; signed and unsigned multiply/divide; logical operations; and single- and double-word binary and hexadecimal shifts. Absolute, relative, indexed, immediate, and indirect addressing are available in both the 16-bit and 32-bit instructions.

Reliability and Maintainability

The MSE/14 is implemented on only four boards, dramatically reducing the number of board interconnections, which results in enhanced reliability. Very Large Scale Integrated (VLSI) circuits are used to minimize chip count, which again results in improved reliability.

The MSE/14 Error Checking and Correction feature on the semiconductor version corrects all single-bit memory errors, and detects most multiple-bit errors. ERCC constructs a 5-bit check field each time a 16-bit data word is written, and recomputes the check field when the word is read. If the check bits match, data goes to the processor. If check bits do not match, the erroneous bit is corrected, and the corrected word is transmitted to the processor. If a multiple-bit failure is detected, an interrupt is generated so that the error condition can be processed.

The MSE/14 parity feature on the core version detects single-bit errors. The parity circuitry generates an odd parity bit each time a 16-bit data word is written and regenerates the parity bit when the word is read. If the parity bits are different, an interrupt is generated so that the error condition can be processed.

A virtual programmer's console further enhances reliability by eliminating almost all mechanical switches. At power-up time, the Built-In-Test (BITE) diagnostic program is executed to test the central processor, memory, I/O bus, and prefetch processor. Results of the BITE diagnostic are shown by a LED status indicator on the front of the processor chassis. Faults can be isolated to the module level by examining the CPU accumulator with the virtual console or by visually examining LED indicators on one of the CPU boards. The BITE diagnostics are also callable from a user routine, which is very useful for running periodic system integrity checks. Also supplied is the Integrated Diagnostic Management System (IDMS), which is a diagnostic operating system. It uses the virtual console and provides more extensive diagnostics for the CPU, memory, I/O interfaces, and peripherals. During power outages, the optional Battery Backup Unit (BBU) maintains semiconductor memory contents. It can support 256k bytes of memory for approximately 60 minutes. In addition, to simplify maintenance, all boards can be accessed from the top of the processor chassis.

Advanced Microprogrammed Implementation

The MSE/14 is implemented with an extremely powerful control processor driven by a 64-bit control word with multiple independent control fields. By achieving a high degree of functional parallelism in each 200-nanosecond microcycle, the MSE/14 utilizes the flexibility and economy of microprogrammed implementation. A separate prefetch processor is implemented with a 13-instruction stack. This instruction prefetch capability allows instruction fetch cycles to overlap with instruction execution cycles, which effectively accelerates MSE/14 throughput.

Floating-Point Capabilities

The MSE/14 offers the optional choice of either a firmware Floating-Point Instruction Set (FIS) or a hardware Floating-Point Unit (FPU). Both support single- and double-precision floating-point arithmetic with 7- and 16-decimal-digit accuracy. Both use a 56-instruction ECLIPSE floating-point repertoire. Both use a 32-bit Status Register to monitor floating-point operations and identify errors to a fault handler. They also add a guard digit to all arithmetic operations for additional accuracy. Data General's Extended BASIC, FORTRAN 5, FORTRAN 77, PL/I, DG/L™, and CMS-2M system programming languages support the FPU and FIS.

TABLE 1 - MSE/14 INSTRUCTION SET

Fixed Point Arithmetic Instructions	
Add	ADD
Add Immediate	ADI
Add Word Immediate	ADDI
Compare Limits	CLM
Complement	COD
Decimal Add	DAD
Decrement and Skip if Zero	DSZ
Decimal Subtract	DSB
Exchange Accumulators	XCH
Extended Decrement and Skip if Zero	EDSZ
Extended Increment and Skip if Zero	EISZ
Extended Load Accumulator	ELDA
Extended Store Accumulator	ESTA
Halve	HLV
Increment	INC
Increment and Skip if Zero	ISZ
Load Accumulator	LDA
Move	MOV
Negate	NEG
Sign Extend and Divide	DIVX
Signed Divide	DIVS
Signed Multiply	MULS
Skip if ACS > ACD	SGT
Skip if ACS ⩾ ACD	SGE
Skip if Bit Nonzero	SNB
Store Accumulator	STA
Subtract	SUB
Subtract Immediate	SBI
Unsigned Divide	DIV
Unsigned Multiply	MUL

Logical Instructions	
Add Complement	ADC
AND	AND
And Immediate	ANDI
AND with Complemented Source	ANC
Exclusive OR	XOR
Exclusive OR Immediate	XORI
Inclusive OR	IOR
Inclusive OR Immediate	ORI

Shift Instructions	
Double Hex Shift Left	DHXL
Double Hex Shift Right	DHSR
Double Logical Shift	DLSH
Hex Shift Left	HXL
Hex Shift Right	HXR
Logical Shift	LSH

Bit Manipulation Instructions	
Count Bits	COB
Locate and Reset Lead Bit	LRB
Locate Lead Bit	LOB
Set Bit to One	BTO
Set Bit to Zero	BTZ
Skip on Zero Bit	SZB
Skip on Zero Bit and Set to One	SZBO

BYTE Instructions	
Load Byte	LDB
Store Byte	STB
Extended Load Byte	ELDB
Extended Store Byte	ESTR

Data Movement Instructions	
Block Add and Move	BAM
Block Move	FLM

Stack Instructions	
Modify Stack Pointer	MSP
Pop Block	POPB
Pop Multiple Accumulators	POP
Pop PC and Jump	POPJ
Push and Jump	PSHJ
Push and Multiple Accumulators	PSH
Push Return Address	PSHR
Restore	RSTR
Return	RTN
Save	SAVE

Special Instructions	
Dispatch Absolute	DSPA
Alternate Extended Operation	XOP1
Execute	XCT
Extended Jump	EJMP
Extended Jump to Subroutine	EJSR
Extended Load Effective Address	ELEF
Extended Operation	XOP
Jump	JMP
Jump to Subroutine	JSR
Load Effective Address	LEF
Load MAP	LMP
System Call	SCL

I/O Instructions	
Data in A	DIA
Data in B	DIB
Data in C	DIC
Data Out A	DOA
Data Out B	DOB
Data Out C	DOC
I/O Skip	SKP
No I/O Transfer	NIO

CPU Instructions	
Halt	HALT
Interrupt Acknowledge	INTA
Interrupt Disable	INTDS
Interrupt Enable	INTEN
I/O Reset	IORST
Mask Out	MSKO
Read Switches	READS
Vector	VCT

Floating-Point Instructions (Optional)	
Absolute Value	FAB
Add Double (FPAC)	FAD
Add Double (Memory)	FAMD
Add Single (FPAC)	FAS
Add Single (Memory)	FAMS
Clear Errors	FCLE
Compare Floating Point	FCMP
Divide Double (FPAC)	FDD
Divide Double (Memory)	FDMD
Divide Single (FPAC)	FDS
Divide Single (Memory)	FDMS
Fix to AC	FFAS
Fix to Memory	FFMD
Float from AC	FLAS
Float from Memory	FLMD
Halve	FHLV
Integerize	FINT
Load Double	FLDD
Load Exponent	FEXP
Load Single	FLDS
Load Status	FLST
Move Floating Point	FMOV
Multiply Double (FPAC)	FMD
Multiply Double (Memory)	FMMD
Multiply Single (FPAC)	FMS
Multiply Single (Memory)	FMMS
Negate	FNEG
No Skip	FNS
Pop Floating-Point State	FPOP
Push Floating-Point State	FPSH
Read High Word	FRH
Scale	FSCAL
Skip Always	FSA
Skip = 0	FSEQ
Skip ⩾ 0	FSGE
Skip ⩾ 0	FSGT
Skip ⩽ 0	FSLE
Skip ⩽ 0	FSLT
Skip ≠ 0	FSNE
Skip On No Zero Divide (DVZ)	FSND
Skip On No error	FSNER
Skip On No Mantissa Overflow	FSNM
Skip On No Overflow (OVF)	FSNO
Skip On No OVF and No DVZ	FSNOD
Skip On No Underflow (UNF)	FSNU
Skip On No UNF and No DVZ	FSNUD
Skip On No UNF and No OVF	FSNUO
Store Double	FSTD
Store Single	FSTS
Store Status	FSST
Subtract Double (FPAC)	FSD
Subtract Double (Memory)	FSMD
Subtract Single (FPAC)	FSS
Subtract Single (Memory)	FSMS
Trap Disable	FTD
Trap Enable	FTE

Character Instructions	
Character Move	CMV
Character Compare	CMP
Character Translate	CTR
Character Move Until True	CMT

The MSE/14 hardware Floating-Point Unit provides high-speed parallel operation with the central processor. It executes a 64-bit double-precision floating-point ADD in just 2.0 microseconds and a double-precision floating multiply in only 5.0 microseconds. The Floating-Point Unit is contained on three printed circuit boards and contains its own Built-In-Test (BITE) capability, which identifies faults to the board level. Faults are reported directly to the processor for communication to the user.

Memory Allocation and Protection

The MSE/14 Memory Allocation and Protection (MAP) capability permits memory expansion to 2048k bytes and facilitates multiuser hardware protection within the operating system. Memory pages are allocated in 2k-byte increments that are small enough for efficient memory use and large enough to eliminate heavy memory management overhead. Each 2k-byte increment is relocated to create a logically contiguous user space, eliminating fragmentation in dynamic multiuser environments. A single "LOAD MAP" instruction reestablishes a user's entire program for fast context switches.

Write protection and address validity protection prevent programs from interfering with one another. Input/output protection prevents the execution of unauthorized I/O instructions from user programs.

Extended Hardware Stack

The MSE/14's extended hardware stack is a last-in, first-out stack made up of a series of variable-length frames that can be randomly addressed. A SAVE instruction saves the machine state during subroutine linkage and allocates a stack frame. A RETURN instruction reverses the procedure. PUSH and POP instructions save and restore single or multiple registers. Stack protection features automatically detect stack overflow and underflow.

Virtual Programmer's Console

To facilitate system management and programming, a virtual programmer's console has replaced the front panel lights and switches previously used to modify and examine registers and memory. The virtual programmer's console can be either a hardcopy or CRT terminal.

When the system is in virtual console mode, normal console functions such as breakpointing, examining and depositing of accumulators and memory, and program loading can be performed from the MSE/14 console device.

This virtual console function is achieved through PROM-resident software that exists within the CPU and communicates with the user console through the standard CPU built-in asynchronous interface. The program is transparent to the user, which means that it does not occupy any memory address space.

Input/Output Capabilities

The MSE/14 system permits optimization of data transfer characteristics for each peripheral-device class. High-performance storage devices, such as fixed-head disk and moving-head disk storage systems, have transfer rates in the megabyte-per-second range. These devices, plus medium-to-high-performance devices such as floppy disks, magnetic tape subsystems, and high-speed printers, are attached to the MSE/14 data channel, which features throughput up to 1.7 megabytes per second.

Character-oriented, interrupt-per-transfer devices, such as low-speed terminals and printers, are handled through programmed I/O facilities.

Asynchronous and synchronous communications multiplexers attach directly to the programmed I/O facilities in low-line-count, low-baud-rate configurations. For larger configurations operating at medium-to-high-baud rates, these units are attached via a ROLM Model 1626 IOP (I/O Processor). The IOP is a front-end processor that off loads interrupt processing and certain line protocol and error control functions from the MSE/14 to substantially increase system throughput.

Advanced Packaging

The ROLM MSE/14 chassis includes a standard heat exchanger to ensure efficient chassis cooling. Unique features of ROLM's MSE/14 Processor chassis include the special packaging that makes logistic support easier, faster, and more economical. Access for servicing is facilitated by captive attaching screws in the power supply, connector panel, and top cover. Wedges that clamp the circuit modules to provide a heat-conducting path are accessed from the top rather than from the sides of the chassis. This permits complete single-sided module access when the top cover is removed.

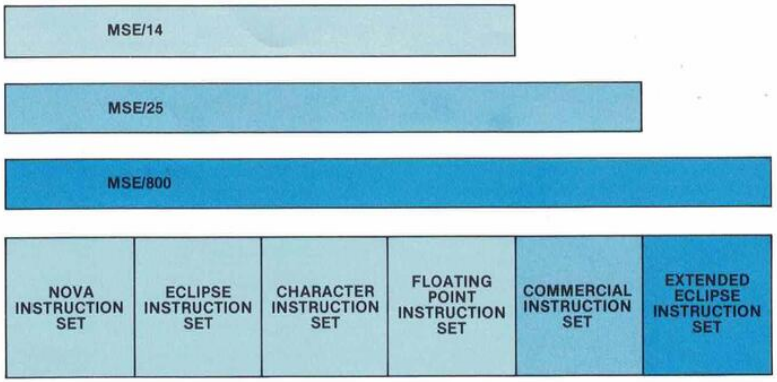
The ac power supply is a plug-in-unit. Replacing the primary power supply requires only that the plug-in power supply be removed and another one slipped into place. Converting the primary power source from ac to dc, or vice versa, requires only that the plug-in power supply and its companion power line filter be replaced. Separate connector pins are used for ac and dc to ensure an open circuit in the event primary power is not compatible with the installed power supply.

PRODUCT EXTENSIONS AND OPTIONS

Standardized I/O Wiring

The I/O slots in the MSE/14 Processor chassis can be optionally wired to provide I/O slot position independence. This means that interfaces can be moved from slot to slot and added without any wiring changes or

ROLM MSE FAMILY INSTRUCTION SETS



additions. This capability has several benefits, such as easy addition of interfaces in the field; easy addition of user designed interfaces; and easier maintenance during trouble-shooting since interfaces can easily be reconfigured. Although there are some interfaces that do not conform to this wiring scheme, most systems can be configured to meet the standardized wiring requirements.

Peripherals, Controllers, and Communications

The MSE/14 is compatible with the entire ROLM Line of Mil-Spec and commercial peripherals and controllers, including these Mil-Spec devices:

- Model 4050 35M-Byte Fixed-Media Disk
- Model 3348 4M-Byte Fixed-Head Disk
- Model 3385 Floppy Disk
- Model 3371 Line Printer
- Model 3365 Mag Tape
- Model 3368 Cartridge Mag Tape
- Model 3390 Commercial Disk Cartridge Drive Subsystem
- Model 4000 Commercial Disk Pack Drive Subsystem (96M Bytes)
- Model 4001 (Commercial Disk Pack Drive Subsystem (190M Bytes)

In addition, the MSE/14 supports several communications interfaces:

- Model 3769 Asynchronous Line Multiplexer
- Model 3767 Synchronous Line Multiplexer
- Model 3768 Cyclic Redundancy Check
- Model 3550 Multiprocessor Communications Adapter (MCA)
- Model 3551 Serial Multiprocessor Communications Adapter (SMCA)

The Model 3550 MCA (parallel) and the Model 3551 SMCA (bit serial) combine up to 15 ROLM and Data General processors in a multiprocessor system. The Model 3550 MCA allows a bus length of 150 feet; the Model 3551 SMCA allows a bus length of up to 1.25 miles (2 km).

Most ROLM Mil-Spec peripherals also have commercial versions that are software- and media-compatible with their Mil-Spec counterparts.

A full line of compact NTDS standard interfaces is also available for use with the MSE/14. These interfaces come in Slow, Fast, ANEW, and Serial types, with 8-, 16-, and 32-bit configurations, and are built to MIL-STD-1397.

In addition, the MIL-STD-1553A Bus is supported by ROLM's Model 3760 Interface.

I/O and Memory Expansion

The MSE/14 can expand its I/O capability and core memory capacity by adding an expansion chassis. There are three basic chassis to choose from:

Model 2166B—Combination I/O - Memory Chassis:
Provides 11 additional I/O slots and up to 128k bytes of core memory for core version memory expansion in a single ATR chassis.

Model 2146—Memory Expansion Chassis:
Provides up to 384k bytes of core memory for core version memory expansion. The basic configuration contains 64k bytes and can be expanded in 64k-byte increments.

Model 2150—I/O Expansion Chassis:
provides 15 addition I/O slots in a single ATR chassis.

Optional Temperature Ranges

The MSE/14 Processor in the core configuration is available in either of two optional temperature ranges. The wide temperature range offers an air inlet temperature from −25 °C to +60 °C. The extreme temperature range offers an air inlet temperature from −55 °C to +71 °C.

SOFTWARE

ROLM's MSE/14 Processor has been engineered to take full advantage of either ROLM's Advanced Real-Time System (ARTS) or Data General Corporation's Advanced Operating system (AOS).

Advanced Real-Time System

ARTS is a real-time operating system for ROLM Mil-Spec ECLIPSE processors. It contains the appropriate advanced real-time features of Data General's AOS, incorporating them into a compact, modular, and configurable system. ARTS is capable of supporting a wide range of system hardware configurations, from small to large memory capacity and with or without disk storage. It is designed to handle the real-time environment encountered in modern military systems without compromising performance.

ARTS is a downward compatible subset of AOS, with an emphasis on real-time response. It supports all of the basic features of AOS, except those that are unnecessary in a real-time system. This compatibility becomes very important during application development since extensive checkout can be done under AOS before moving to final checkout under the ARTS operating environment.

Data General's Advanced Operating System provides the development tools necessary to efficiently develop real-time ARTS application software. An AOS software development facility provides the dynamic environment required for source file editing, for assembly or compilation, and for binding of object files into a program file for execution. ARTS supports the high-order languages (FORTRAN 5, FORTRAN 77, DG/L, PL/I, and CMS-2M system programming languages) that are used to develop applications under AOS.

ARTS can be used in a wide variety of applications through various memory and peripheral device combinations. The ARTS application environment is characterized by a relatively small number of processes (1 to 32) that assume a known environment. The system can be tailored precisely to an application's requirements, ranging from a small memory-only configuration to a 2-megabyte system with multiple storage module disk units.

Advanced Operating System

AOS represents an intelligent multiprogramming operating system that can control the three most common computer environments: time-sharing, multiple batch job streams, and transaction processing. The AOS system has dynamic memory management capabilities, including generalized sharing of both code and data; management of all system resources based on user-established priorities and system measured changes in resource usage; sophisticated multiprogramming techniques, including concurrent control of multiple system and user processes, multitasking within processes, intertask and interprocess communications; and secure data management facilities, including multiple file access levels controlled by user privileges and hierarchical file directory structures.

For application development, AOS provides FORTRAN 5, FORTRAN 77, PL/I, and DG/L system programming languages, a sophisticated Macro-assembler, and programming aids

such as text editors and a symbolic debugger. AOS also supports the application development environment for ROLM's Advanced Real-Time System (ARTS), which is a real-time subset of AOS.

SERVICE

Ease of maintenance is a prime consideration at ROLM. The equipment is designed to minimize the need for service. Extensive diagnostics and operation and maintenance documentation are provided. As part of the support package of every system, ROLM provides two weeks of programming or maintenance training with each qualified system.

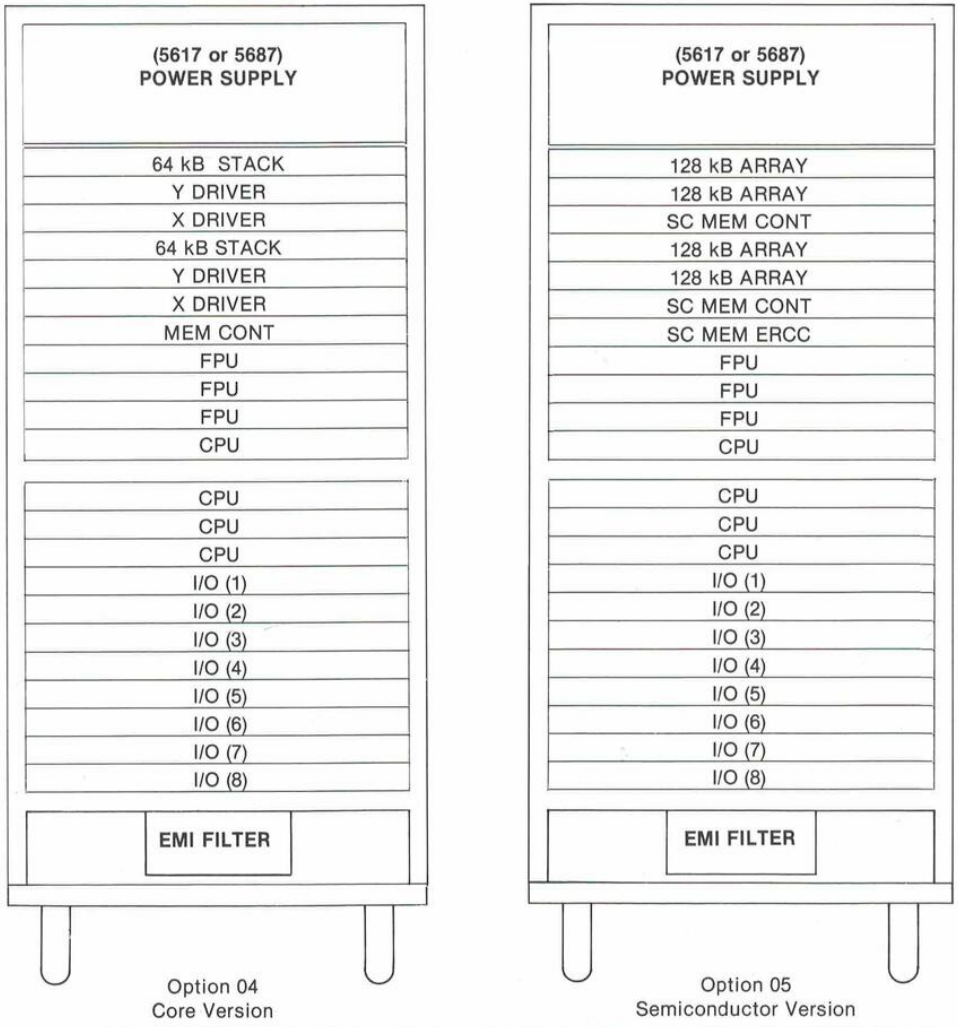
CONFIGURATIONS

The MSE/14 Processor comes in two versions, based on whether the main memory is core (Option 04) or semiconductor (Option 05).

The processor on both versions requires four boards, and the optional hardware Floating-Point Unit requires three boards. Each version has eight I/O slots which can be optionally wired pin-for-pin to the external I/O connector for configuration flexibility. If I/O interfaces selected are not compatible with this wiring, then dedicated wiring is provided. I/O capability can be expanded to external I/O chassis by using one or more of the slots for the Model 3561B I/O Expander.

The core version has 64k bytes of parity memory, which can be expanded internally by another 64k bytes. Up to a total of 2048k bytes can be added with external memory. The main memory of the semiconductor version is totally contained within the chassis. Either 128k bytes (standard), 256k bytes, 384k bytes, or 512k bytes of memory can be configured. Depending on the capacity, the semiconductor memory can be configured to be two-way interleaved or four-way interleaved. The main memory of the semiconductor version has an optional battery backup module which mounts external to the MSE/14 chassis. The Model 5617 power supply is standard for ac operation, and the Model 5687 power supply is optional for the dc operation.

MSE/14 CHASSIS CONFIGURATIONS



Option 04
Core Version

Option 05
Semiconductor Version

AOS Minimum Equipment Configuration (MEC)

MSE/14
256k Bytes of Memory
Floating-Point
System Console
10M-Byte Disk System
Programmable Interval Timer
9-Track Magnetic Tape

ARTS* Minimum Equipment Configuration (MEC)

MSE/14
64k Bytes of Memory
9-Track Magnetic Tape**

An AOS software development facility is required to develop ARTS application software.

***Any program load device can be substituted so long as it is compatible with the AOS software development facility.*

SPECIFICATIONS

Environmental

Inlet air temperature:
- Standard (0 °C to 50 °C)
- Wide (−25 °C to +60 °C)
- Extreme (−55 °C to +71 °C)

} Core memory only Option 04

Vibration:
10g, 5-2000 Hz, with vibration isolators (MIL-E-5400, Curve IVa), 2g, 5-2000 Hz, hard mounted (MIL-E-16400), Curve IIa)

Shock:
15g, 11 ms (MIL-E-5400) 400 lb hammer, with isolators (MIL-E-16400), (MIL-E-901C)

Humidity:
95% relative

EMI characteristics:
MIL-STD-461A

Altitude:
70,000 feet (22,966 meters) per MIL-E-5400 Class 2

Power

MSE/14 Input Power (Options):

Voltage	Frequency	Phase	
115 (92-130) Vac	47-63, 400	1	
220 (180-240) Vac	47-63	1	
115/200 Vac	400	3 (3-Wire)*	MIL-STD-704C
208 (180-240) Vac	47-63	3 (3-Wire)*	
+28 Vdc	—	—	MIL-STD-704C

MSE/14 Power Dissipation

575 watts Maximum on semiconductor version
65 watts Maximum on semiconductor version during battery back up
555 watts Maximum on core version

Model 2166B Combination I/O - Memory Chassis:
(Depends upon the amount of memory and the interfaces selected)

Model 2146 Memory Chassis:
90 watts (128k bytes), 135 watts (256k bytes)
47-400 Hz, 115 Vac

Model 2150 I/O Chassis:
(Power depends on interface selections)
47-400 Hz, 115 Vac

Size and Weight

MSE/14 Processor Chassis*:
7.62 in. × 13.30 in. × 24.19 in. (19.35 cm × 33.78 cm × 61.44 cm); 90 lb (40.90 kg) filled (with heat exchanger)

*WYE or DELTA

Model 2166B Combination I/O -
Memory Chassis*:
7.62 in. × 10.12 in. × 19.56 in. (19.35 cm × 25.70 cm × 49.68 cm); 70 lb (28.18 kg) filled (without heat exchanger)

Model 2150 I/O Chassis:
7.62 in. × 10.12 in. × 19.56 in. (19.35 cm × 25.70 cm × 49.68 cm); 62 lb (28.18 kg) filled (without heat exchanger)

Model 2146 Memory Chassis*:
7.62 in. × 13.30 in. × 24.19 in. (19.35 cm × 33.32 cm × 61.44 cm); 70 lb (31.81 kg) with 192k bytes memory (with heat exchanger)

Chassis without heat exchanger is a full ATR package with same dimensions as the Model 2150.

Processor

Instruction length:
16 bits (short class)
32 bits (extended class)

Data path:
16 bits

Hardware accumulators:
4 integer - 16 bits
4 floating-point - 64 bits (optional)

Index registers:
2 integer - 16 bits

Instruction types:
Fixed-point arithmetic
Logical operations
Character operations
Floating-point operations (optional)

Addressing modes:
Direct
Immediate
Indexed
Program counter relative
Accumulator relative
Multilevel indirect

Addressability:
Word (16-bit)
Byte (8-bit)
Bit (1-bit)

Bus structure:
Separate - Memory in
- Memory out
- I/O

(Cont.)

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SPECIFICATIONS (Cont.)

Memory

Core capacity:
- 128k bytes internal
- 1920k bytes external

Core access time:
- 400 nsec internal
- 700 nsec external

Core cycle time:
- 1μsec internal
- 1.1 μsec external

Core error checking:
- Parity, single-bit error detection

Core module capacity:
- 32k words × 17 bits

Semiconductor capacity:
- 512k bytes internal

Semiconductor cycle time:
- 400 nsec

Semiconductor interleaving:
- 2-way or 4-way

Semiconductor error checking:
- ERCC single-bit error detection and correction

Semiconductor module capacity:
- 64k words × 21 bits

Input/Output:

I/O Types:
- Programmed
- Data channel

Interrupts:
- 16 priority interrupt levels

Devices:
- 59 addressable devices

Performance

	Semiconductor	Core
Execution speed	830 KOPS	435 KOPS
Data channel input	1.7M bytes/sec	1.25M bytes/sec
Data channel output	1.42M bytes/sec	0.87M bytes/sec
Data channel latency (max)	7.6 μsec	6 μsec

Instruction Execution Times (μsec) — Typical

Standard set:

ADD	0.2 (1.0 for core)
MULT (unsigned)	4.0
DIV (unsigned)	2.4–7.4
MOV	0.2
JMP	1.2 (2.0 for core)
LDA	0.8 (2.0 for core)
STA	0.4 (2.0 for core)

Floating-Point Set	FPU	FIS
ADD (single)	2.0	27.0
ADD (double)	2.0	27.0
SUB (single)	1.8	26.6
SUB (double)	1.8	26.6
MUL (single)	3.4	41.6
MUL (double)	5.0	97.4
DIV (single)	7.0	74.6
DIV (double)	13.0	169.4

The materials contained herein are summary in nature, subject to change, and intended for general information only. Details and specifications concerning the use and operation of ROLM equipment and software are available in the applicable technical manuals.

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