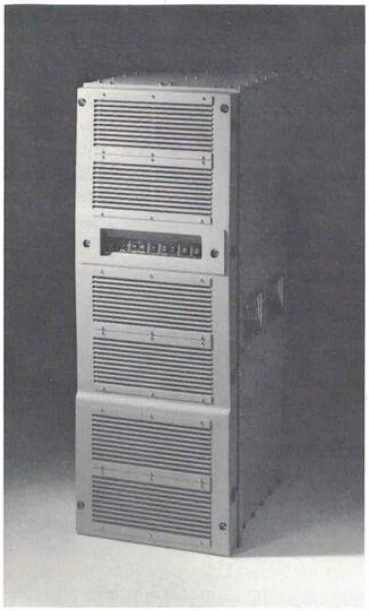
PRODUCT BRIEF

ROLM MIL-SPEC Computer Systems

MSE/800 MIL-SPEC ECLIPSE COMPUTER



FEATURES

- **Advanced 32-bit architecture**
- **Virtual addressability to 4 gigabytes**
- **Memory expansion to 8192k bytes**
- **Internal system bandwidth of 36.4 megabytes per second**
- **Eight-level hierarchical ring security system**
- **Advanced diagnostic capability**
- **Full Mil-Spec, software identical version of the Data General ECLIPSE® MV/8000 computer**
- **Designed to meet MIL-E-5400, MIL-E-16400, and MIL-E-4158 standards**
- **Advanced modular packaging**

DESCRIPTION

The MSE/800 is the most powerful Mil-Spec ECLIPSE computer available. It incorporates an advanced 32-bit architecture with up to 8 megabytes of main memory and provides over 4 gigabytes of virtual addressability. An efficient demand paging technique and high-speed I/O bandwidth let the MSE/800 make use of its vast logical space with maximum efficiency. Individual program user space can range up to 512 megabytes. This gives the MSE/800 the high capacity and performance needed for very-large-scale computational, real-time, and multiprogramming data processing.

MSE/800 systems feature an extensive data security mechanism and "fail-soft" reliability measures. The system's 4-gigabyte virtual address space is divided into 8 processing segments of 512 megabytes each for efficient memory management. An 8-level hierarchical ring structure partitions the system's 4-gigabyte logical address space to protect system resources. This ring structure is designed to directly correspond to the allocation of segments within the MSE/800 architecture, and it provides a hardware basis for an effective process protection mechanism.

The MSE/800 Availability, Reliability and Maintainability (ARM) system features are the most advanced ever incorporated in a Mil-Spec ECLIPSE computer. The System Control Processor (SCP) performs self-diagnostics on internal system functions, maintains a log of system errors, and identifies hardware faults to the field-replaceable unit level. It also lets operators inspect memory and step through programs to monitor both hardware and software performance. In addition, the MSE/800 incorporates modular system design for easy accessibility and fast maintenance.

The MSE/800 is fully software and electrically compatible with earlier Mil-Spec ECLIPSE computers. Programs developed to run under the Advanced Operating System (AOS) on Mil-Spec ECLIPSE computers can run without modification under the Advanced Operating System/Virtual Storage (AOS/VS) on MSE/800 systems.

Advanced Microprogrammed Architecture

The MSE/800 represents a major evolution of the Mil-Spec ECLILPSE system architecture. It provides a hardware foundation for addressing 4 gigabytes of virtual memory, and yet is fully program-compatible with other ECLIPSE models. The MSE/800 utilizes advanced bit slice and LSI architecture for high performance. A pipelined instruction processor lets the system make optimal use of its fast 220-nanosecond microcycle speed. The system cache and instruction cache memory modules accelerate MSE/800 operations. And extensive diagnostic capabilities help ensure the availability, reliability, and easy maintenance of all MSE/800 components.

The MSE/800 control storage is implemented entirely in high-speed RAM memory modules. It occupies a 4k- × 80-bit (75 standard, 5 used when optional FPU is installed) RAM memory area. Microdiagnostics are overlaid in this writable control store area for accurate and rapid fault isolation.

Instruction Processor

The MSE/800 Instruction Processor interprets instructions for execution. Instruction Processor operations are pipelined for optimum performance. The Instruction Processor maintains up to four instructions in the pipeline at one time, enabling one instruction execution in every microcycle. It simultaneously maintains one fully decoded instruction while a previously decoded instruction is being executed.

The Instruction Processor is buffered by a 1k-byte instruction cache, which is directly mapped to main memory. The MSE/800 transfers instructions from the instruction cache and data from the system cache to main memory simultaneously, to achieve even greater performance improvements.

System Cache

The MSE/800 uses a 16k-byte system memory cache to speed access to main memory. The system cache is ported to both the CPU and the I/O system, and it functions as a look-ahead and look-back buffer for the system. The system cache contains 1024 blocks of 16 bytes which are mapped directly to main memory locations.

The system cache optimizes performance for multiple operations by transferring data received from the CPU and I/O system to main memory at high speed. Transfers between the system cache and main memory occur at a rate of 16 bytes in 550 nanoseconds for write operations and 16 bytes in 440 nanoseconds for read operations. The MSE/800 further improves system cache transfer efficiency by simultaneously fetching data from the system cache and instructions from the instruction cache.

Address Translation Unit

The Address Translation Unit (ATU) is a hardware accelerator, or address cache, for the demand paging system. It effectively eliminates processor overhead for page translations by maintaining a table of recently referenced page addresses. During processing, memory references tend to cluster in page groups or working sets that are referenced repeatedly. The ATU stores a table of 256 recently referenced pages in a high-speed cache memory. When a program requests a page, the MSE/800 hardware first checks for the location of the requested page in the ATU cache. Since the majority of page references are kept in the ATU cache, this relieves the processor from having to regenerate the translation for every page reference. The ATU lets the system obtain page addresses at hardware speeds using the 36.4-megabyte internal I/O bandwidth, which results in dramatic performance efficiencies.

As the page cluster that forms a program's working set moves through memory, some of the pages become inactive and new pages are called in. The address translation unit provides information to AOS/VS's page replacement algorithm to identify the inactive pages so that they can be transferred back to disk storage or overwritten, making room for new entries in the address translation table.

To monitor the active status of all pages in its address table and to protect the integrity of the data kept on disk, the ATU maintains two bits for each physical memory page frame. These are the referenced bit and the modified bit.

The referenced bit indicates that an individual page has been referenced by software. AOS/VS's page replacement algorithm uses the referenced bit to determine which page in memory should be replaced by a new page being brought in from disk. Generally, the algorithm selects the least-frequently referenced page for replacement.

The modified bit, when set, indicates that a memory-resident page has been modified. When a page is replaced, its modified bit is examined. If the page is modified, it is written back to disk. If the page is not modified, the copy on disk is identical to the copy in memory, and thus no write-to-disk is necessary.

System Control Processor

The System Control Processor (SCP) is an independent diagnostic processor that provides the extensive "fail-soft" reliability measures implemented on the MSE/800. The SCP consists of a console control board and a NOVA® architecture processor board with a 4k-byte PROM and 32k-byte RAM memory. The 1.26-megabyte Model 8042 Mil-Spec Flexible Disk Drive provides ample storage capacity for error logs, diagnostic instruction sets, and a copy of the MSE/800 microcode. A terminal dedicated to the SCP system provides MSE/800 operators with soft system console facilities.

The System Control Processor automatically reloads the alterable microcoded control store of the MSE/800 every time the system is powered up. It can also be loaded under operator control. This design has many advantages. Operators can use the SCP to check control store validity, and upgrades can be installed by just loading a new copy of the microcode from floppy disk, instead of requiring the time-consuming task of rewiring processor boards.

A diagnostic bus connects the SCP console control board to other MSE/800 boards. If an error occurs in one of the boards, the SCP logs the error and determines its type, its location, and the time it occurred. For example, if the SCP detects a failure in the instruction cache, it can take the unit off-line. This lets the MSE/800 continue to operate in degraded mode, protecting critical processes until the problem can be corrected. The console control board also provides the system timing for all MSE/800 components.

The SCP runs programs designed to isolate hardware problems. Because the MSE/800 maintains all its control store in alterable memory, the SCP, under operator control, can preempt the control store when necessary, and run far more extensive diagnostic software than could otherwise be accommodated.

A terminal connected to the SCP enables it to act as a soft system console interface to the MSE/800. Operators can directly address MSE/800 memory locations and examine, load, and manipulate memory registers or stacks. The operating microcode can be verified against the duplicate copy maintained by the SCP, and either one can be verified against a reference file. Additional diagnostic and performance evaluation programs can be run and console operators can receive interactive reports. Operators can also single-step through programs instruction-by-instruction to examine the performance of applications software.

The SCP constantly monitors MSE/800 vital characteristics such as temperature and voltage. When any abnormality occurs, it notifies the operators so they can take the proper corrective action. Further, operators can use the SCP to test MSE/800 operations under abnormal conditions. The SCP can be directed to speed up or slow down the system clock and alter the voltage to the power supply, so that components can be stressed to more easily isolate and identify intermittent failures.

Instruction Set

The MSE/800 Instruction Set ensures fast, efficient machine response for large-scale computational and multiprogramming environments. The

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MSE/800 Instruction Set is a superset of the ECLIPSE instruction set, and is compatible with other ECLIPSE computers at the binary opcode level. The MSE/800 Instruction Set is implemented in microcode, which is loaded into the MSE/800 microsequencer by the System Control Processor.

MSE/800 instructions, which include 16- and 32-bit single-word instructions, can operate within the 64k-byte or 4-gigabyte addressing range. The MSE/800 Instruction Set supports 8-, 16-, and 32-bit fixed-point operands. It performs fixed-point arithmetic; bit, bit-string, byte, word and block manipulations; signed and unsigned integer multiply/divide and logical operations; single- and double-word binary and hexadecimal shifts; and single- and double-precision floating-point arithmetic operations.

The MSE/800 Instruction Set also supports queue and privileged instructions. Queue instructions operate on double-linked lists to improve the performance of operating system and high-level languages such as FORTRAN OR PL/I. MSE/800 privileged instructions are used by the operating system for direct control of the memory management system and other vital system resources.

Floating-Point Unit

The optional Floating-Point Unit (FPU) substantially increases the performance of double-precision (64-bit) floating-point operations. Totally transparent to application software, installation of the FPU requires no recompilation or reassembly. The FPU, implemented in one board, is inserted in a reserved processor slot.

Built around bit-sliced technology, the FPU uses a 64 ALU data path to manipulate operands in one machine cycle. Consequently, double-precision operations achieve performance increases from 2 to 4 times relative to processing without the FPU.

In addition to the expansion of the floating-point ALU width from 32 to 64 bits, the microinstruction is expanded to 80 bits, or a total control storage of 4k by 80 bits. When the FPU is not installed, only 75 bits of the microinstruction are decoded. The other 5 bits are reserved for the FPU. The extra control word width is used to support the high-performance FPU. Since control storage is RAM, a new copy of the MSE/800's microcode is provided on a floppy disk.

Hardware Stack Management

The MSE/800 system speeds stack management operations by maintaining stack parameters in hardware. The system uses four 32-bit registers. These include the stack pointer, the frame pointer, the stack limit, and the stack base register. The hardware stack is a last-in/first-out stack consisting of a series of variable-length frames that can be randomly accessed. A SAVE instruction saves the machine state during subroutine linkage and allocates a stack frame. A RETURN instruction reverses the procedure. PUSH and POP instructions save and restore single or multiple registers. The MSE/800 system incorporates stack protection features to automatically detect stack overflow or underflow. Additionally, MSE/800 system stack management facilities are designed to provide binary compatibility with other ECLIPSE system software.

Demand Paged Memory Management

The MSE/800 system provides up to 4 gigabytes of virtual address space divided into 8 segments of 512 megabytes each. This lets programmers develop lengthy program codes with vast address requirements without requiring them to divide their programs or invoke overlay techniques. MSE/800 programmers can have their programs reference any address within their addressing segment—or within any other accessible 512-megabyte segment, up to the limit of 4 gigabytes.

The MSE/800 system accomplishes efficient use of 4 gigabytes of virtual addressability within its cost-effective configuration capacity of 8 megabytes of physically addressable main memory through the use of sophisticated demand-paged memory management techniques.

Only the program addresses which comprise the working set of a user's program are kept resident in the main memory. The remainder of the logical addresses in a user program is kept in on-line disk storage. All the logical addresses in the MSE/800 system are divided into 2k-byte pages. For each program, the MSE/800 system translates the user's logical addresses into physical addresses in the system's main memory modules.

During processing, the system uses high-speed microprogrammed RAM memory units to examine the logical addresses used by an active program. It traps program references to pages that are not resident in main memory and switches control to operating system software to execute the transfer of the page containing the requested addresses from secondary storage to memory. The MSE/800 system's mapping and demand paging technique ensures high performance because it allows program requests for memory to use any available memory locations as soon as they become available, regardless of their physical location. The MSE/800 demand paging technique does not require contiguous physical addresses for processing. It also lets multiple processes or programs share individual memory locations.

Security Mechanism

The Address Translation Unit also provides the logic to enforce the MSE/800 system's hardware-based security mechanism. The system imposes an 8-level ring structure on its 4 gigabytes of virtual address space; each ring directly corresponds to one of the 8 processing segments established for efficient memory managament. An access gate is added to each ring in the hierachy so that the rings may be logically arranged in a processing-privilege hierarchy. Highest privilege resides in the innermost ring, and higher privilege processes may access and control lower privilege rings. When a process in a higher-privilege ring issues an instruction to execute code in a lower-privilege ring, however, it must transfer control to that ring. The system performs this operation as a return from a subroutine call. Conversely, outer rings can transfer control to inner, higher-privilege rings, but they do not receive read or write access to inner rings.

A typical arrangement of an MSE/800 ring structure is to dedicate the innermost rings to critical system processes—with operating system software in the innermost ring (ring 0), for example, and with file system software in ring 1, peripheral management software in ring 2, and data base software in ring 4. User programs could reside in the outermost, lowest-priority 512-megabyte processing areas, rings 6 and 7.

User requests for system resources must cross these ring boundaries. The ATU checks access privileges and entry points to the various rings before any processing is allowed to

occur. After the ATU has verified that a ring transfer request for system resources contains the proper access codes, it performs a series of additional checks. For example, the ATU checks the read, write, and execute bits of each page in the transfer to see that they allow a specific operation. It identifies and traps all pages in which faults occur. The ATU allows system software to handle requests resulting in faults.

Bank Controller

The MSE/800 Bank Controller controls the selection of a memory module when it receives an address from the system cache. It also performs error checking and correction on data transfers between the bank controller and main memory, and provides byte parity checking on data transfers it receives from the system cache.

The bank controller puts the entire contents of the MSE/800 main memory through a complete ERCC check (1 second for every 1 megabyte of main memory). It accomplishes this in the course of performing refresh operations on the dynamic RAM memory modules. It reads one 16-byte block and puts it through a complete error checking and correction process, then writes it back to the memory module. It repeats this operation on a different block during each refresh cycle, and progresses sequentially through the entire contents of main memory every 8 seconds for an 8-megabyte system. This process reduces the possibility of single-bit errors accumulating in less-frequently referenced locations.

Input/Output System

The MSE/800 system incorporates a three-level independent Input/Output system. It includes a 16.16-megabyte-per-second Burst Multiplexer Channel (BMC) for direct memory access by high-speed disk storage subsystems, a 2.27-megabyte-per-second Data Channel for medium- to high-speed devices, and a Model 8041 Input/Output Processor for character-oriented devices.

The MSE/800 provides a high-speed 16k-byte system cache to buffer all memory I/O. Transfers between storage subsystems and the system cache occur at 18.2 megabytes per second. Internal system transfers between the system cache and the MSE/800 memory system occur at 36.4 megabytes per second. The BMC and the Data Channel transfer data directly from disk to the system cache. The Input/Output Processor collects character-oriented transmissions and sends them to the system cache in high-speed bursts, minimizing system overhead.

Software

MSE/800 software support is provided by the Advanced Operating System/Virtual Storage (AOS/VS), a multifunction, multilanguage software system that, depending upon the application, may let up to 128 users simultaneously develop and execute interactive and batch-oriented operations in a secure environment. AOS/VS performs extensive system resource optimization, and lets multiple users simultaneously develop and execute programs in both 16- and 32-bit mode. AOS/VS program modules and data bases are allowed to reside within each user's logical address space as a process-wide context. This improves performance and reduces overhead for operating system services because programs running MSE/800 systems can use the CALL instruction to invoke AOS/VS services like any other subroutine call.

The 32-bit high-level language support includes ANSI FORTRAN 77, ANSI General-Purpose Subset PL/I, ANSI BASIC, ANSI COBOL, and APL. All these languages have been implemented integrally with the MSE/800 computer for maximum efficiency and performance. The SWAT™ Native Language Debugger provides source and code level debugging facilities for AOS/VS FORTRAN 77, PL/I, and COBOL programs.

AOS/VS language support for 64k-byte addressing range includes AOS COBOL, globally optimizing FORTRAN 5, PL/I, Extended BASIC, RPG II, DG/L™ Structured Programming Language, and Macroassembler. AOS-standard software systems support for 64k-byte addressing range includes the INFOS® II File Management System, Data General/Data Base Management System (DG/DBMS), Data General's Transaction Processing Management System (TPMS), AZ-TEXT™ Word Processing Software, and Idea (Interactive data entry/access) software.

Programming

The MSE/800 system was designed for complete software compatibility with AOS-based ECLIPSE computers. The MSE/800 instruction set is an upward-compatible superset of other ECLIPSE instructions sets, and the ECLIPSE instruction set is a superset of the NOVA instruction set. This allows programs written for ECLIPSE or NOVA computers to run on the MSE/800 without rewriting, changing mode, or recompiling. Conversely, programmers can use the MSE/800 as a development system for 16-bit Mil-Spec ECLIPSE systems, provided only that they limit their programs to the instruction parameters, operating system features, and address capacity of the smaller machines.

Further, the MSE/800 operating system, AOS/VS, gives programmers essentially the same interface as AOS. It uses the same CLI commands. Programming in 512-megabyte addressing range is made even easier by the fact that AOS/VS does not require overlays; the extremely large-scale data handling facilities of the MSE/800 are sufficient for the largest arrays and programs.

CONFIGURATION

System Configuration

A typical system includes several items:

Model 800 Processor
Model 8001 Floating-Point Unit (FPU)
Model 8020 and 8024 Memory Units, as desired
Model 8040 Expander, to terminate the I/O bus and expand it beyond the main chassis
Model 8041 I/O Processor
Model 8042 Mil-Spec Flexible Disk Drive
Model 8043 or Model 8044 ac/dc Converter, if desired for input power conditioning
Model 4051 Mil-Spec Disk Subsystem
Model 4052 Mil-Spec Slave Disks, as desired
Model 3369 Magnetic Tape Controller
Model 3365 Magnetic Tape Unit
Model 8050 I/O Chassis, and Keyboard/Display terminals, for system control and application requirements
Model 9900 AOS/VS Operating System, and other software as desired.

This configuration is normally augmented by interfaces and peripheral devices as required by the application.

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Peripherals and Options

The MSE/800 system is designed to be electrically compatible with other ECLIPSE systems. This allows the MSE/800 to use ROLM®Mil-Spec and commercial peripheral products, including auxiliary disks, industry-compatible magnetic tape drives, display, line printers, and card readers.

The MSE/800 accepts both 16-bit and 32-bit word storage formats. This allows existing Mil-Spec ECLIPSE compatible devices to run directly on the MSE/800 without data conversion.

ROLM also offers a broad line of general- and special-purpose I/O interfaces, including a complete line of NTDS interfaces.

SPECIFICATIONS

Functional

Memory Word Length:
32 bits
Data Length:
8-, 16-, 32- and 64-bits
Hardware Registers:
4 fixed point
4 double-precision float
1 PC
4 stack management
Address Modes:
Direct addressing of 64k bytes and 4 gigabytes
Memory Cycle Time:
880 nanoseconds per 16-byte block to system cache
Memory Capacity:
8 megabytes (semiconductor memory)
Memory Increments:
256k bytes, 1024k bytes
System Cache:
16k-byte Direct Mapped, write-back
Instruction Cache:
1k-byte Direct Mapped
Instruction Pipeline:
4 levels
Page Size:
2048 bytes
Referenced/Modified Bits:
One pair per each page frame
Address Translation Unit:
256 Entry, Direct Mapped, 512k-byte working set
Logical Address Space:
4 gigabytes
Segment Size:
512M bytes
Number of Segments:
8
Number of Rings:
8
Page Table Structure:
One or two levels per segment
1 level—1M-byte logical address space
2 level—512M-byte logical address space
Maximum I/O transfer rate:
18.2M bytes/sec (combined)
Burst Multiplexer Channel:
Maximum transfer rate—
16.16M bytes/sec input
14.54M bytes/sec output
Data Channel:
Maximum transfer rate—
2.27M bytes/sec input
1.3M bytes/sec output
Input/Output System:
16- and 32-bit word length, 16 priority interrupt levels
57 devices addressable

Environmental

Inlet air temperature:
0°C to +50°C
Vibration:
MIL-STD-167 Type I (4 to 50 Hz) hardmounted
MIL-STD-810C, method 514.2
Shock:
MIL-STD-810C method 516.2
Procedure I (15g, 11 msec)
Procedure III (30g, 11 msec)
Procedure V (bench handling)
MIL-S-901C, grade A, Class II
Medium weight type A (3000 lb hammer)
EMI:
MIL-STD-461A notice 3
MIL-STD-461A notice 1 (with Model 8043 or 8044 ac-dc converter)
Humidity:
To 95° relative humidity per MIL-STD-810C method 507.1 procedure 1
Sand and Dust:
MIL-STD-810C method 510.1
Explosive Atmosphere:
MIL-STD-810C method 511.1
Fungus:
MIL-STD-810C method 508.1
Salt Spray:
MIL-STD-810C method 509.1

General

Power:
115/200 Vac 400 Hz 3-phase (4-wire) 8A (typical) per phase (per MIL-STD-704C)
115 Vac 60 Hz 3-phase (3-wire) 14A (typical) per phase Type 1 power per DOD-STD-1399 Section 300 (Model 8043 ac-dc converter optional)
208 Vac 60 Hz 3-phase (3-wire) 8A (typical) per phase (with Model 8043 ac-dc converter)
440 Vac 60 Hz 3-phase (3-wire) 4A (typical) per phase (Type 1 power per DOD-STD-1399 Section 300) (with Model 8044 ac-dc converter)
380 Vac 50 Hz 3-phase (3-wire) 5A (typical) per phase (with Model 8044 ac-dc converter)
Heat Generated:
13,500 BTUs per hour
Dimensions:
46 in. high × 17.5 in. wide × 24 in. deep
(116.84 cm × 44.45 cm × 60.96 cm)
Weight:
610 lb

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The materials contained herein are summary in nature, subject to change, and intended for general information only. Details and specifications concerning the use and operation of ROLM equipment and software are available in the applicable technical manuals.

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