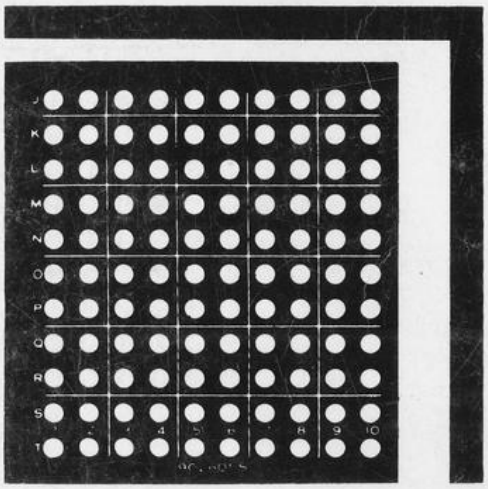
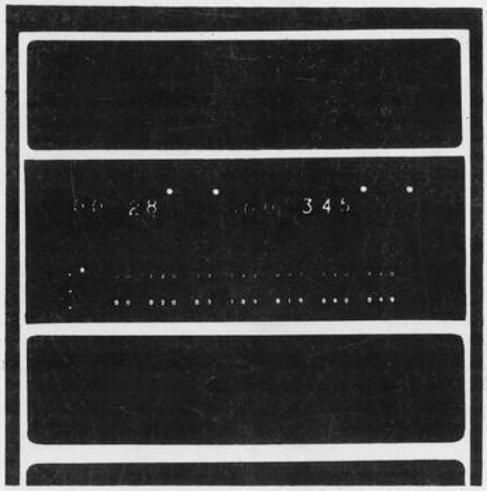
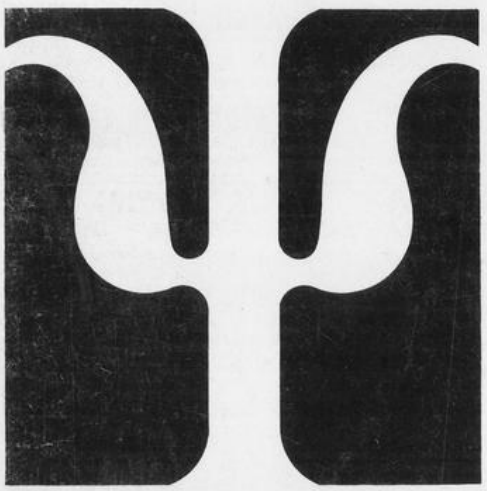
lab handbook







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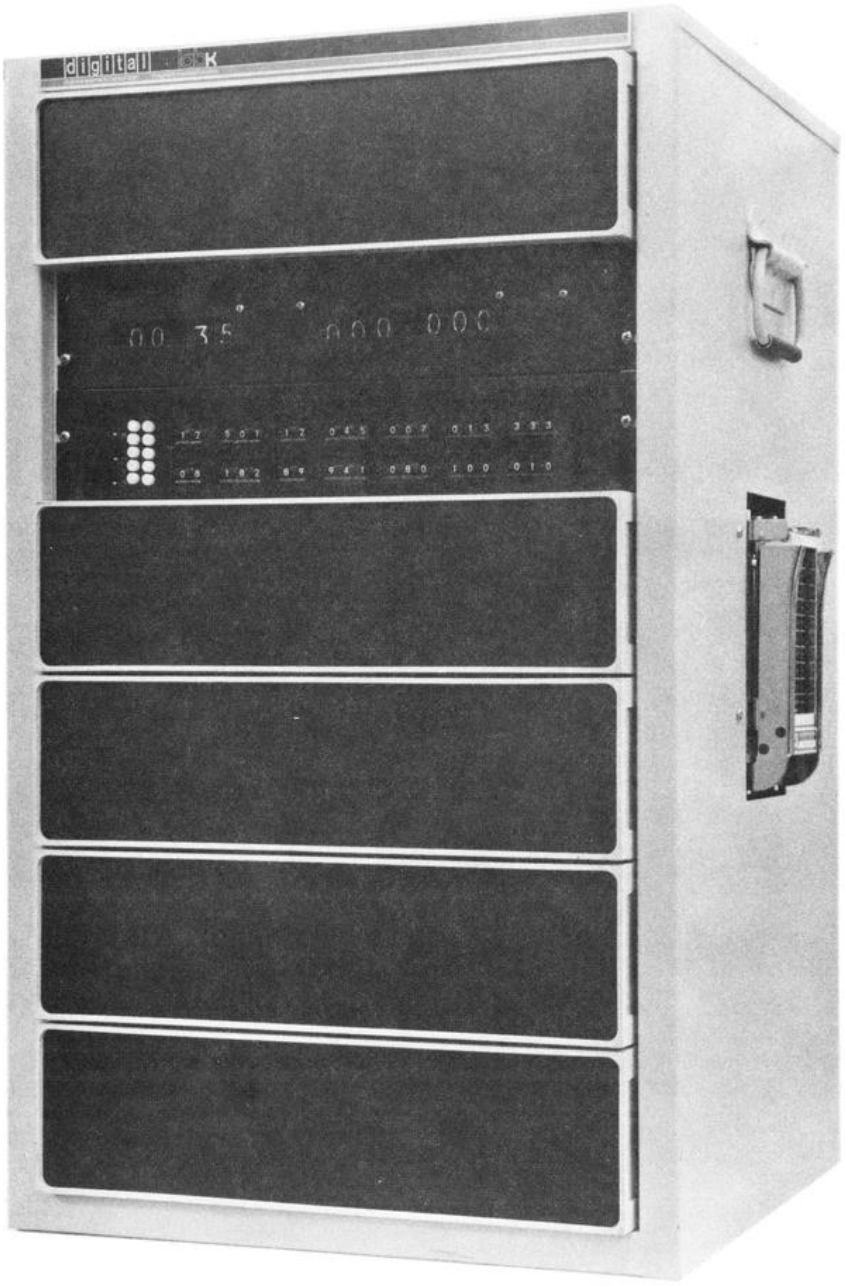


The LAB-K Controller

CHAPTER 1
INTRODUCTION

The LAB-K is designed to assist the research psychologist in precisely controlling time and events in experiments. The LAB-K can be programmed for either subject or experimenter paced control. After the components of an experiment have been programmed on the LAB-K patchboard and the experiment has commenced, program components are accommodated and executed sequentially without any assistance from the researcher.

Basically, the LAB-K consists of a group of logic kits, each of which is designed to execute a specific logical operation. A 200-position, prewired plugboard integrates these logic operations and provides the control function for the LAB-K. The plugboard is "patched up", i.e., programmed by means of plug wires. Plugboard programming provides the researcher with complete control of functional capabilities; as an added benefit, it is possible to maintain a permanent record of programs for future use, or for conversion to computer software. Each logic kit consists of a group of functionally related modules. Individual modules are combined to yield a general function or application (for example, a down counter).

Modules are interconnected by plugging them into the module mounting rack. Consequently, expanding the LAB-K is a simple matter of plugging optional modules into the mounting rack.

There are two LAB-K logic configurations: basic and optional. Each kit is designated by application and identified by a capital letter. The basic configuration consists of six kits, as follows:

Kit	Application
Input Logic	A
1-s, 10-s, 60-s Time Bases	D
0 – 9 Sequencer	B
Down Counter	C
Up Counter	E
Output Logic	F

These kits, which can be used without any additional logic, provide the researcher with a functional logic controller. If the nature of the particular research requires additional controls, the basic configuration can be expanded by utilizing the following optional kits:

Kit	Application
.001-s, .01-s, .1-s Time Bases	L
VI/VR Programmer	M
Second VI/VR Programmer	P
IRT Programmer	Q
Session Timer	N

In general, the LAB-K controls and counts empirical data. It can accommodate from 1 to 10 functional components or steps, that is, operant schedules or discrete trials.

These functional components are programmed on the plugboard and sequentially implemented by a sequencer that has a ten-step capability. The sequencer steps the components of a schedule according to the responses of an organism (subject paced control), or according to a predetermined time interval that is not dependent on the responses of an organism (experimenter paced control).

In subject paced control, the LAB-K is used to step schedule components, count intervals, and provide signals to external equipment (lighting lamps, or providing reinforcement, etc.). Schedule components are "chained" together on the patch-board and sequentially stepped by the sequencer. If, for example, a schedule consists of a fixed ratio, a fixed interval, and a DRL, then these components are chained together on the plugboard, and the sequencer steps the schedule from component to component.

Individual components are programmed by implementing the appropriate LAB-K logic. To program a fixed interval, it is necessary to select a time base, set a predetermined number into a down counter, and then connect these points to a step on the sequencer.

If, for example, this component is going to be run on step 1, then the above mentioned points are connected to step 1. The logic within the component is enabled (logically prepared) when the sequencer steps to step 1. A time base is enabled into the down counter, the thumbwheel switch is enabled and, subsequently, the number to which it has been set is read into the down counter.

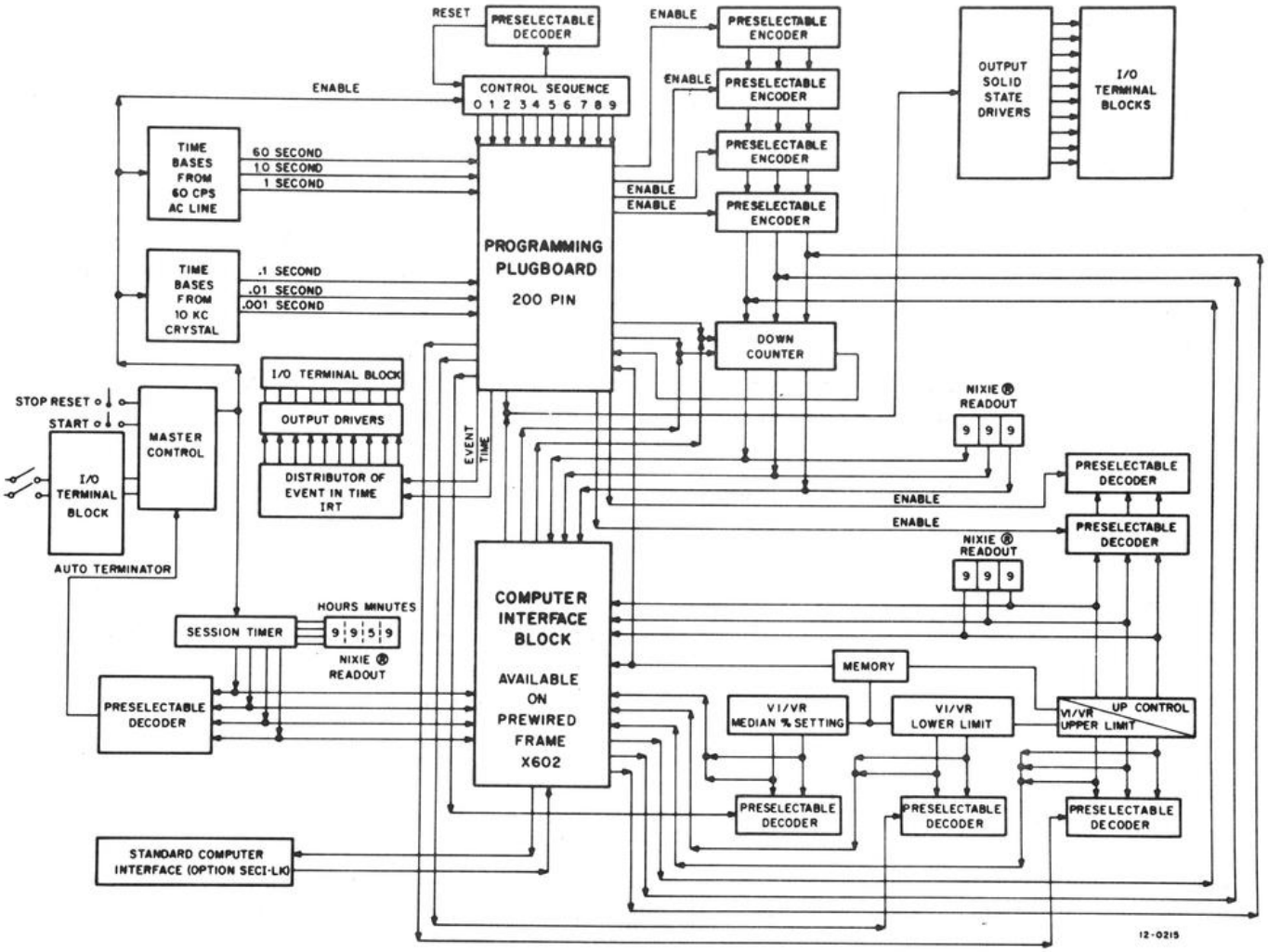
Termination of the component depends on the component contingency, e.g., down counter on zero, down counter on zero + event, etc. This contingency is connected to the next step on the sequencer; thus, the sequencer is stepped only when a contingency is true.

The following block diagram illustrates the manner in which the logic kits are controlled by the sequencer. Any logic within a kit that is connected to a step on the sequencer (0–9) is enabled when a step is true.

The sequencer step (pulse) activates logic components such as counters, one shots, and so on; and it also enables gates by putting them in an "if, then" state. For example, if event X occurs, it triggers only the gate that has been enabled by the sequencer; then, this gate changes state and subsequently effects another result, as providing reinforcement, or energizing a lamp.

In experimenter paced control, the plugboard is programmed in the same manner as subject paced control, but the implementation of the LAB-K logic is not contingent upon the response of an organism. In this type of experiment, the LAB-K is used to enable sequentially preselected stimuli and count data within a timed interval.

In experimenter paced control, time and events (or a large number of intervals) can be recorded in relation to a stimulus. For example, the research psychologist can, through programming the LAB-K, initiate a time period while a stimulus is in progress, or start a time period while a tone period is in progress, etc. Thus, the researcher can count and record data over a fixed period. For example: a researcher wants to collect heartbeats over a 30-minute period; the experiment is scheduled to run for 2 hours, and three stimuli are going to be presented sequentially. The researcher wants to determine the heart rate before the first stimulus, the heart rate after the first stimulus, and the heart rate 10 seconds before the second stimulus.



This is achieved with the LAB-K enabling the stimuli with steps on the sequencer and recording responses on an IRT counter. Thus, the researcher can evaluate his responses within a fixed time period.

Normally, this type of scheduling requires 8 to 10 timers. The LAB-K, however, allows the researcher to reduce the number of counters necessary. The number of counters available depends on the number of thumbwheel switches available to encode or decode the counters.

The LAB-K provides the researcher with the hardware and the logic necessary to control the functional components (FI, FR, etc.) of most common experiments. The LAB-K contains most of the logic a researcher will need to design his own control systems.

Before the introduction of the LAB-K Controller, the researcher could not design his own control system unless he possessed a knowledge of an Electronics Engineer. Digital's solution to the complex control problem is Module Level Design (MLD). MLD is a program that allows the researcher to design his own control systems through the use of digital logic. To achieve this end, the researcher must acquire a thorough knowledge of digital logic. This knowledge allows the researcher to analyze and use electronic circuits, though he may not possess an extensive background in Electronic Engineering.

After the principles of digital logic have been mastered, the user can design a control system using the MLD system by simply selecting the K Series modules needed for the implementation of specific logic functions; and arranging the modules into a functional control system.

Logic functions, or modules, are interconnected to form a functional control system, using a 200-position plugboard. The plugboard provides access to the input logic (event signals, etc.), application logic (counters, control gates and flip-flops, etc.), and output logic (drivers, etc.). Plug wires are used to interconnect this logic.

Programming the LAB-K and implementing the MLD system requires an understanding of the LAB-K hardware, K Series logic, and the control function of each kit. This information is contained in Chapters 2, 3, and 4.

Chapter 2 (Step-By-Step Assembly of LAB-K) is written in a step-by-step format and well supported by illustrations. If the assembly procedures are followed carefully, LAB-K assembly is a relatively easy task.

By assembling the LAB-K, the researcher gains firsthand knowledge of the mechanical and electrical components that comprise the LAB-K. An understanding of how the LAB-K components are used ensures optimum use of the LAB-K logic; and, after the principles of digital logic are mastered, it facilitates troubleshooting. The researcher also develops a knowledge of soldering and wiring techniques by assembling the LAB-K. These skills are necessary if the researcher desires to modify the LAB-K for a special control function.

Chapter 3 (Building Blocks of Digital Logic) provides an introduction to the principles of digital logic. The K Series logic symbology (the positive logic used in the LAB-K), is used to demonstrate the various operators of digital logic. A thorough understanding of this material enables the researcher to evaluate the LAB-K electronic circuits (schematically represented in the symbology of digital logic). Circuit evaluation is an essential part of plugboard programming and Module Level Design.

Chapter 4 (Application Notes) outlines the various applications of LAB-K kits in the control of time and events. Chapter 4 also contains sample plugboard programs for the control of individual functional components and one multiple schedule program. This information provides the researcher with the ability to control time and events in most life science experiments.

Each sample program is presented in a format that enables the researcher to develop a facility for controlling the time and events of experiments through the implementation of digital logic. The logic principles used in these sample programs can be used as a guideline when the researcher desires to design his own control system.

Chapter 5 (Checkout Procedure) provides the necessary information for integrating each kit into the LAB-K system, and then verifying that the kit is operational. By checking out the LAB-K logic, the researcher reinforces his knowledge of digital logic and gains practical experience in analyzing electronic circuits on the logic level.

CHAPTER 2
STEP-BY-STEP ASSEMBLY OF LAB-K

Before assembling the LAB-K, perform the following procedure:

Step	Procedure
1	Lay out, in a display, the major assembly units (see hardware list), as follows: a. Cabinet and hardware b. Power Supply c. Modular mounting panels and hardware d. Input/output connection hardware e. Logic modules
2	Check the sub-assembly components of the above units against the parts list; and, if there are any items missing, immediately notify Digital Equipment Corporation.
3	Turn to the Appendix C and read the section on wire insulation stripping, solderless and soldered connections.

NOTE

Prefix the name of any assembly unit with the cabinet serial number when ordering additions to LAB-K from Digital Equipment Corporation.

CAUTION

Step-by-step instructions for assembling the LAB-K are given in the following sections. The unit must be assembled in essentially the same sequence as outlined in this manual.

2.1 MODULAR MOUNTING PANEL

Assemble and mount the Modular Mounting Panel (see Figure 2-1), as follows:

NOTE

If you have purchased the X602 automatic Wirewrap Frame (Option R), perform steps 3a, 3b, and 3c, and turn to Section 2.3.

Step	Procedure
1	Mount the H800 and H808 Connector Blocks on the H020 Mounting Frame, as shown in Figure 2-2. Use the K943S mounting panel as a guide.
2	Mount the Ground Lugs (see Figure 2-1) on the H020 Mounting Bar of racks 2 and 3 at slot positions 4, 12, 20 and 28 (see Figure 2-3).
3	Make the power supply connections on the K943S (rack 1).

a. Prepare the following hook-up wire (Strip 1/4 in. from both ends of each wire.):

- (1) 35 in. orange (+5)
- (1) 35 in. black (ground)
- (1) 6-1/4 in. orange

NOTE

All wire used in this kit, unless specified otherwise, is 18 gauge.

b. Make the following connections, and solder in place (Use Figure 2-3 as a guide.):

( ) 35 in. black to pin C, slot 32, row A
( ) 6-1/4 in. orange from pin A, slot 32, row A, to pin A, slot 32, row B.
( ) 35 in. orange to pin A, slot 32, row B.

c. Make a twisted-pair out of the 32 in. orange and black wires. (Leave about 2-1/2 in. untwisted at the unconnected end.) Wrap the twisted portion of the wire in spaghetti, and slip it between the connector block and the mounting bar.

NOTE

If you have the X602 option, repeat steps 3a, 3b, and 3c for rows C and D (mounting rack 2) and rows E and F (mounting rack 3).

Step	Procedure
4	On rack 2, rows C and D, mount the 932 Bus Strips (Figure 2-1), and make the power supply connections.

a. Insert a 932 Bus Strip on the A pins of row C from slot 5 to slot 16 (12 pins) and from slot 21 to slot 32 (12 pins). (The 932 Bus Strip must be cut to size.) In the same slot positions, insert the 932 Bus Strips on the C pins of row C.

b. Insert the 932 Bus Strips in row D at the slot positions designated in step 4a.

c. Solder, at each pin, the 932 Bus Strips in rows C and D. (Use the K943S as a guide.)

d. Prepare the following lengths of hook-up wire. (Strip 1/4 in. from both ends of each wire.)

(2) 6-1/4 in. orange	(4) 7/8 in. black	(4) 1-1/2 in. black
(6) 1-3/8 in. orange	(1) 29 in. black	(1) 23 in. black
(6) 1-3/8 in. black	(1) 29 in. orange	(1) 23 in. orange
(4) 7/8 in. orange	(4) 2-1/2 in. black	

e. In row C, make the following connections, and solder in place (see Figure 2-3).

( ) 1-3/8 in. orange from pin A, slot 16, to pin A2, slot 18.

( ) 1-3/8 in. orange from pin A2, slot 18, to pin A2, slot 20.

( ) 7/8 in. orange from pin A2, slot 20, to pin A, slot 21.

( ) 1-3/8 in. black from pin C, slot 16, to pin C2, slot 18.

( ) 1-3/8 in. black from pin C2, slot 18, to pin C2, slot 20.

( ) 7/8 in. black from pin C2, slot 20, to pin C, slot 21.

f. Make the above connections (step 4e) in row D.

g. Make the following connections, and solder in place (see Figure 2-3 and use the K943S, rack 1, as a guide).

( ) 2-1/2 in. black from pin C, slot 5, row C, to the Ground Lug.

( ) 1-1/2 in. black from the Ground Lug to pin C, slot 5, row D.

( ) 2-1/2 in. black from pin C, slot 27, row C, to the Ground Lug.

( ) 1-1/2 in. black from Ground Lug to pin C, slot 27, row D.

h. Refer to steps 3b and 3c, and make power supply connections using the 29 in. black and 29 in. orange wires.

5 On Rack 3, rows E and F, mount the 932 Bus Strips, and make the power supply connections.

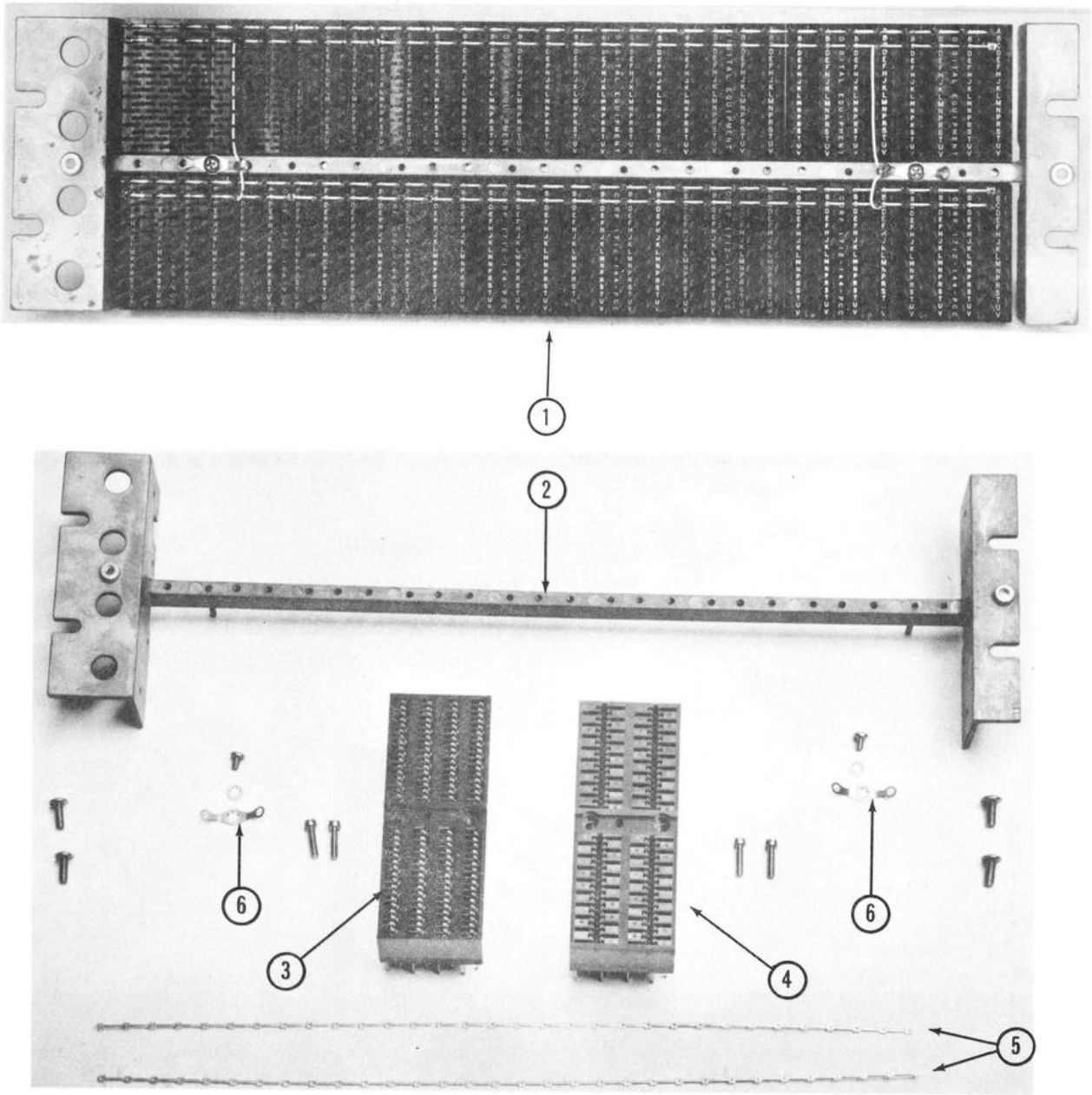
a. Insert a 932 Bus Strip on the A pins of row E from slot 5 to slot 32 (28 pins). In the same slot positions, insert a 932 Bus Strip on the C pins of row E.

b. Insert the 932 Bus Strips in row F at the slot positions designated in step 5a.

Step	Procedure
5 (cont)	c. Solder, at each pin, the 932 Bus Strips in rows E and F.
	d. In row E, make the following connections, and solder in place. ( ) 1-3/8 in. orange from pin A2, slot 2, to pin A2, slot 4. ( ) 7/8 in. orange from pin A2, slot 4, to pin A, slot 5. ( ) 1-3/8 in. black from pin C2, slot 2, to pin C2, slot 4. ( ) 7/8 in. black from pin C2, slot 4, to pin C, slot 5.
	e. Make the above connections (step 5d) in Row F.
	f. Refer to Steps 3b and 3c, and make the power supply connections using the 23 in. black and 23 in. orange wires.
6	Mount the three modular mounting racks on the H953A Cabinet at the locations shown in Figure 2-4.

CAUTION

Ensure that the racks are mounted in the proper locations.



INDEX	QUANITY	NOMENCLATURE
1	1	K943S MODULAR MOUNTING PANEL
2	2	H020 MOUNTING FRAME
3	13	H800 CONNECTOR BLOCK
4	3	H808 CONNECTOR BLOCK
5	8	932 BUS STRIPS
6	8	GROUND LUGS

Figure 2-1 Modular Mounting Panel

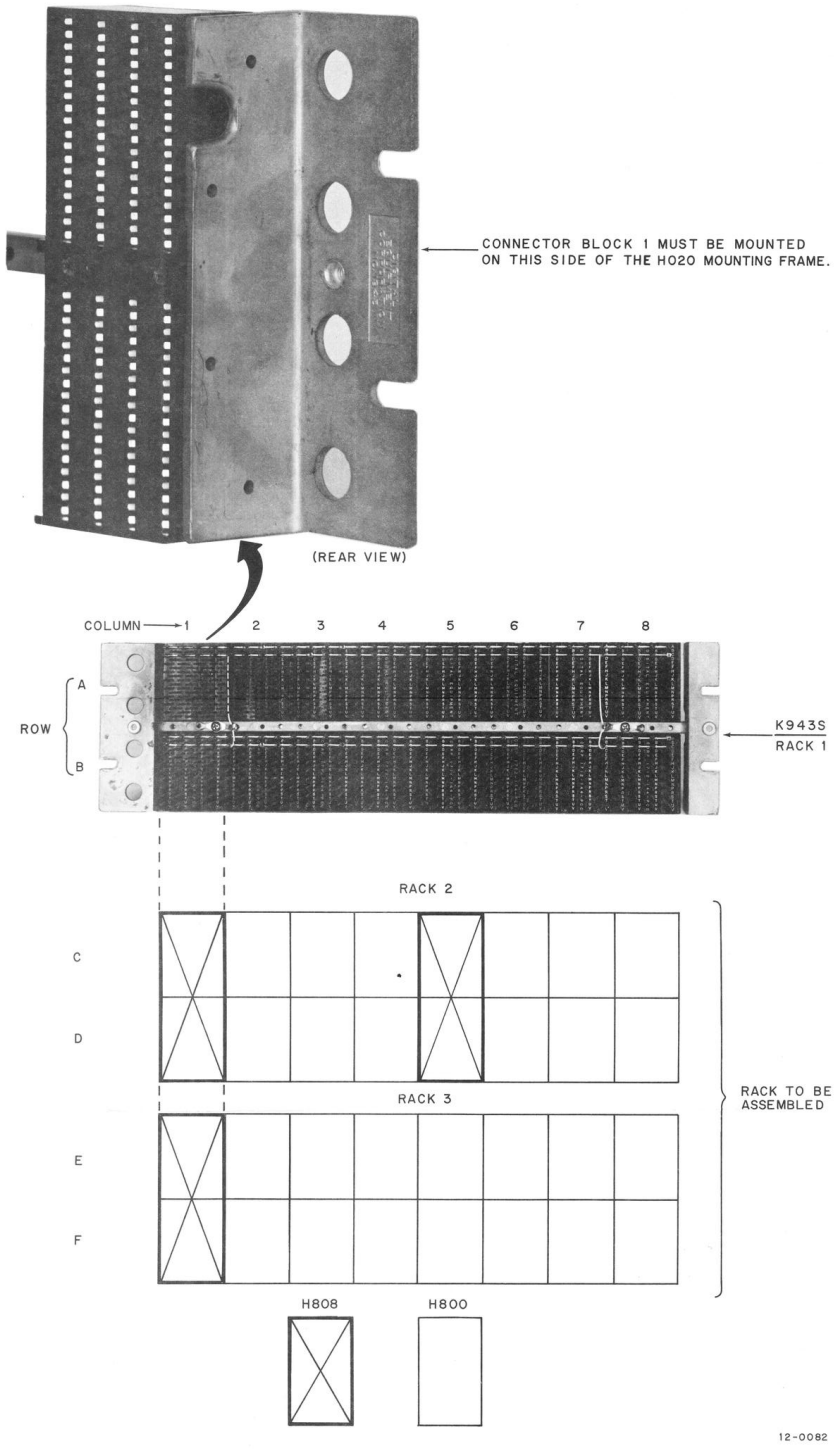


Figure 2-2 Connector Block Mounting Locations

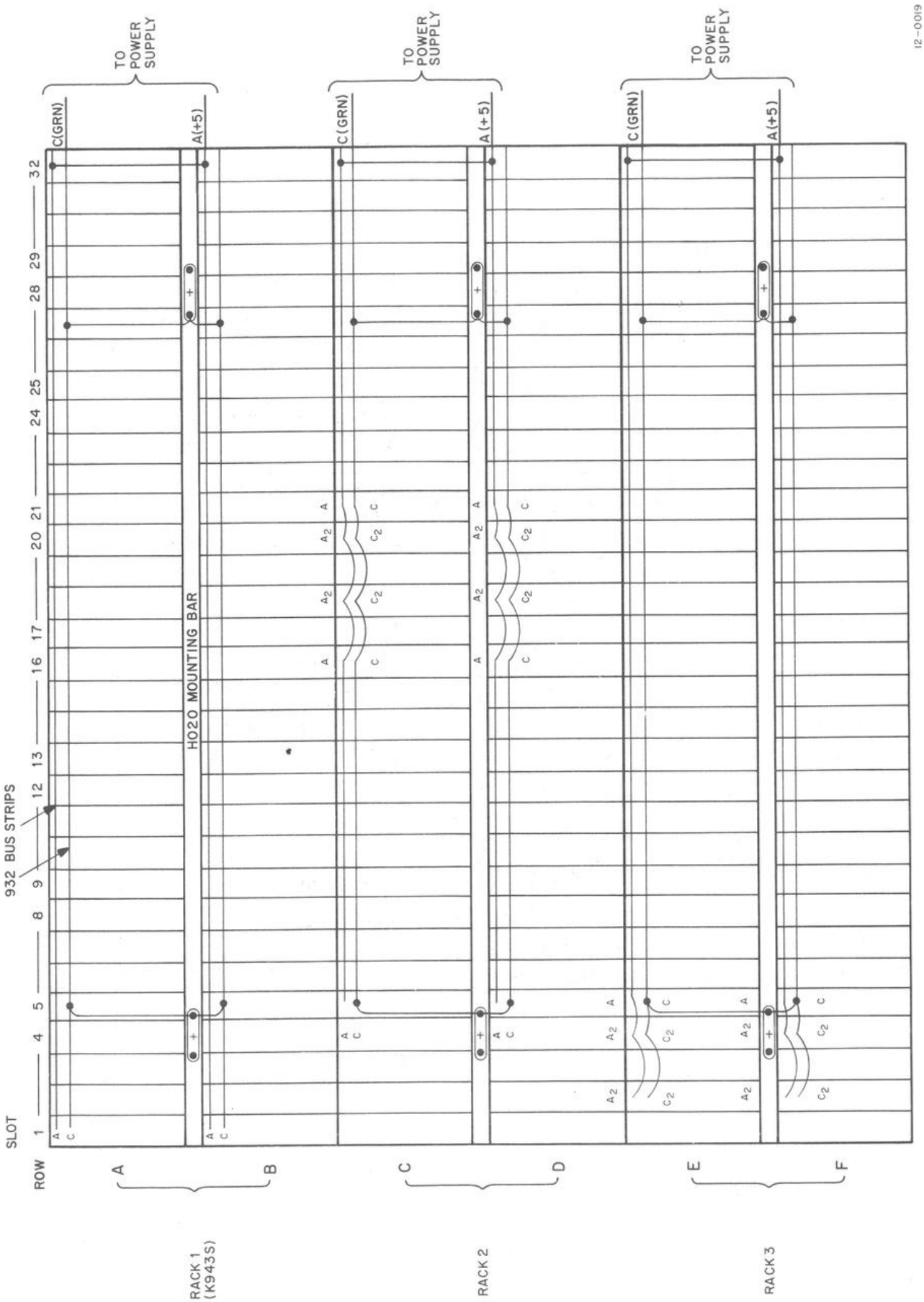


Figure 2-3 Module Rack Wiring

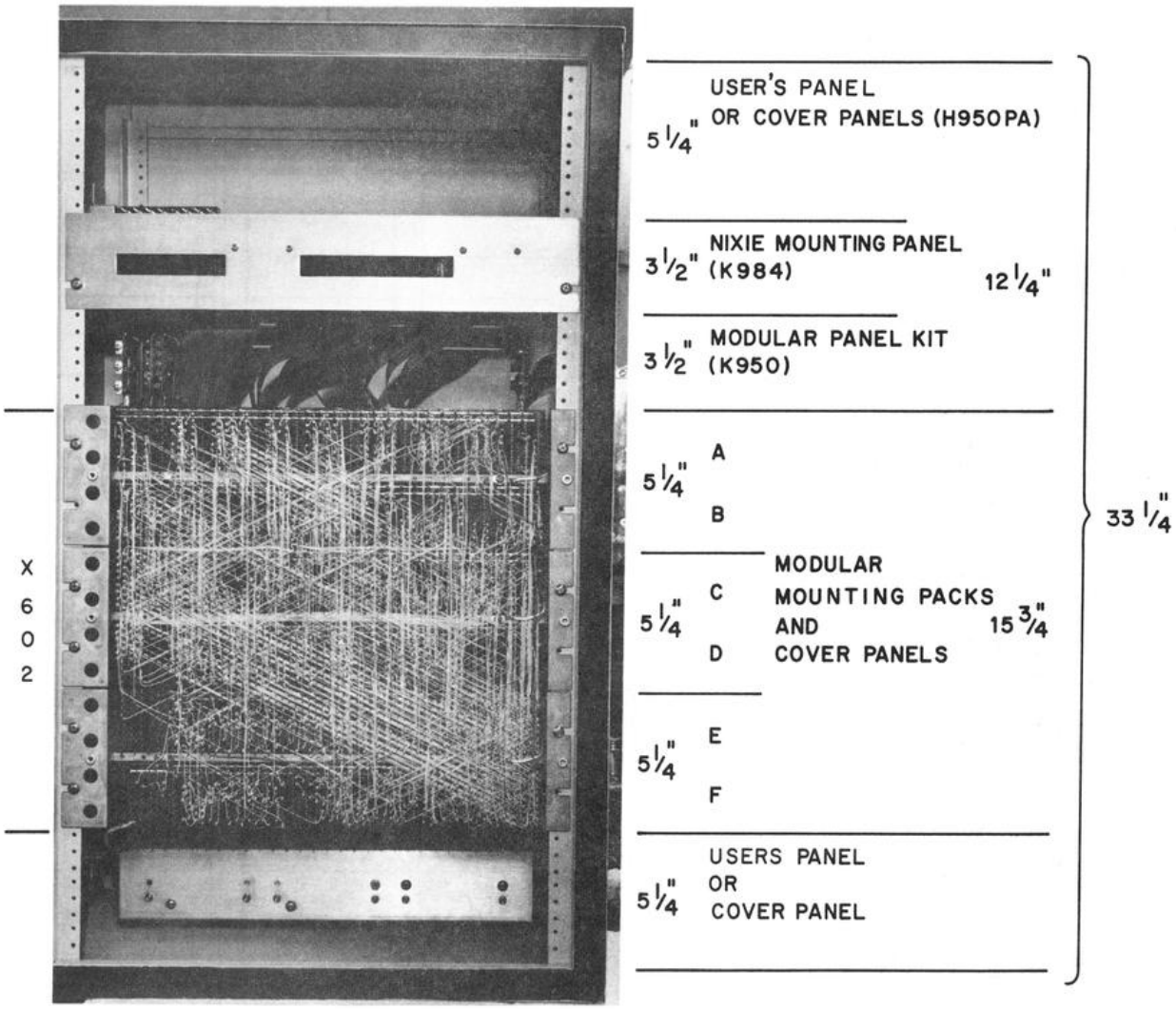


Figure 2-4 Panel Locations - H953A Cabinet

2.2 WIRE WRAPPING

NOTE

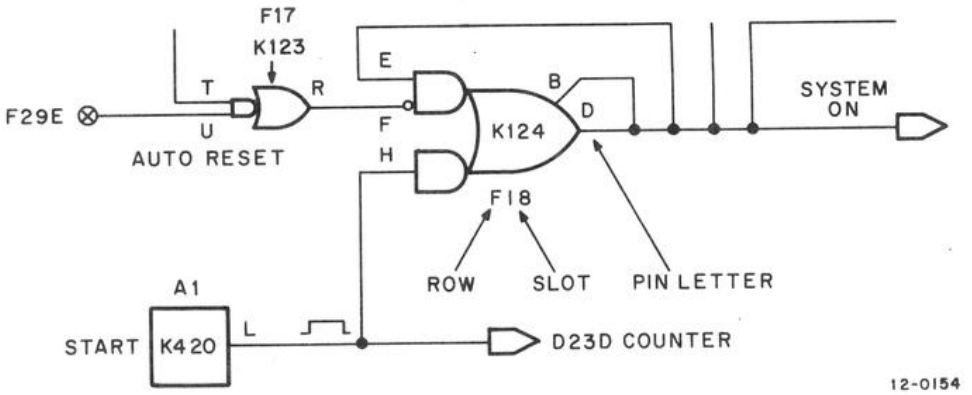
Turn to the appendices, and read the material on wire-wrapping techniques.

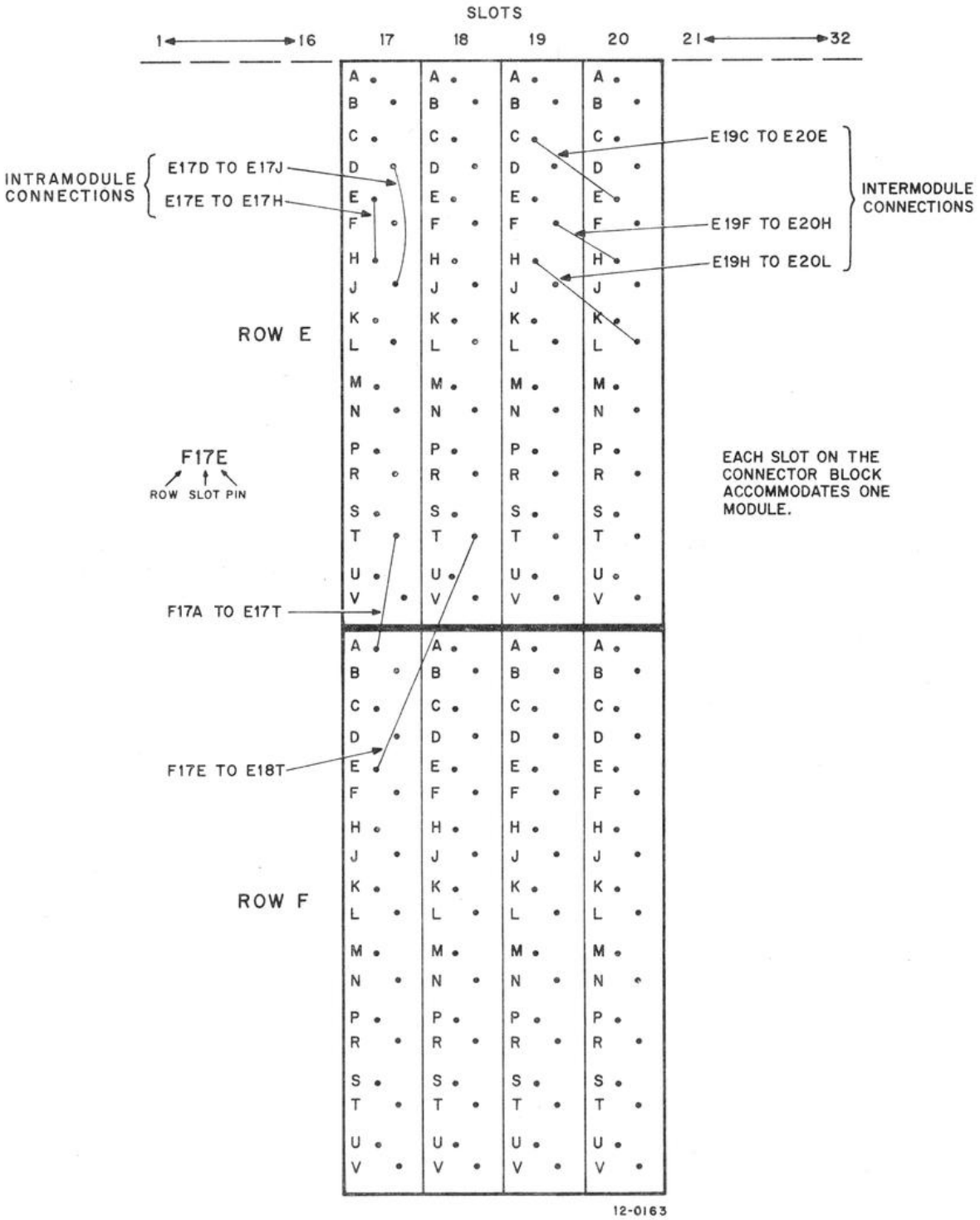
The LAB-K logic is interconnected by plugging module boards into the modular mounting rack. This rack must be wired to facilitate these connections.

The printed circuit connections on a module board are terminated at gold-plated contacts, located on the etched side of the board. The latter contacts are identified by letters that are identical to the pin letters on a H800 or H808 connector block (contact A connects to pin A, etc.). These letters are used on the LAB-K schematic drawings to identify logic connection points, which are made on the module rack connector blocks.

The module rack location (row and slot) is identified by an alphanumeric designation that is usually located adjacent to the pertinent schematic logic symbol. For example, the K124 Module schematic symbol is found in the lower left-hand corner (see illustration below) of schematic drawing X602-0-5; and F18 is written adjacent to it. This shows that the K124 Module is plugged into slot 18 of row F. The letters located at the wiring points of the K124 identify the pin connections made at slot 18 of row F. F18B, for example, is connected to F18D. Both pins are located in slot 18 of row F; that is, on the same module board. Thus, the latter connection is called an **intramodule** connection.

F18D, however, is also connected to pins located in other rows or slots, such as F17N, F17H, D12U, and E5F. The latter type of connection is called an **intermodule** connection; that is, the pin connections are located on more then one module board. (See Figures 2-5 and 2-6).

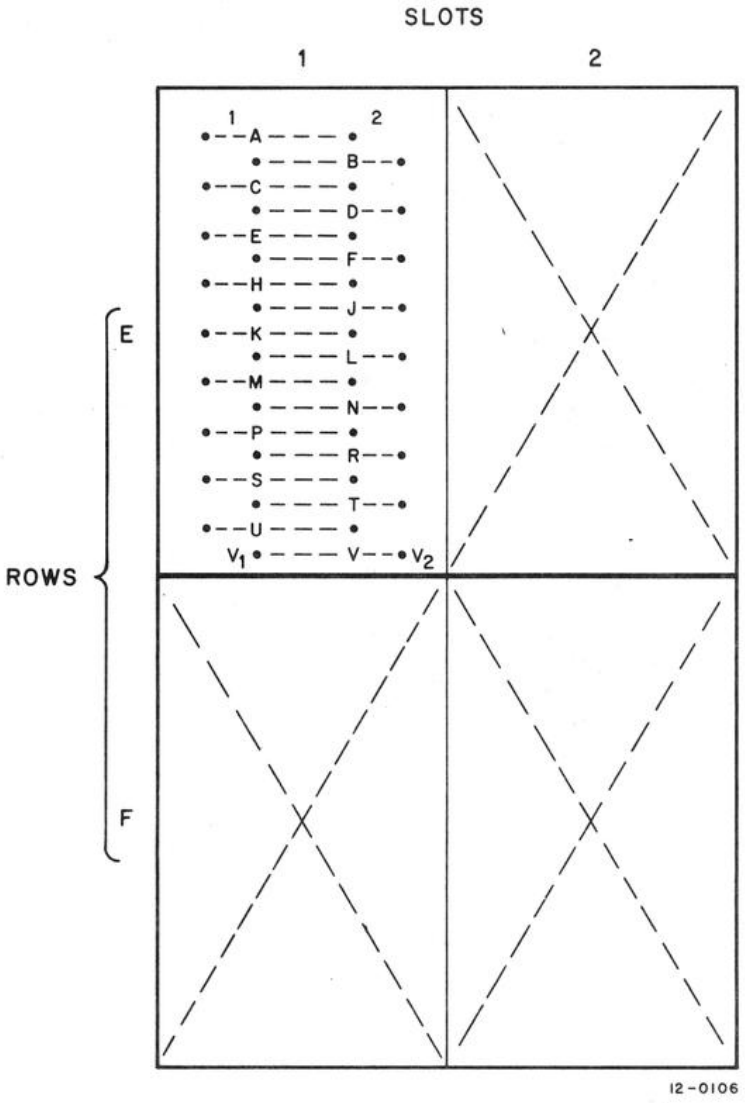




NOTE

These are not actual wiring points.

Figure 2-5 H800 Connector Block

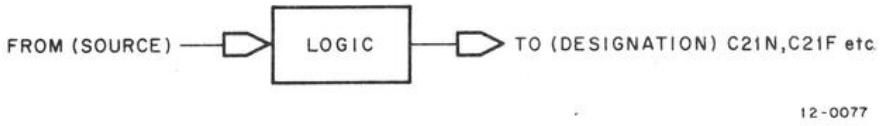


NOTE

The row 1 pin is located to the left of a letter, and a row 2 pin is located to the right of a letter (see pin V above).

Figure 2-6 H808 Connector Block

The logic connection points for a module are usually found on one drawing. To determine connection points, simply trace the logic's output line to the logic to which it is connected. Some logic, however, is connected to logic that is schematically represented on another drawing. For example, F17 (RIGHT RESP) is connected to B16L, B25T, C21N, and C21F, all of which are represented on other drawings. This situation is represented by a special schematic symbol, shown below.



The destination (or source) of an extraneous logic signal is indicated by an application name, such as down counter, and by an alphanumeric designation. When the alphanumeric designation is not prefixed by the application name, the source or designation is determined by referring to the Module Utilization drawing (see Figure 2-7). For example, to determine the destination of B16N, look at row B, slot 16, on the Module Utilization drawing, which is application M (VI/VR) - the logic gate is K028.

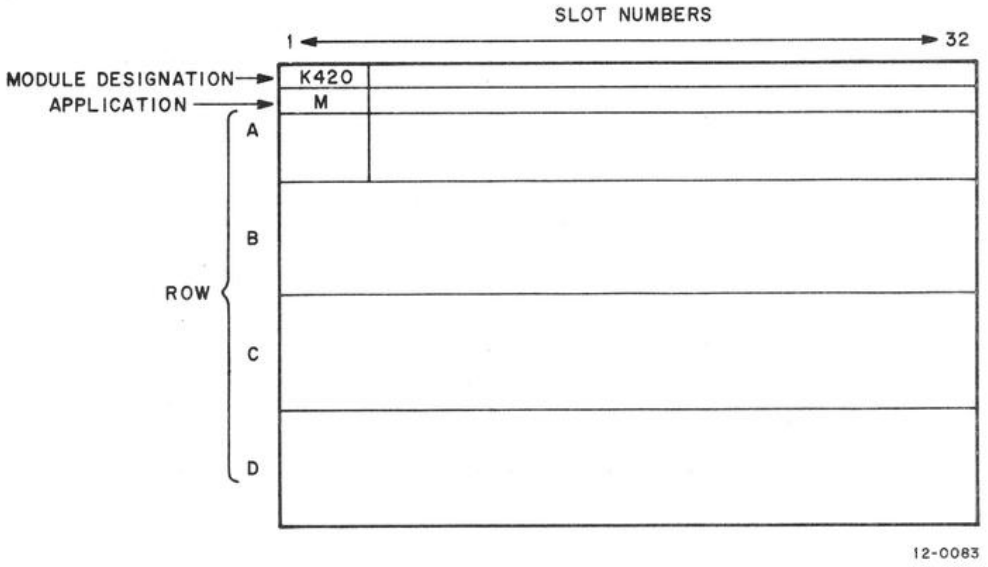


Figure 2-7 Module Utilization Drawing - Key

When making the wire-wrapped connections, each connection that is made must be documented in the form of a wiring list. This list is necessary to ensure that all necessary connections have been made after an application has been wired.

The following is the wiring list for Application A (Input Logic), represented on schematic drawing X602-0-5.

Application A Wiring List

From	To	From	To
F14D	F15E	F17D (Left Event)	C21L (Down Counter)
F15F	F16F		C21J (Down Counter)
F16H	F16D		B25R (Down Counter)
F16J	A22P	F17K (Right Event)	C21N (Down Counter)
F16E	F17F		C21F (Down Counter)
F14F	F15K		B25T (Down Counter)
F15L	F16M	A01D (MASTER RESET)	C06K (Sequencer)
F16N	F16K	A01D (MASTER RESET)	F17T (Auto Reset)
F16P	A22U	A01D	E5U (Timing Kit L)
F16L	F17M	A01D	E5 (Timing Kit L)
F17R	F18F	A01D	C22T (Sequencer)
A1L	F18H	A01D	C06K (Sequencer)
F18E	F18D	A01D	C29J (Down Counter)
F18B	F18D	A01D	C28J (Down Counter)
F18D (System On)	F17N		C27J (Down Counter)
F18D	F17H	A01E (MASTER RESET)	D23K (Down Counter)
F18D	E5J (Timing Kit L)	A01E (MASTER RESET)	E4T (Up Counter)
F18D	C23M (Sequencer)	A01E (MASTER RESET)	D14N (Output Logic)
F18D	A02L (Sequencer)	A1L (Start)	D23D (Down Counter)
F18D	D07F (Sequencer)		

NOTE

Multiple connections are series connected. For example, F18D would be connected as follows:

F18D to F17N
F17N to F17H
F17H to D12U

No more than two wrappings should be made on any terminal post.

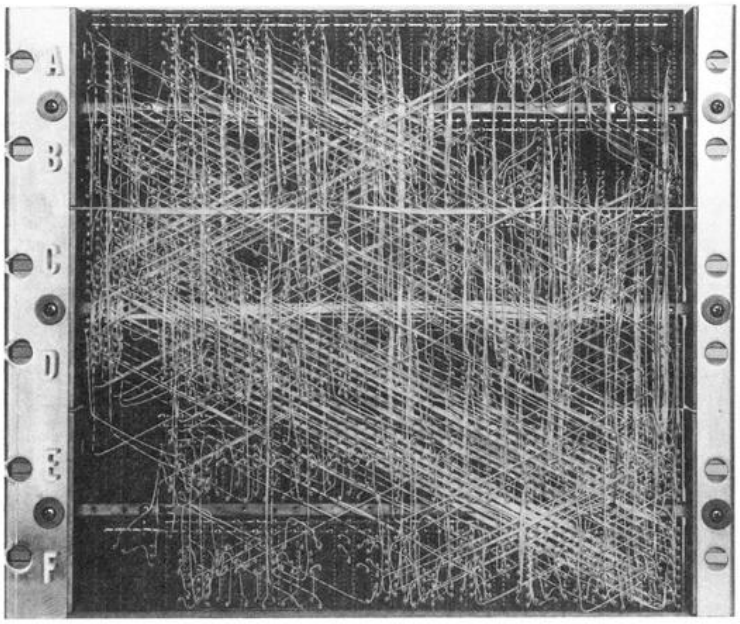
If any of the LAB-K options are to be used, additional wiring is necessary for Application A, as follows:

From	To
F18D (System On)	D12U (Timing Kit L)
F18D	B4F (Session Timer)
F17K (Right Event)	B16L (VR Programmer)
F17D (Left Event)	B16J (VR Programmer)
A01D (MASTER RESET)	B5K (Session Timer)
A01D	B6K (Session Timer)
A01D	B2T (Session Timer)
A01D	B2N (IRT Distributor)
A01E (MASTER RESET)	E4M (VI/VR Programmer)
A01E	E4F (VI/VR Programmer)
A01E	E28F (Second VI/VR Programmer)
A01E	F20J (Second VI/VR Programmer)

Each application that you intend to use is wired in the same fashion.

NOTE

If you do not wish to assemble and wire the mounting panel, then you may purchase Option R – the X602 Automatic Wire Frame (Figure 2-8). The frame is wired to the maximum logic configuration, which accommodates all the LAB-K options. The only wiring that is necessary involves connecting the X602 to the power supply (Steps 3a through 3c of Section 2.1).



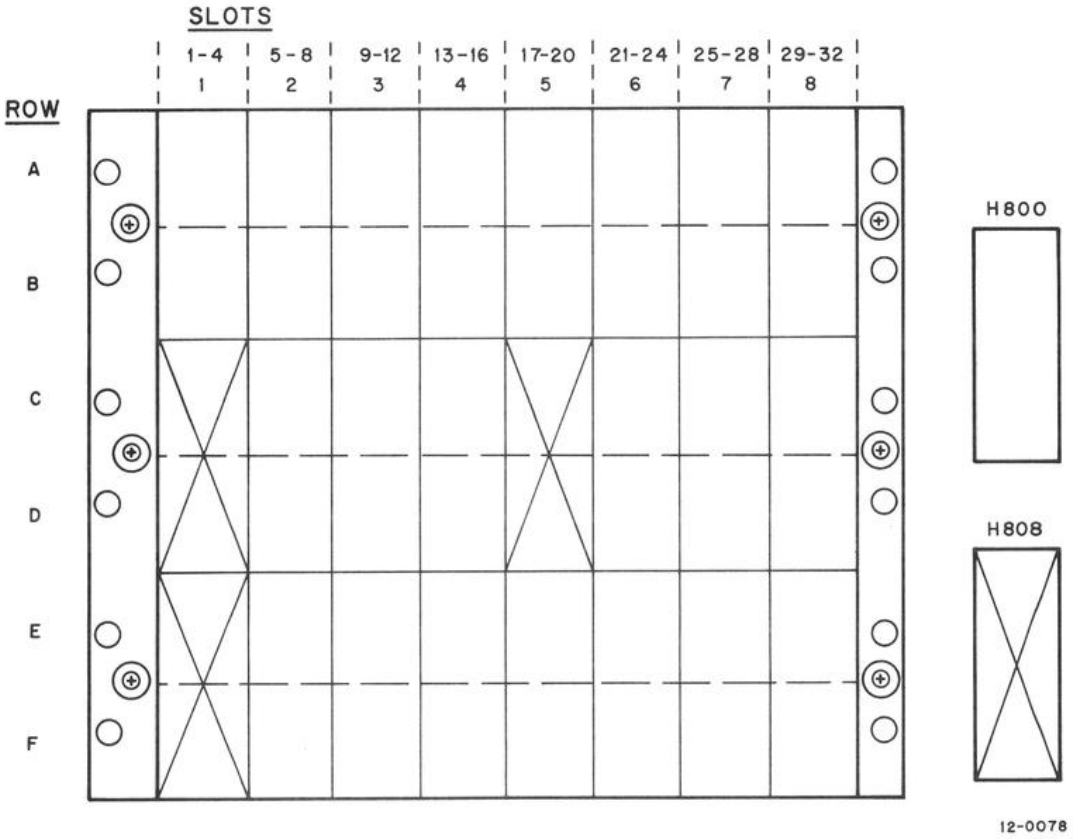


Figure 2-8 X602 Prewired Module Rack

2.3 ASSEMBLY AND MOUNTING OF POWER SUPPLY

NOTE

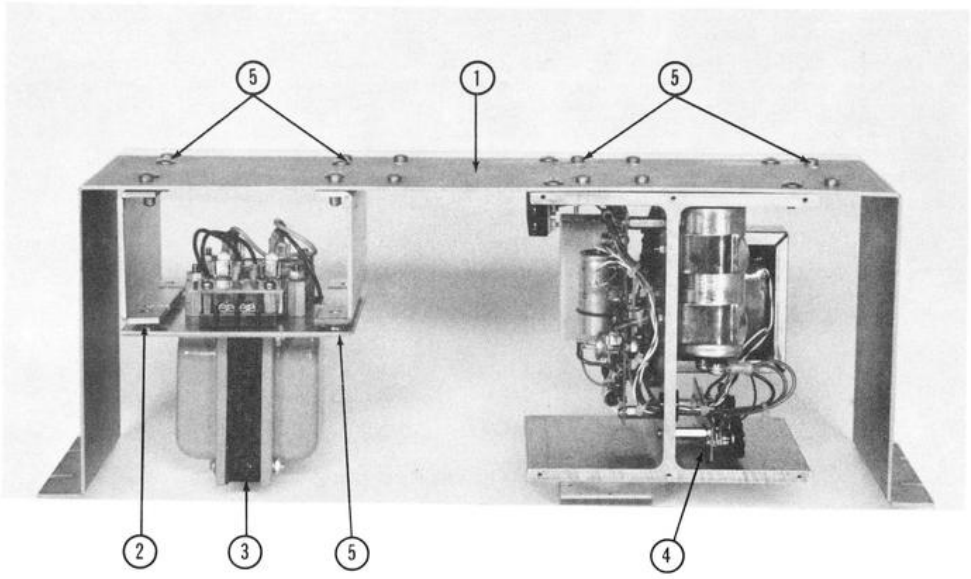
If the X602 Mounting Panel (Option R) is being used, make the power supply connections (Section 2.1, Steps 3a through 3c), and mount the panel at the location shown in Figures 2-4 and 2-11.

Assemble and mount the power supply (see Figure 2-9) as follows:

Step	Procedure
1	Mount the 714 Power Supply to the K984 Mounting Panel (see Figure 2-10).
2	Mount the H002 Mounting Brackets to the K984 Mounting Panel (see Figure 2-10).
3	Mount the assembled Power Supply on the H953A cabinet, as shown in Figure 2-11.

NOTE

Place the transformer near the H002 Mounting Brackets, but do not mount until the wiring connections in Section 2.6, Step 3, are made.



INDEX	NOMENCLATURE
1	K982 MOUNTING PANEL
2	H002 MOUNTING BRACKETS
3	K743 VOLTAGE TRANSFORMER
4	714 7 AMP 5VDC POWER SUPPLY
5	MOUNTING HARDWARE (16) 10-32X $\frac{1}{2}$ LG

Figure 2-9 Power Supply Assembly

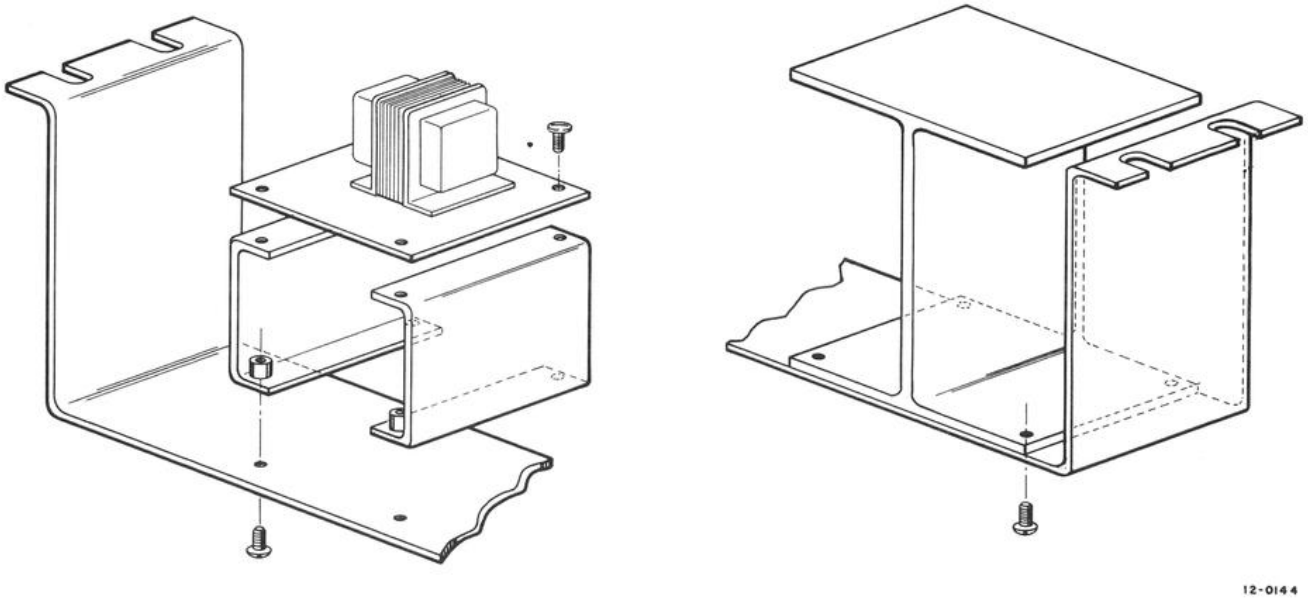


Figure 2-10 Power Supply – Exploded View

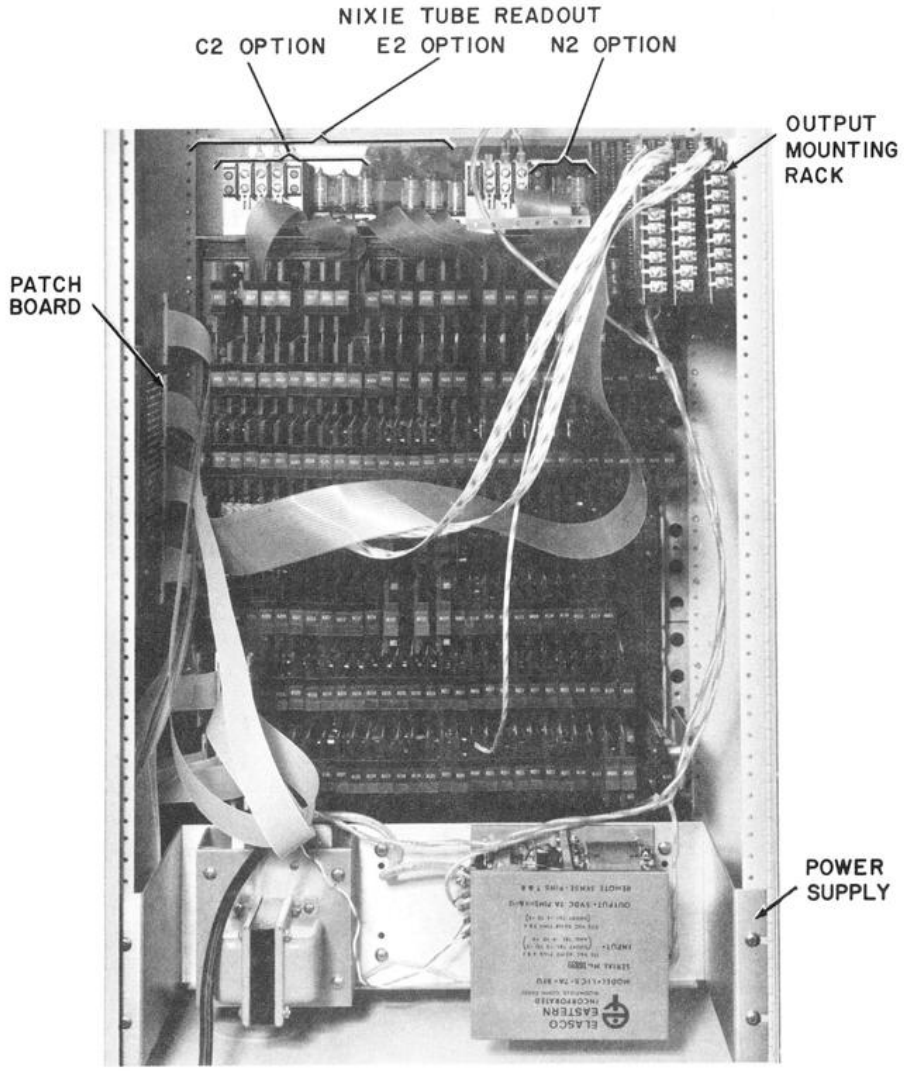


Figure 2-11 LAB-K Rear View

2.4 ASSEMBLY AND MOUNTING OF THE C2, E1, N1, and N3 OPTIONS

2.4.1 C2 Option

Assemble and mount the Down Counter Nixie Readout Option (C2 Option) (see Figure 2-12), as follows:

Step	Procedure
1	Mount three K671 Display Tubes to the K771 Power Supply, as shown in Figure 2-13. The display tubes are stacked to the left; the first board is attached to the K771, and the second tube board attaches to the first, etc., as shown in Figure 2-13.
2	Prepare the K984 Mounting Panel plexiglas backing, as shown in Figure 2-14. If you are planning to use the N1 or N2 Option, Session Counters, two pieces of plexiglas should be prepared.
	NOTE If you plan to use the Up Counter Readout Option, (Option E2), refer to Paragraph 2.4.2, Step 3.
3	Mount the nixie unit to the K984 Mounting Panel. Mount the assembled unit to the H953A Cabinet at the location shown in Figure 2-15.
4	Plug the nixie module boards into the slot positions referenced in Figure 2-16.

2.4.2 E2 Option

Assemble and mount the Up Counter Readout Option (E2 Option), as follows:

Step	Procedure
1	If this option is being used without the C2 Option, it is assembled and mounted in exactly the same manner as the Down Counter Readout.
2	Plug the nixie module boards into the slot positions referenced in Figure 2-16.
3	If both the Down Counter and the Up Counter are going to be used, add three K671 Nixie Boards to the Down Counter assembly, as shown in Figure 2-16. Jumper the power by wiring at Location A, Figure 2-16, and plug the module boards into the slot positions referenced in Figure 2-16.

2.4.3 N1 Option

Mount the N1 Option, (9 hour 59 min. Session Counter), as shown in Figure 2-17.

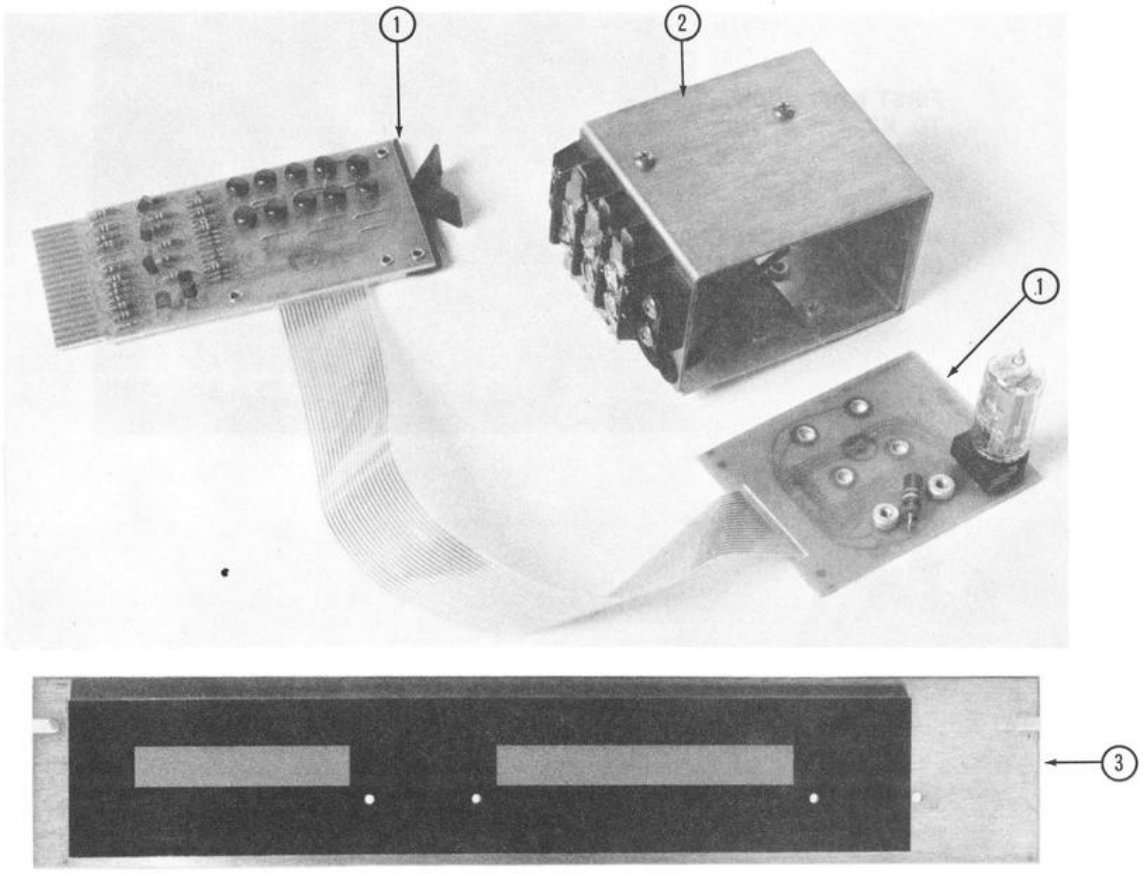
2.4.4 N2 Option

Assemble and mount the N2 Option (99 hour 59 min. Session Counter) as follows:

Step	Procedure
1	The N2 option is mounted as shown in Figure 2-17.
2	Run a jumper wire between circuit boards 3 and 4 (see Figure 2-18).

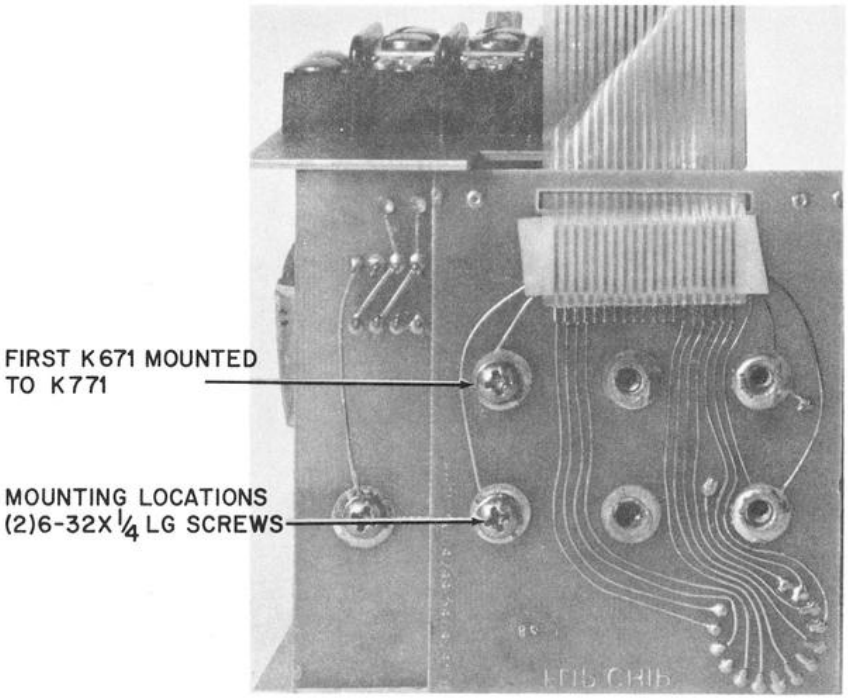
2.4.5 C2, E2, and N2 to K994

Mount the C2, E2, and N2 options to the K984 Mounting Panel, as shown in Figure 2-18.



INDEX	NOMENCLATURE
1	K671 DECIMAL DECODER & NIXIE® DISPLAY
2	K771 DECIMAL SUPPLY
3	K984 MOUNTING PANEL

Figure 2-12 Nixie Tube Readout



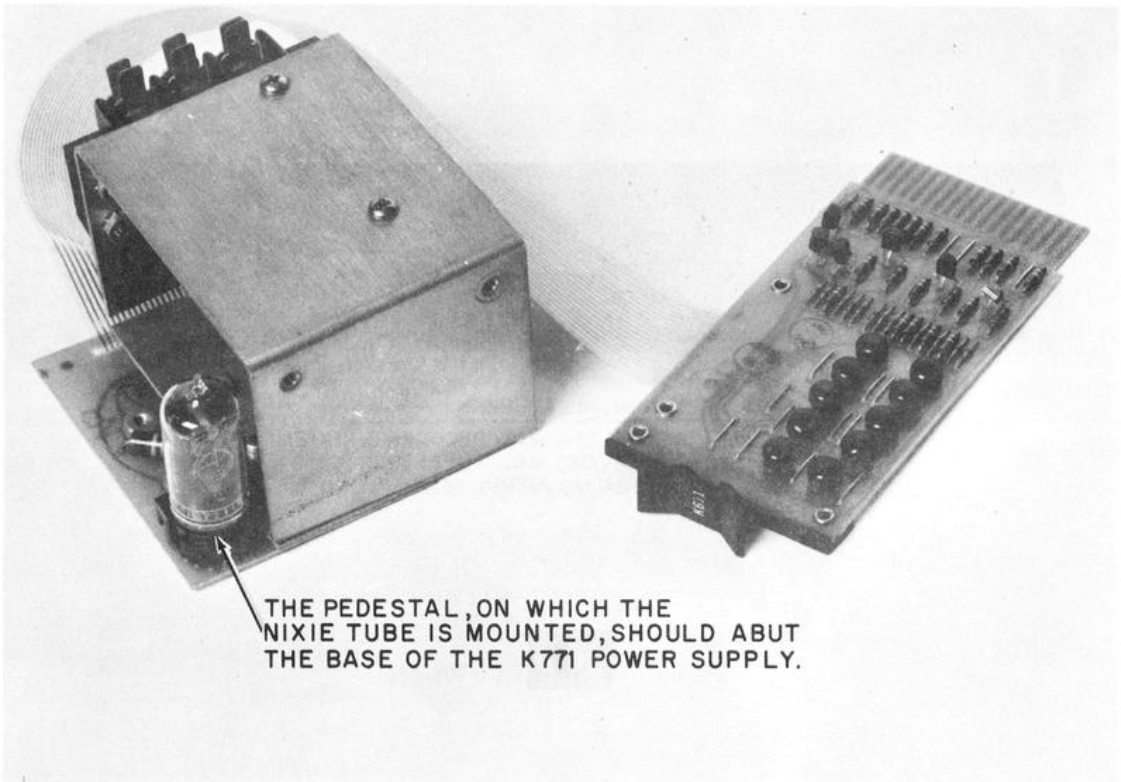
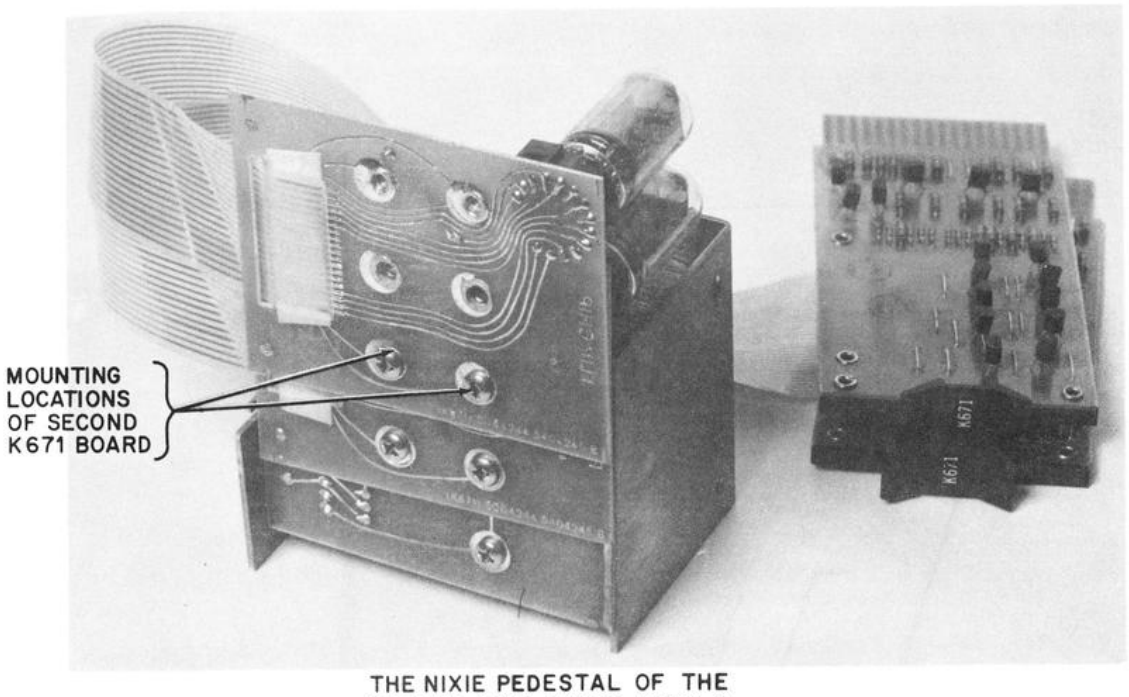
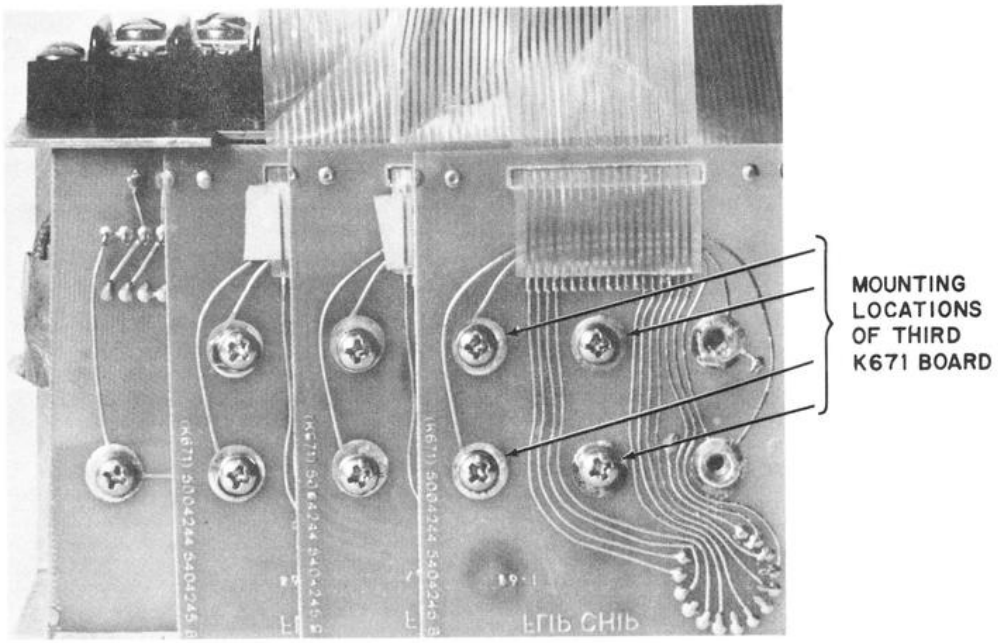


Figure 2-13 (Sheet 1) C2 Option – Mounting Instructions



THE NIXIE PEDESTAL OF THE SECOND K671 BOARD SHOULD ABUT THE EDGE OF THE FIRST K671 BOARD (SEE FIGURE 2-15)



PEDESTAL OF THIRD K671 SHOULD ABUT SECOND K671

Figure 2-13 (Sheet 2) C2 Option – Mounting Instructions

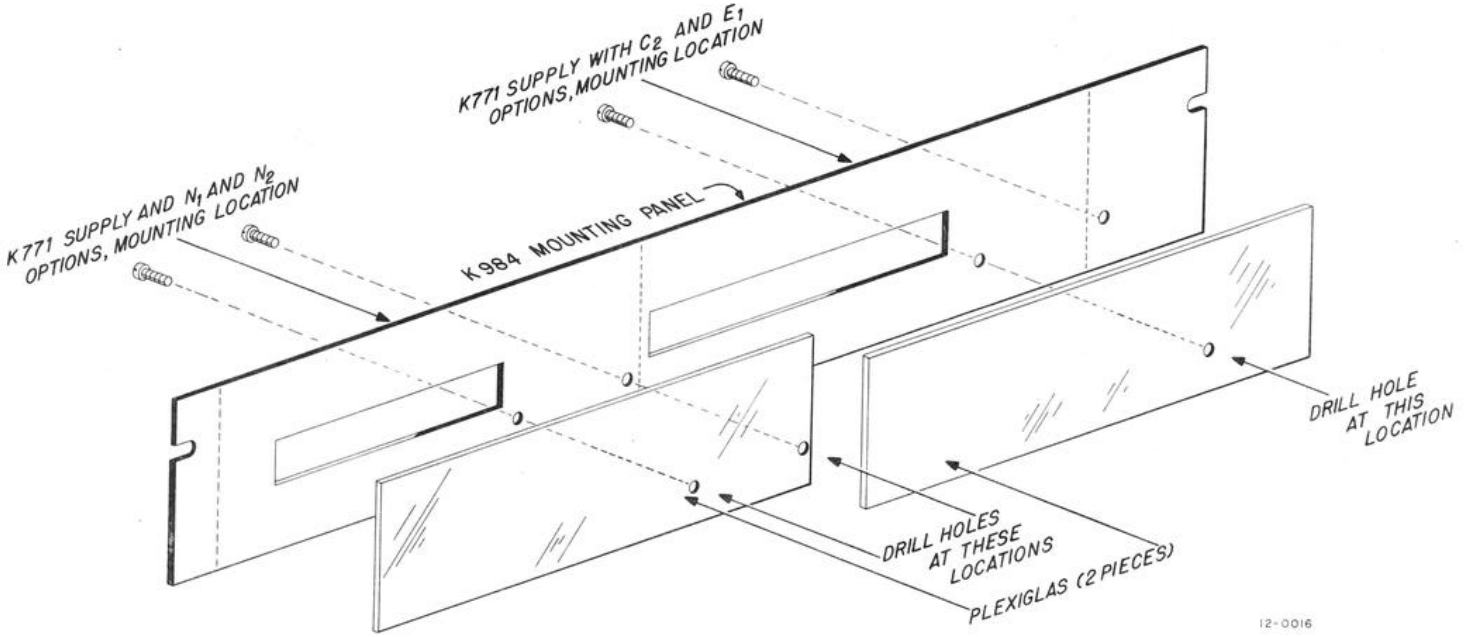


Figure 2-14 Mounting Panel, Plexiglas – Assembly Drawing

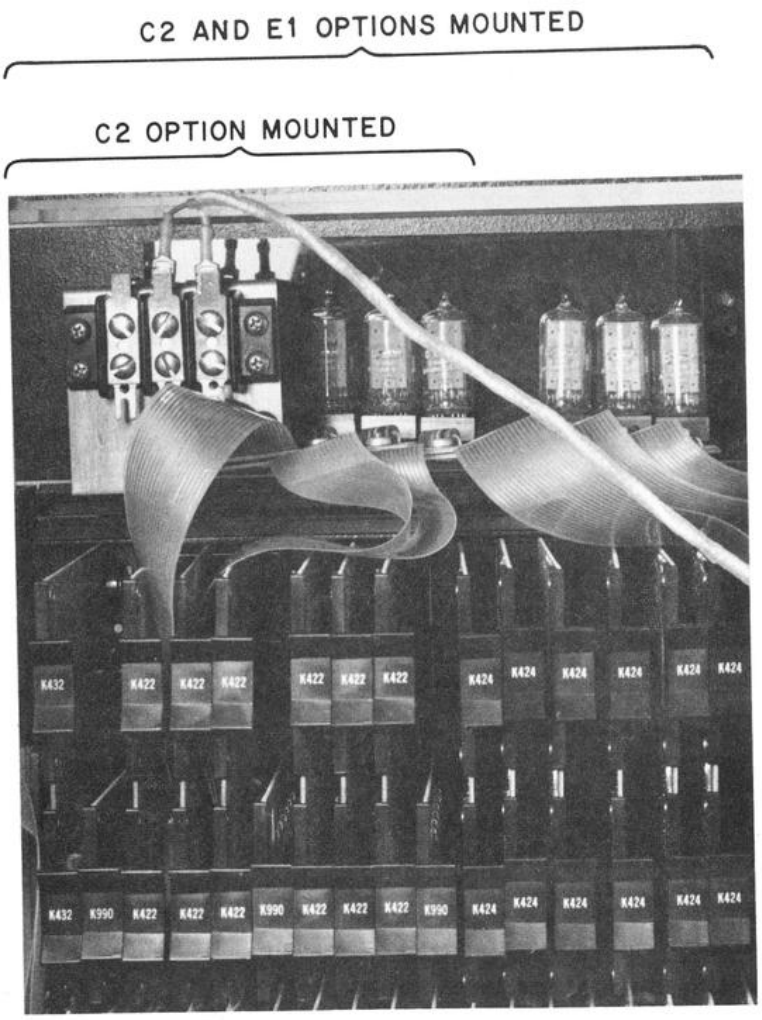
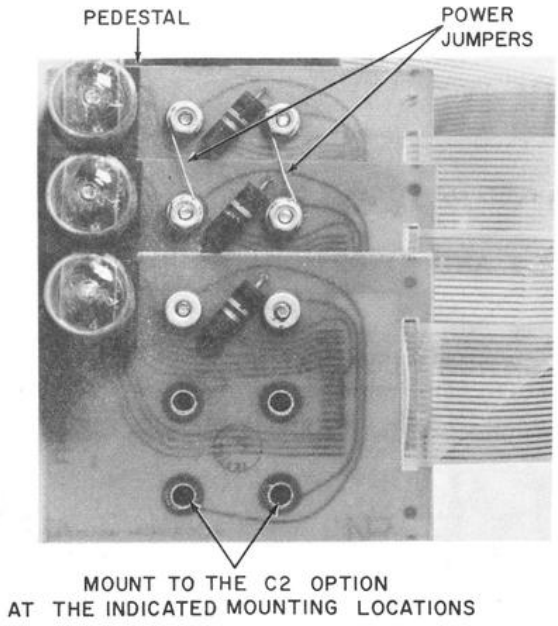


Figure 2-15 C2, E1 Options – Mounting Locations



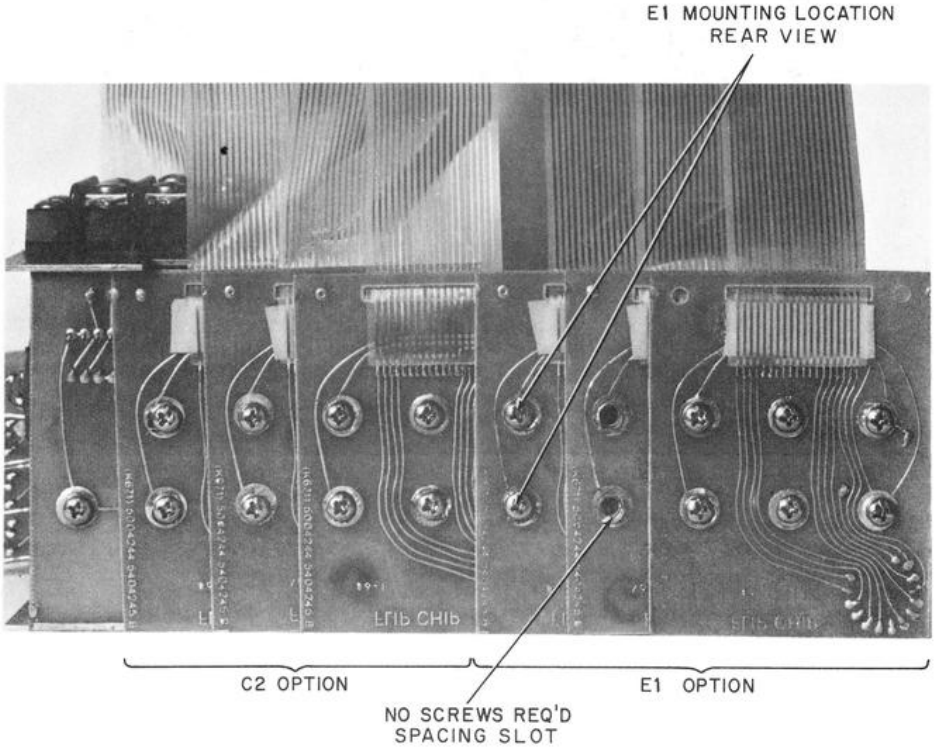


Figure 2-16 (Sheet 1) C2, E1 Options – Assembly Instructions

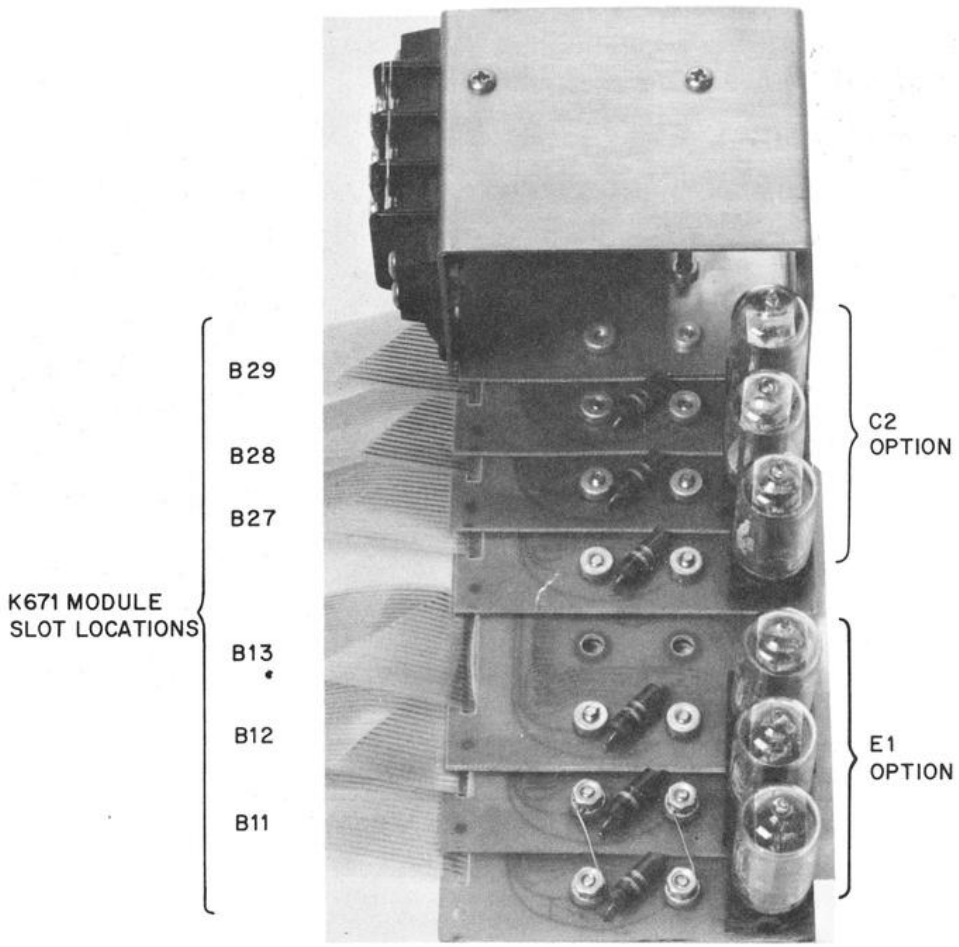


Figure 2-16 (Sheet 2) C2, E1 Options – Assembly Instructions

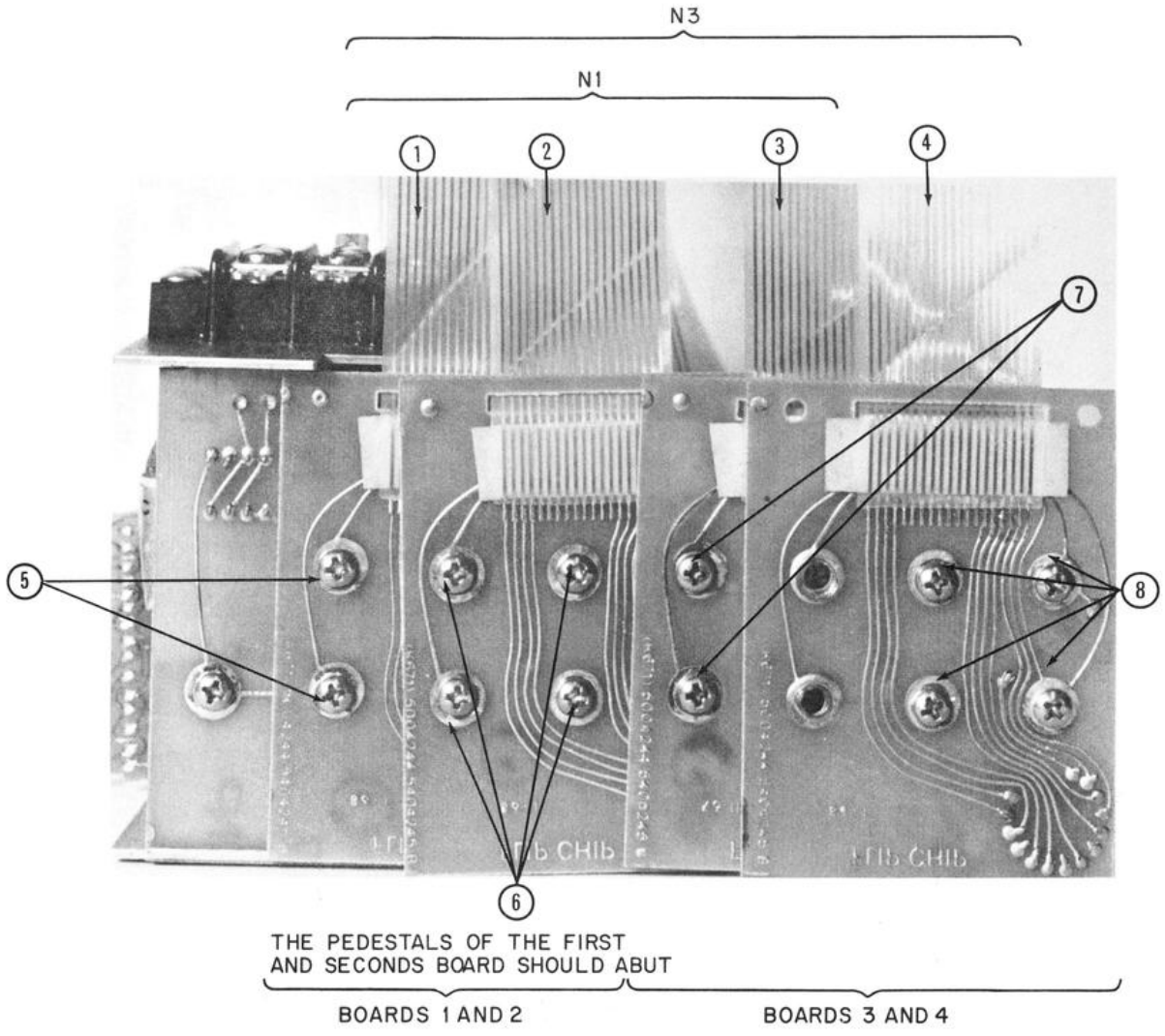


Figure 2-17 N1, N3 Options – Assembly Instructions

INDEX

K671 module slot locations

1. B8
2. B7
3. B10
4. B9
5. Mounting locations of Board 1 (The nixie pedestal should abut the base of the K771 Power Supply.)
6. Mounting location of Board 2 (The pedestals of the first and second boards should abut.)
7. Mounting location of Board 3 (mounted to Board 2).
8. Mounting location of Board 4 (mounted to Board 3).

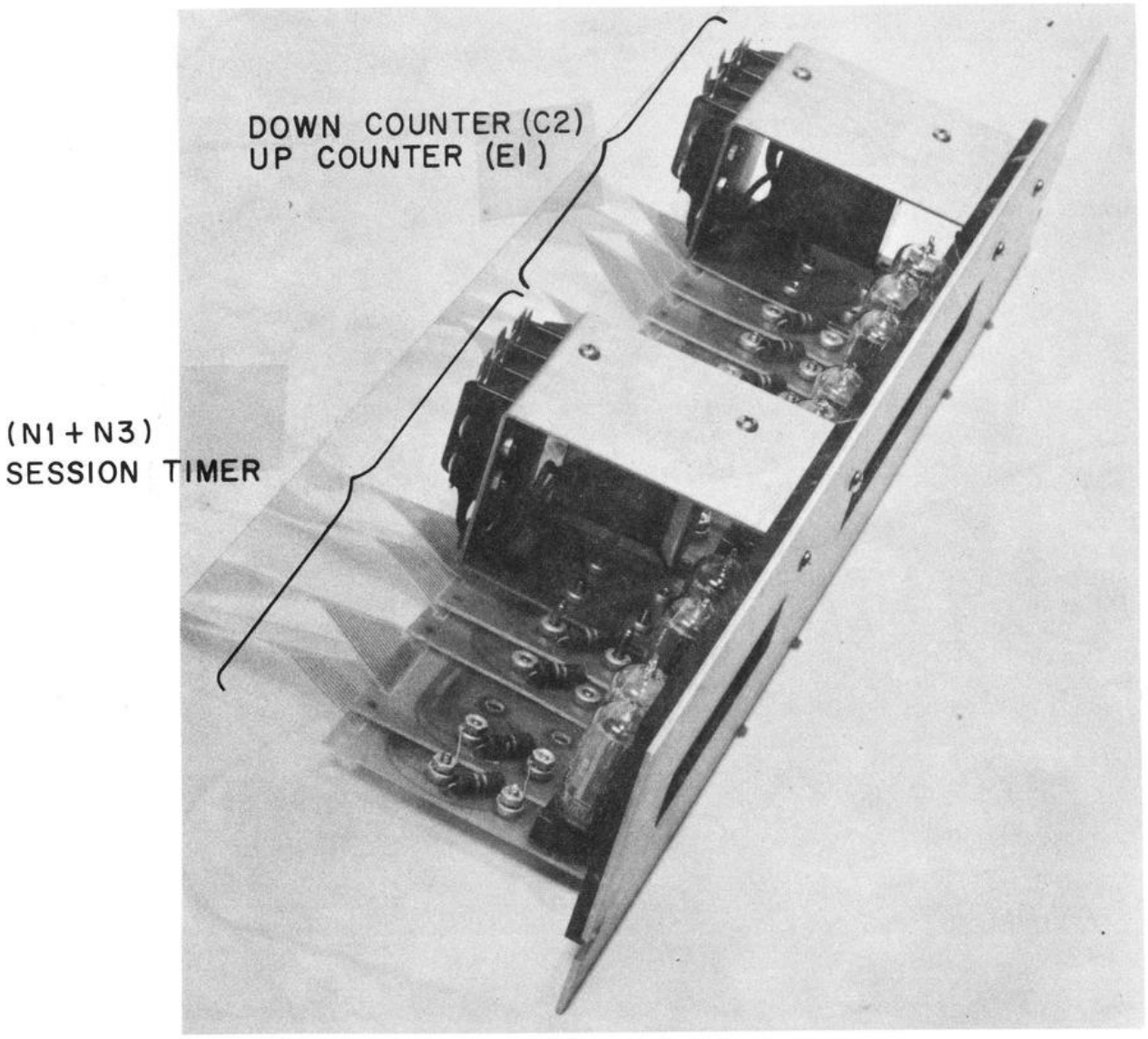


Figure 2-18 C2, E1, and N3 Options – Mounting Locations

2.5 MOUNTING AND WIRING OF SEQUENCER INDICATOR LIGHTS (K410) – OPTION B1

Mount and wire the indicator lights as follows:

Step	Procedure
1	Plug two K410 Modules into slots A2 and A3.
2	Prepare the following lengths of hook-up wire: 32 in. white 4 in. white 32 in. red 4 in. red
3	Strip the four pieces of wire, and connect a spade-lug to both ends of each wire.
4	Make a twisted-pair out of the 32 in. red and white wires. (Leave approximately 2 in. untwisted at each end.) Wrap the twisted pair in spaghetti.
5	Refer to Figure 2-19 for the following steps: Connect 4 in. red between 2 and 3 Connect 4 in. white between 5 and 8 Connect 32 in. red to 4 Connect 32 in. white to 7
6	Refer to Figure 2-21 for the following steps: Connect 32 in. red wire to K743 wiring point B (green wire) Connect 32 in. white wire to K743 wiring point E (green wire)

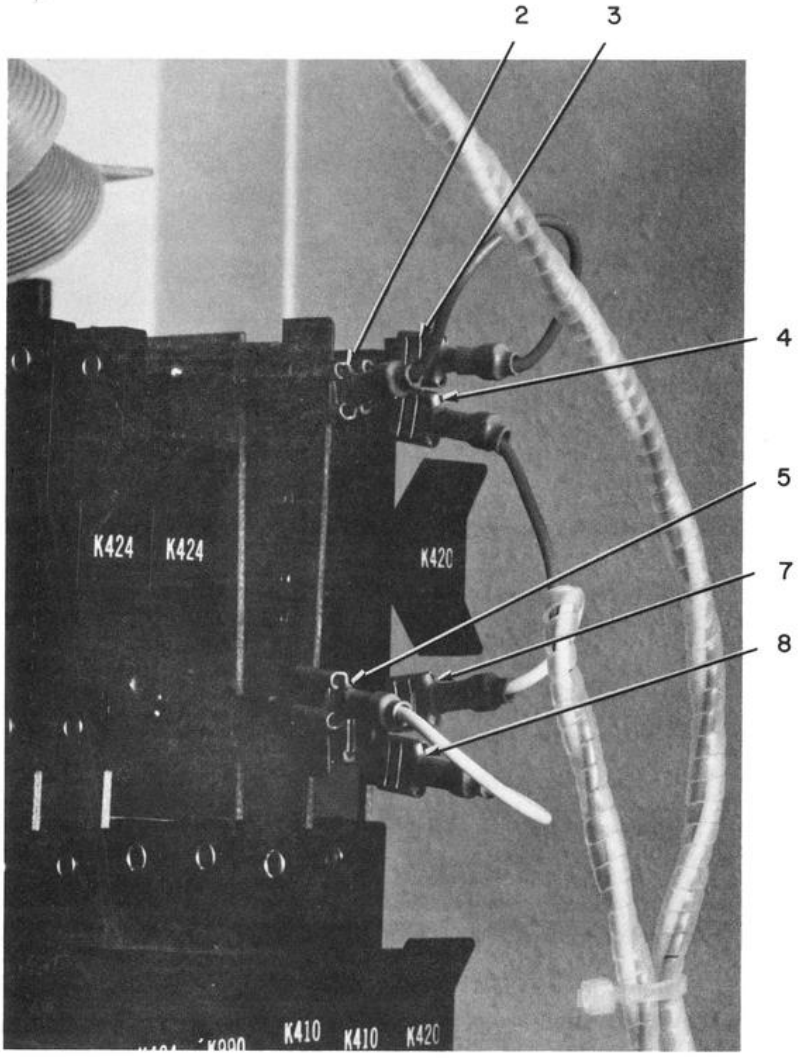


Figure 2-19 K410 Indicator Lights – Wiring Guide

2.6 CONNECTING AND MOUNTING THE 743 TRANSFORMER

Connect and mount the 743 Transformer as follows:

Step	Procedure
1	Remove the terminal cover (see Figure 2-20), and loosen the clamp terminal screws.
2	Prepare the following wire, and mount a ring connector on one end of each 20 in. wire and a spade-lug on one end of each 36 in. wire. 20 in. black — 36 in. black 20 in. white — 36 in. white
3	Refer to Figure 2-21 for the following steps: ( ) Connect a standard three-prong ac power cord to the transformer by connecting the white wire to I, the black wire to G, and the green wire to A. ( ) Connect the bare-wire end of the 20 in. black to H. ( ) Connect the bare-wire end of the 20 in. white to F. **NOTE** The ring end of the 20 in. hook-up wires is connected to the power supply under Section 2.7, Step 5. ( ) Tighten the clamp terminal screws. ( ) Make a twisted pair of 36 in. black and white wires. (Leave approximately 2 in. untwisted at each end.) Wrap the twisted portion in spaghetti. ( ) Connect the spade-lug end of the 36 in. black to C (terminal with existing green wire). ( ) Connect the spade-lug end of the 36 in. white to D (terminal with existing green wire). *( ) Connect the bare-wire end of the 36 in. black to pin V, slot 2, row F. Solder in place. *( ) Connect the bare-wire end of the 36 in. white to pin U, slot 2, row F. Solder in place. ***NOTE** Bring the twisted pair out to the front of the module rack by slipping the wire between the connector block and the module mounting bar. This is an indirect ac power connection to the power module (K731) used in location F02U.
4	Replace clamp terminal cover.
5	Mount the transformer to the H002 brackets as shown in Figure 2-10.

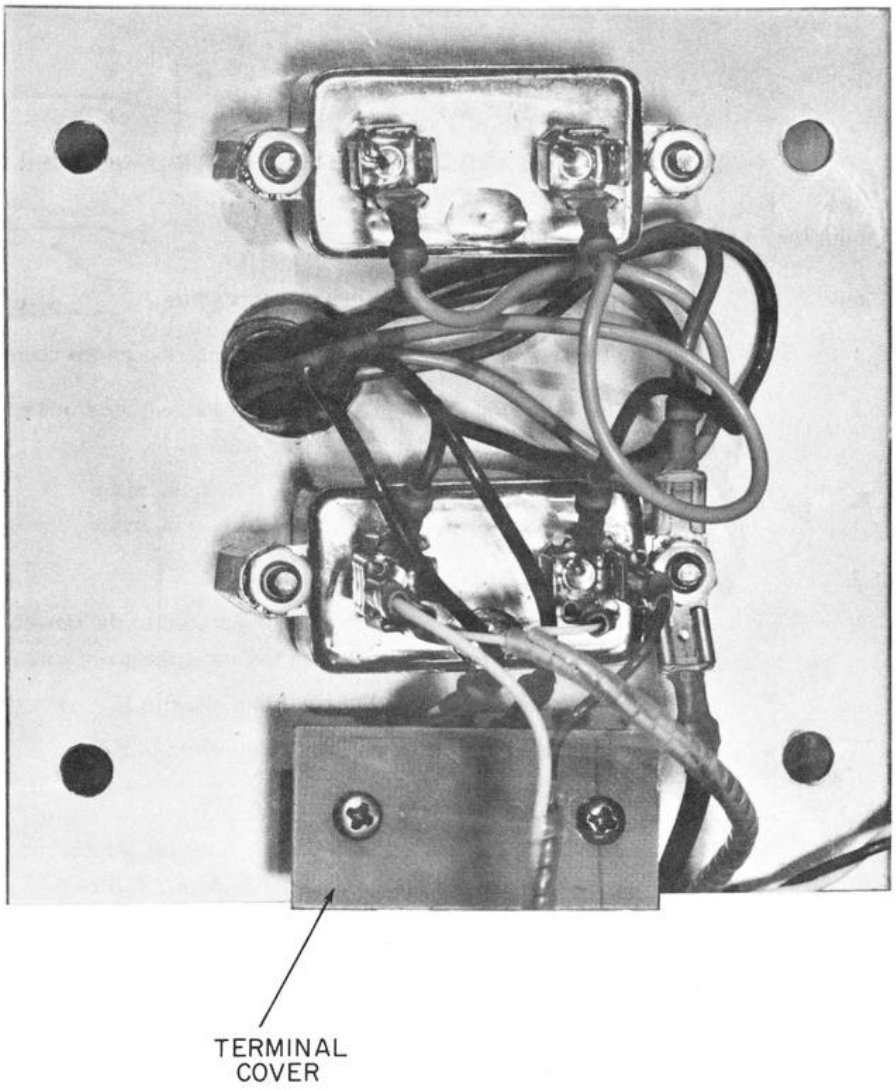


Figure 2-20 K743 Transformer – Terminal Cover Location

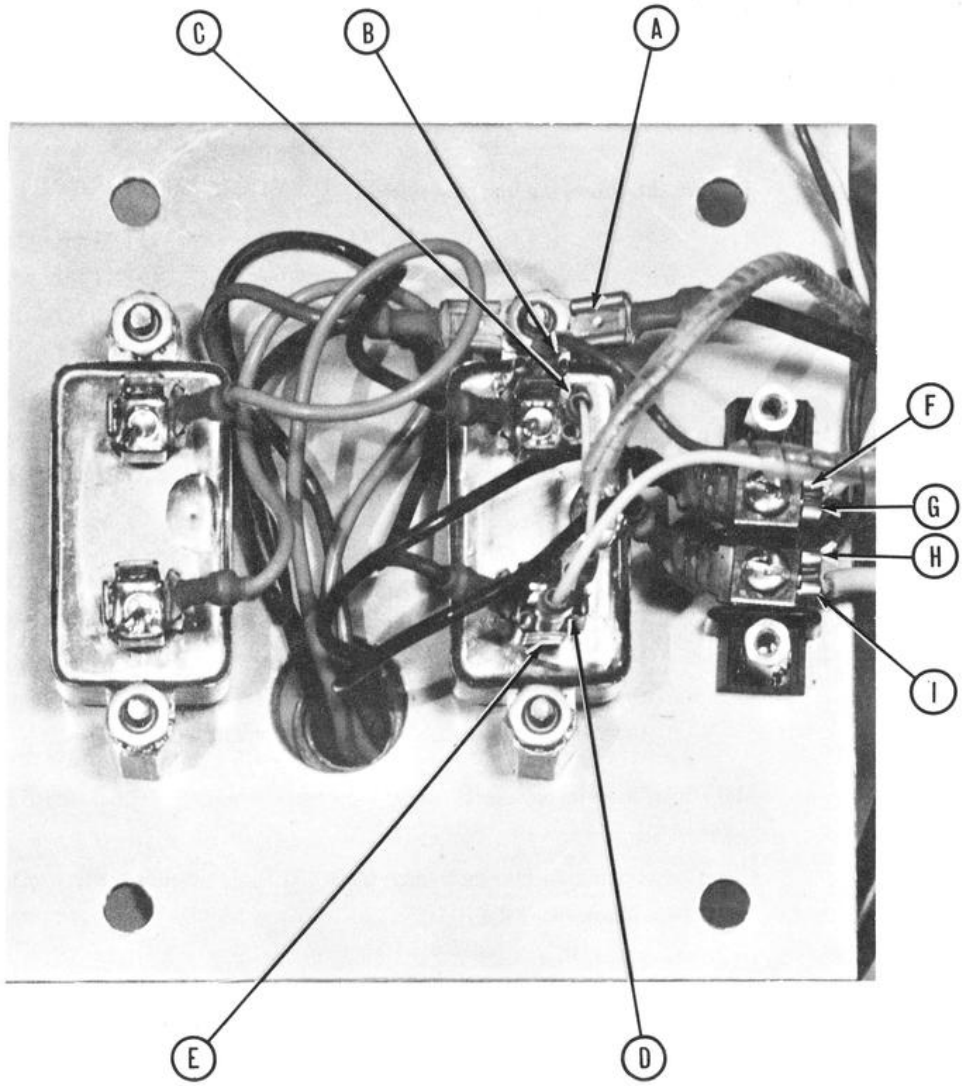


Figure 2-21 Transformer Wiring Points

2.7 CONNECTING NIXIE TUBES, MODULES, AND TRANSFORMER TO THE POWER SUPPLY

Connect nixie tubes, modules, and transformer to the power supply, as follows:

Step	Procedure
1	Prepare the following hook-up wire: (1) 44 in. black (1) 18 in. black (1) 44 in. white (1) 18 in. white
2	Mount Hardware – Mount spade-lugs on one 44 in. black and 44 in. white wires, and ring connectors on the opposite end.
3	Make twisted pairs out of the 44 in. black and white wires, and also the 18 in. black and white wires. (Leave about 2 in. uncovered at each end.) Wrap the twisted portion in spaghetti.
4	Connect the K771 Power Supply as follows: ( ) a. If there is one K771 supply, connect the 44 in. twisted-pair as shown in Figure 2-22 ( ) b. If there are two K771 supplies, connect the 18-in. white connector at A and C and the 18 in. black at B and D, as shown in Figure 2-23 and connect spade-lug end of the 44 in. black to E and 44 in. white to F (Figure 2-23).
5	Make the following connections on the Power Supply Terminal Board (TB). Refer to Figure 2-24. ( ) Connect the 44 in. black from the K771 nixie supply to TB 5. Also, connect a 6 in. black jumper to TB 5. **NOTE** In order to fit both connectors on the same terminal, the arm of the top ring connector must be bent. ( ) Connect a 6 in. black jumper from TB5 to TB 3. Also, connect the 20 in. black from point H on the K743 Transformer (Figure 2-21) to TB 3. ( ) Connect the 44 in. white from the K771 nixie supply to TB 6. Also, connect a 6 in. white jumper to TB 6. ( ) Connect a 6 in. white jumper from TB 4 to TB 6. Also, connect the 20 in. white from point F on the K743 Transformer (Figure 2-21) to TB 4. ( ) Connect a 6 in. white jumper from TB 7 to TB 8. ( ) Connect the three black wires (ground) coming from the Module Mounting racks (racks 1-3) to TB 2 (Section I, Step C, etc.). ( ) Connect the three orange wires (+5V) coming from the Module Mounting racks to TB 1.

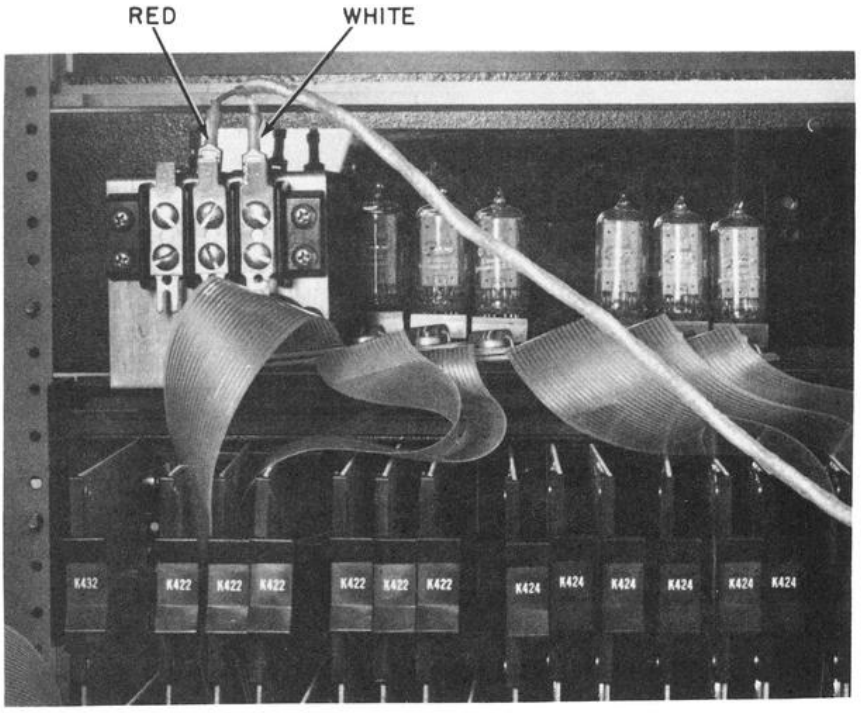


Figure 2-22 K771 Power Supply – Wiring Guide (One K771)

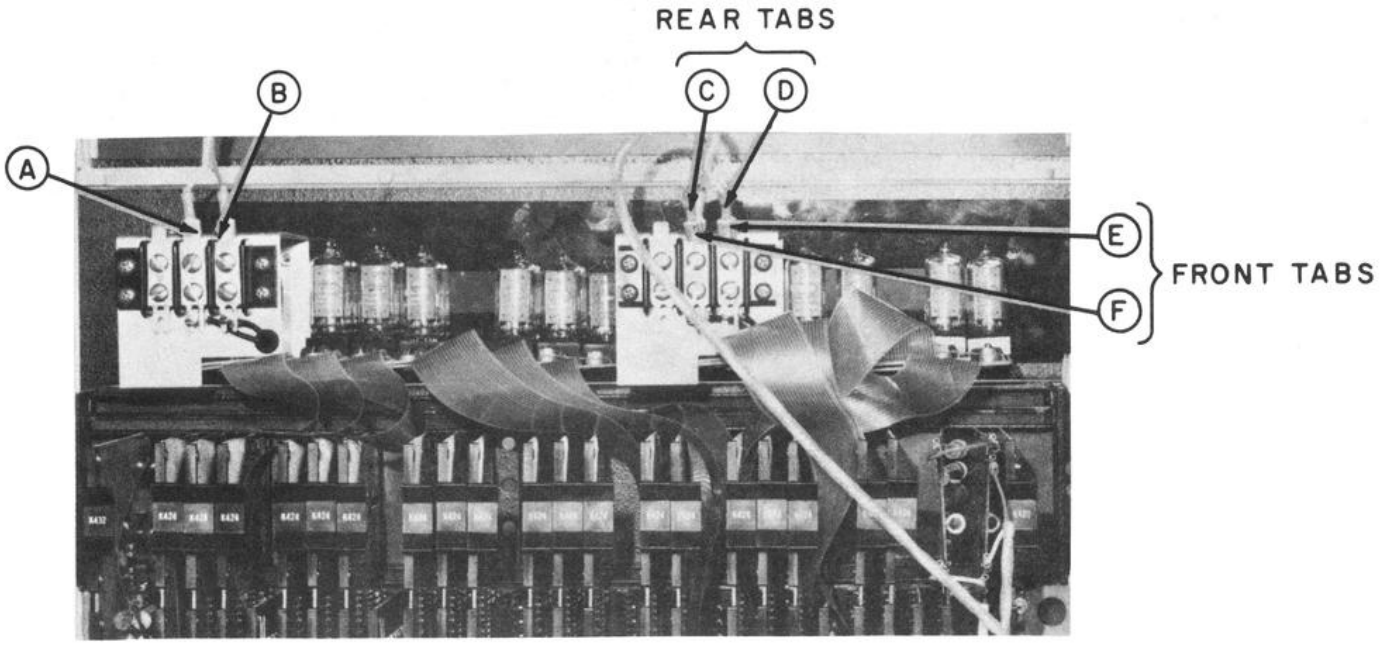


Figure 2-23 K771 Power Supply – Wiring Guide (Two K771s)

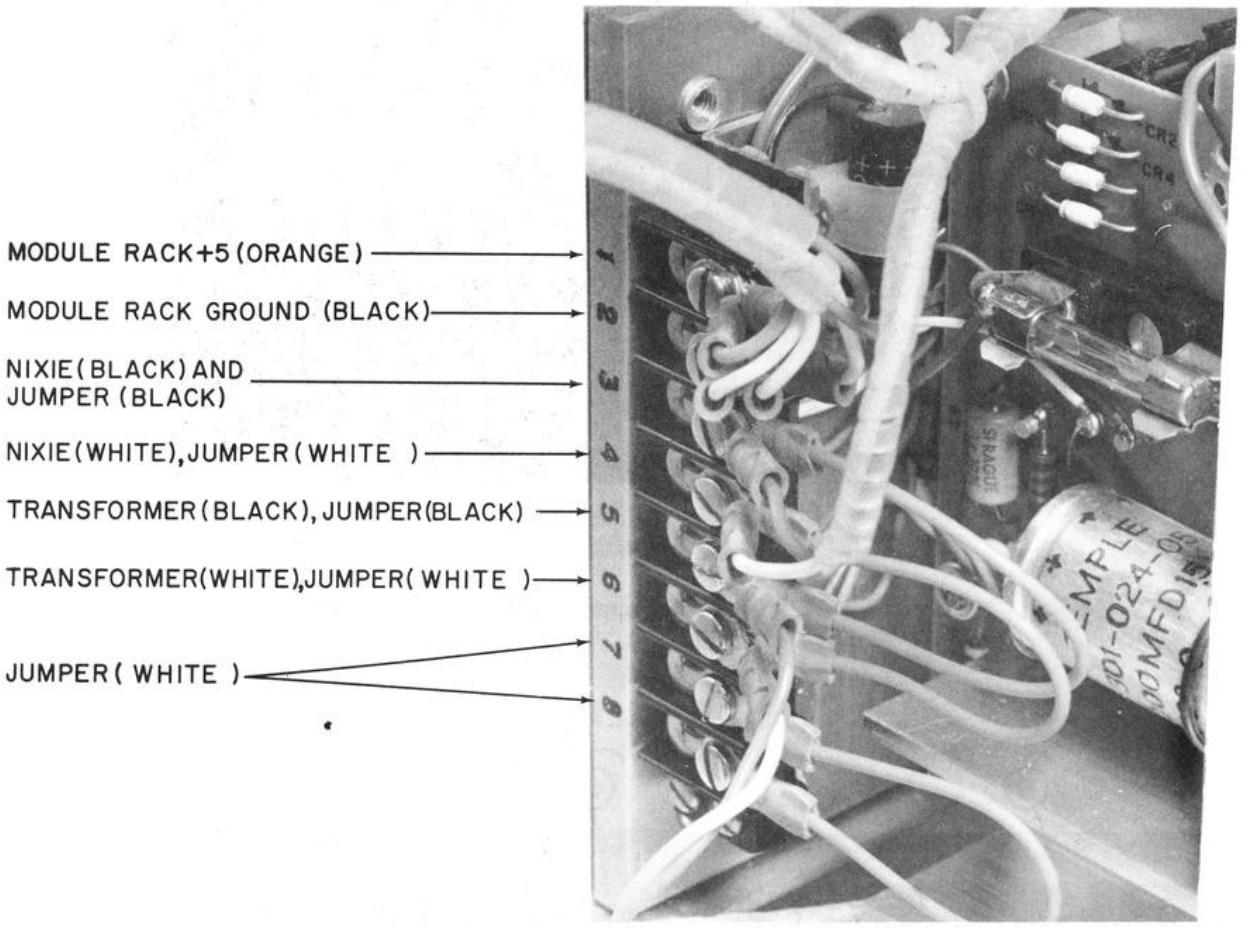


Figure 2-24 Power Supply – Terminal Board (TB) Wiring Guide

2.8 ASSEMBLING, WIRING, AND MOUNTING THE OUTPUT HARDWARE

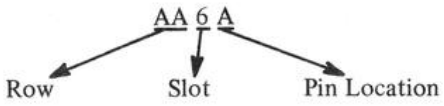
Assemble and wire the output hardware (see Figure 2-25) as follows:

Step	Procedure
1	Mount the connector bracket to the mounting bar, and the mount to the H800 Connector Blocks (see Figure 2-26).

NOTE

If you did not wire-wrap the modular panel, refer to the appendices and Section 2.2 for wire-wrapping instructions.

2 Wire-wrap the connector block for interconnection between K644 connector cable and K782 as follows (see Figure 2-27):



From	To
AA6A	BB8M
AA6C	BB8P
AA6E	BB8S
AA6H	BB8U
AA6M	BB8A
BB8A	BB8C
BB8C	BB8E
BB8E	BB8H
BB6A	BB8N
BB6C	BB8R
BB6E	BB8T
BB6H	BB8V

3 Mount the assembled Output hardware at the location shown in Figures 2-11 and 2-26.

4 Connect the K782 Terminal Module to K580, and connect K784 Terminal Modules to the K683 (see Figures 2-28 and 2-29).

a. Prepare two 3-ft., 8-conductor ribbon cables.

Step	Procedure
4 (cont)	

b. Solder one end of the ribbon cable to the K784 and the other end to the K683, as shown in Figure 2-28.

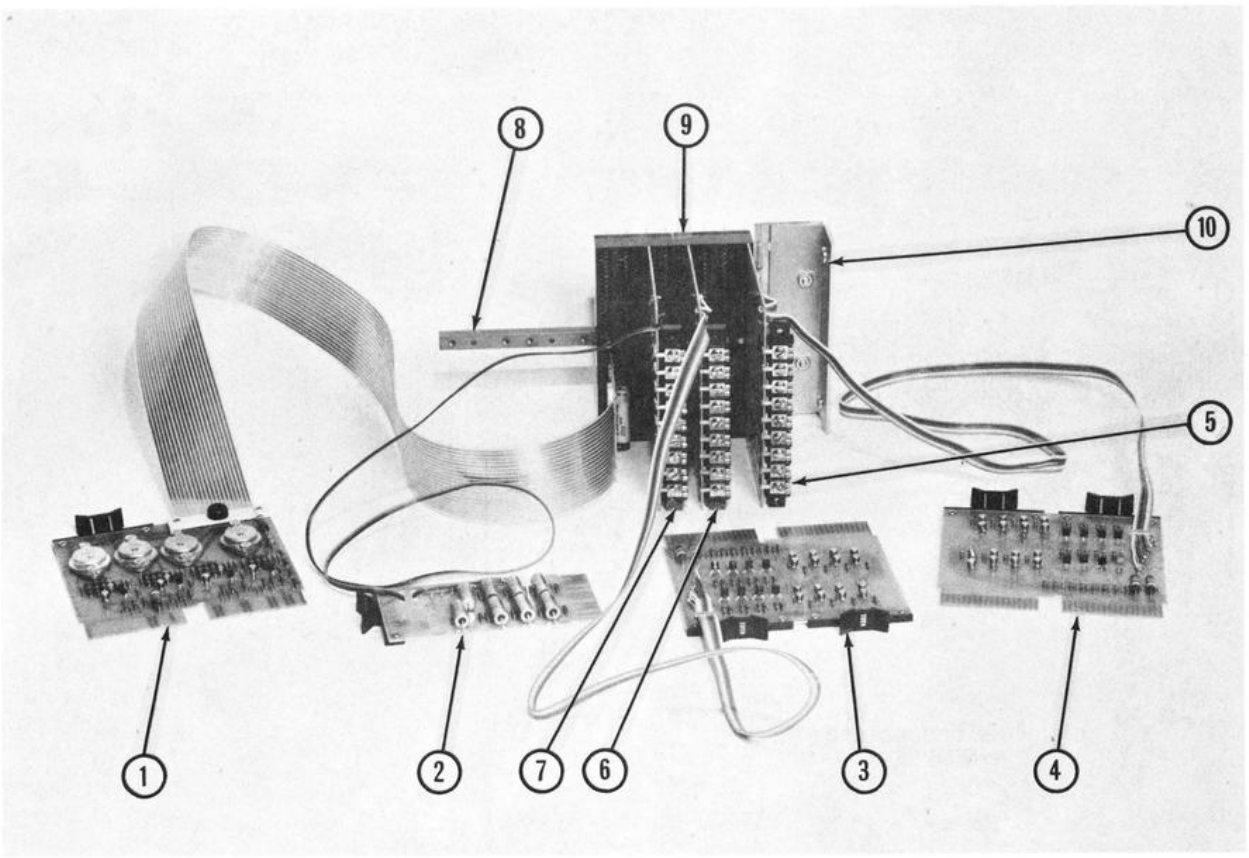
c. If the IRT option has been acquired, repeat step 4b for the second K784 and K683.

d. Prepare a 3-ft., 3-conductor ribbon cable.

e. Solder one end of the ribbon cable to the K782 Terminal Module and the other end to the K580, as shown in Figure 2-29.

f. Plug the Input/Output terminal modules into the Output mounting rack, and then plug the module connector into the mounting rack at the locations shown below (see Figure 2-27).

Module	Input/Output Rack	Module Mounting Rack
K784	AA2	(K683) C30
K784	AA4	(K683) C31
K782	AA6	(K580) F14
K644	BB8	(K644) C32



Index	Nomenclature
1	K644 Driver Module
2	K580 Dry Contact Filters
3	K683 Lamp Drivers
4	K683 Lamp Drivers
5	K784 Terminal Module
6	K784 Terminal Module
7	K782 Terminal Module
8	K941 Mounting Bar
9	H800 Connector Block
10	K940 Mounting Support

Figure 2-25 Output Hardware – Assembly Unit

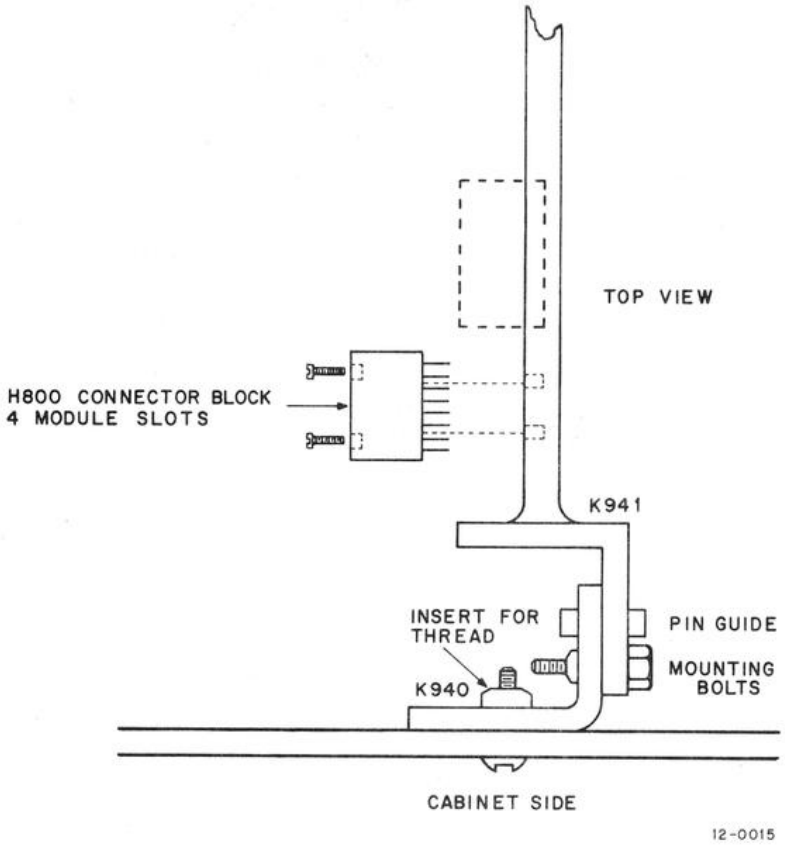


Figure 2-26 Output Assembly – Mounting Bar

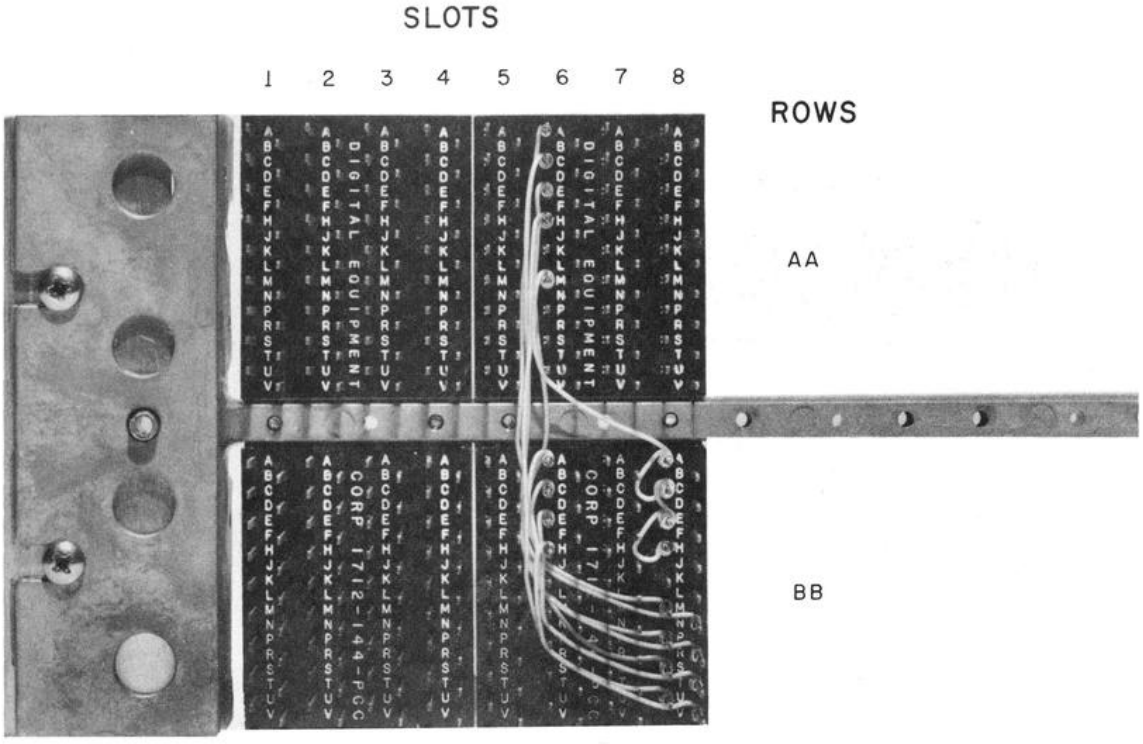
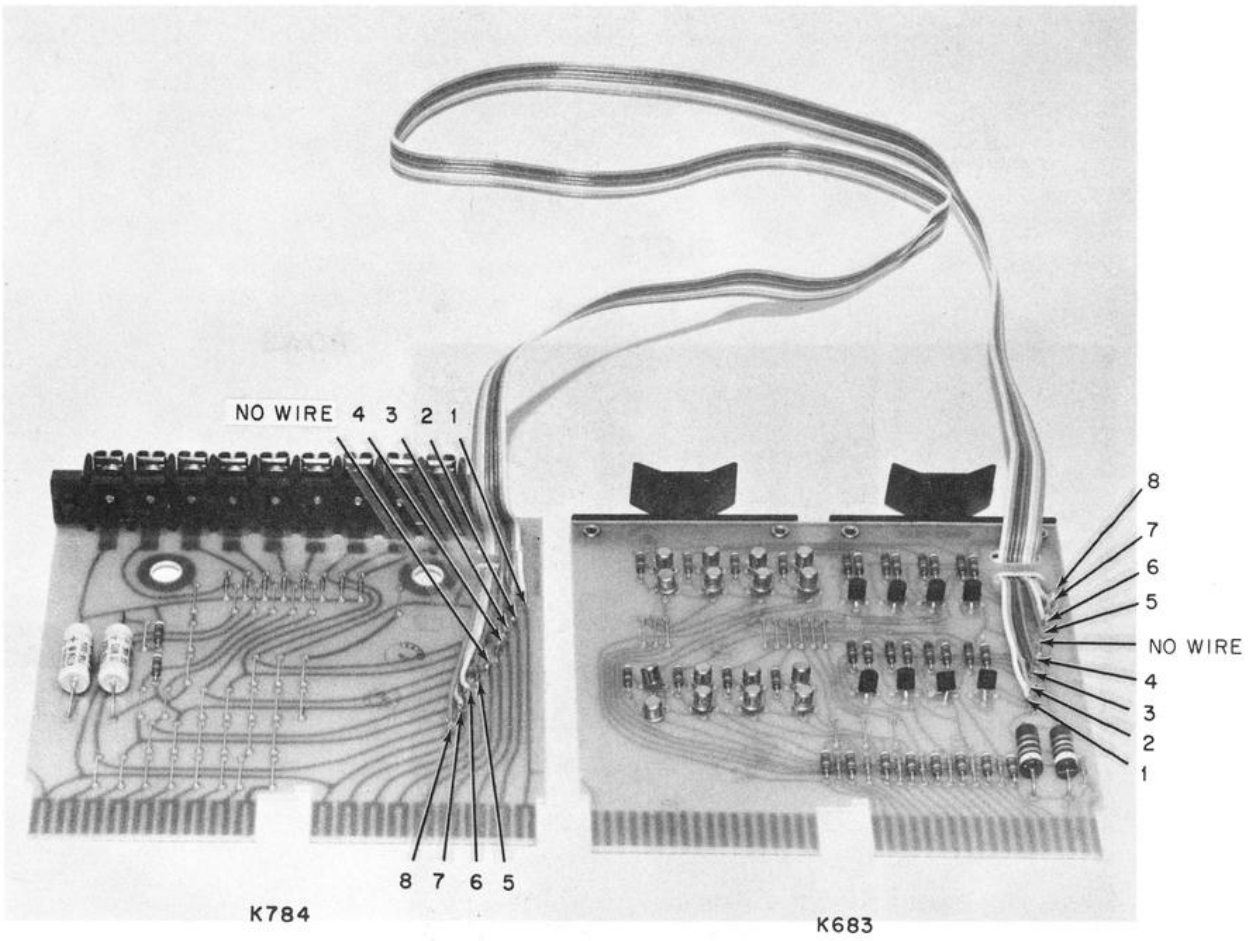


Figure 2-27 Output Assembly – Connector Block



K784	to	K683
1		1
2		2
3		3
4		4
5		5
6		6
7		7
8		8

NOTE

As shown in the above photo, the K784 split lugs are counted in the opposite direction from the K683 split lugs.

Figure 2-28 K784 Wiring Guide

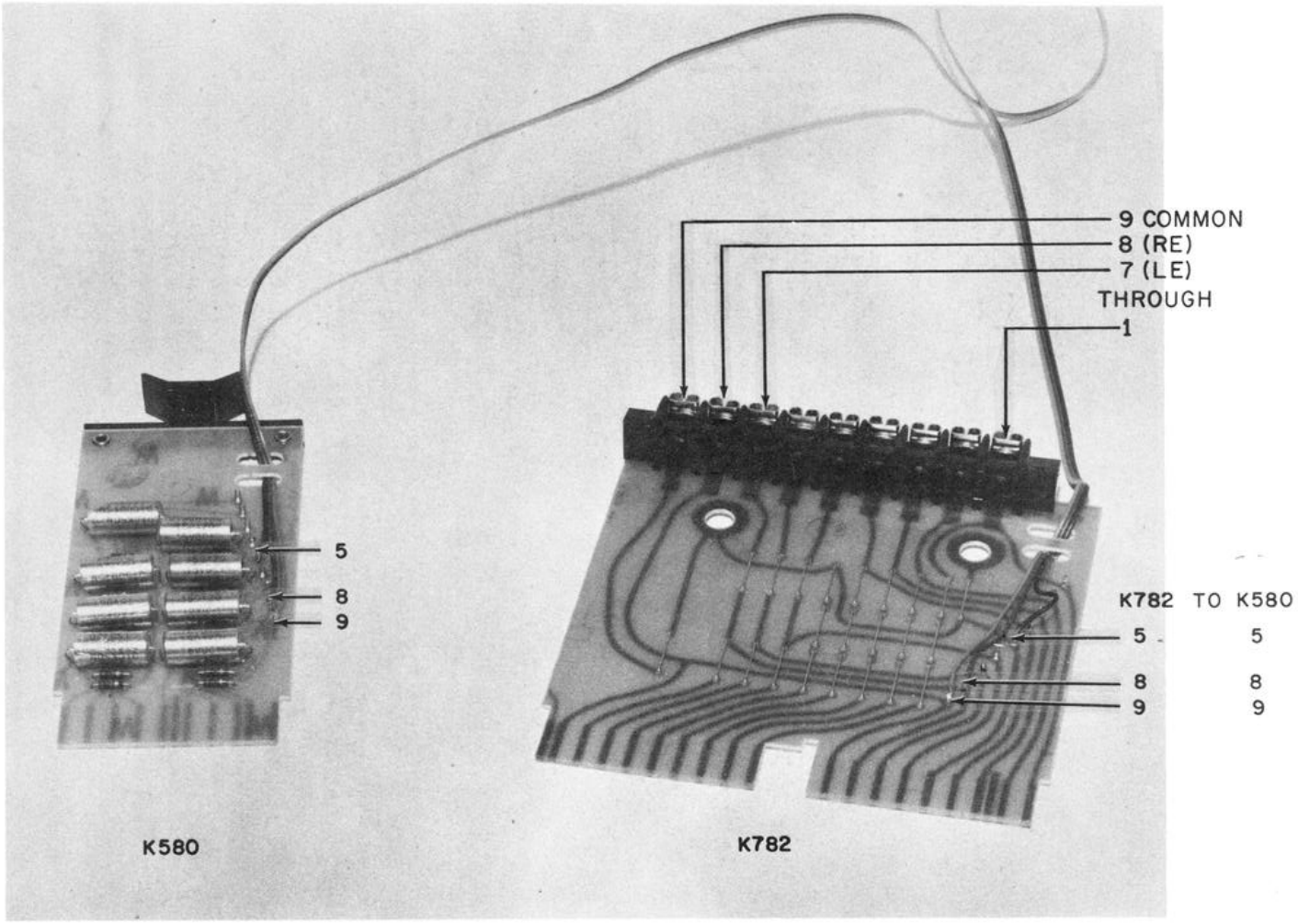


Figure 2-29 K782 Wiring Guide

2.9 MOUNTING AND CONNECTING THE PATCHBOARD

Step	Procedure
1	Mount the patchboard programmer onto the cabinet in the location shown in Figure 2-11.
2	Connect the patchboard connector cables to the module mounting panel, as shown in Figure 2-30.

NOTE

Odd numbered cables are connected to side 1 of the printed circuit board, and even numbered cables are connected to side 2. Side 1 (marked on the board) is the side that can be seen from the rear of the cabinet.

Side 1

Cable	Slot Number
1	E29
3	E31
5	F29
7	F31

Side 2

Cable	Slot Number
2	E30
4	E32
6	F30
8	F32

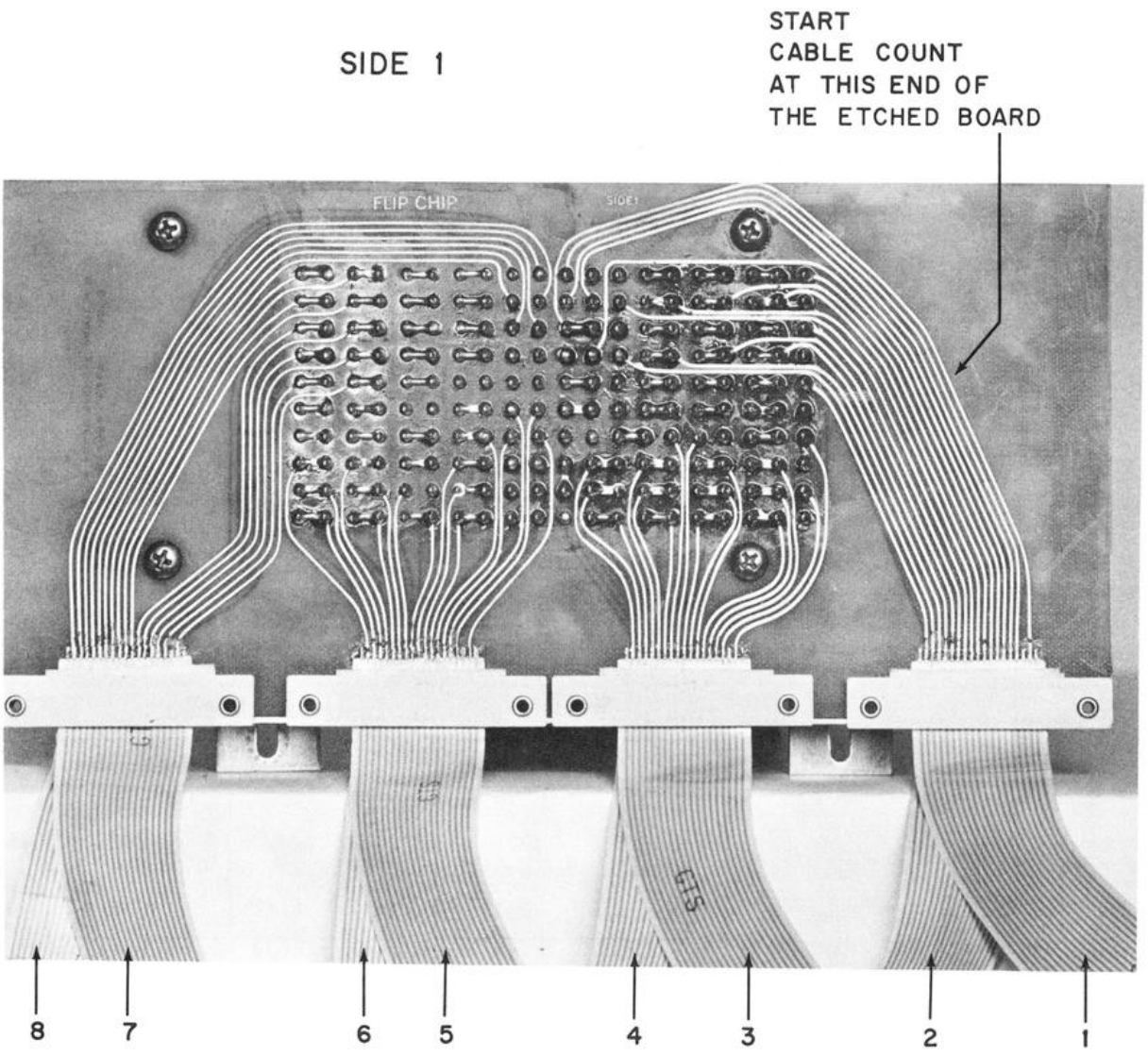


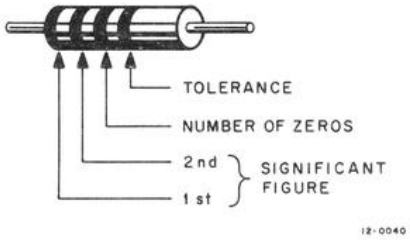
Figure 2-30 Patchboard Connector Cables – Module Rack Location

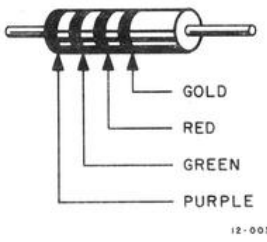
2.10 MOUNTING CAPACITORS AND RESISTORS TO THE K990 BOARDS

Resistors are specified by a color code. Each color is assigned a value, as shown below. It is standard practice to use three bands. Starting from the end, the first band denotes the first digit in the resistance value, the second band represents the second digit, and the third represents the multiplier (the number of zeros following the first two digits). Thus, bands of brown, red, and red are read: 1 for the first digit, 2 for the second digit, and 2 for the number of zeros to be added – 1,200 ohms (1.2K). Orange, white, and orange is read: 39,000 ohms (39K).

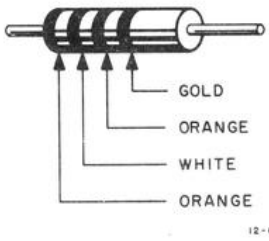
A fourth band is used to indicate tolerance. A silver band indicates a value within 10%; thus, a 1200-ohm resistor with a silver band may range in value from 1080 to 1320 ohms. A gold band represents a value within 5% of the coded value. When the fourth band is not used, the value is within 20%.

Color	Digits	Color	Tolerance
Brown	1	Silver	10%
Red	2	Gold	5%
Orange	3		
Yellow	4		
Green	5		
Blue	6		
Violet	7		
Gray	8		
White	9		
Black	0		

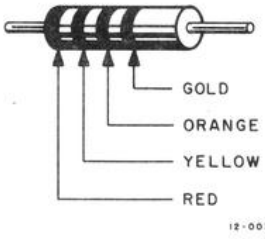




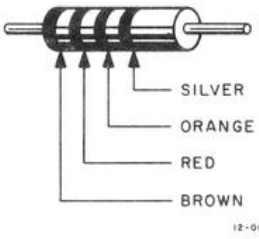
7.5K



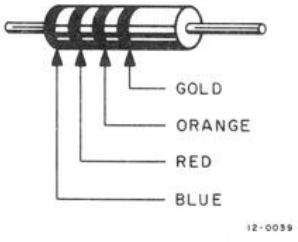
39K



24K

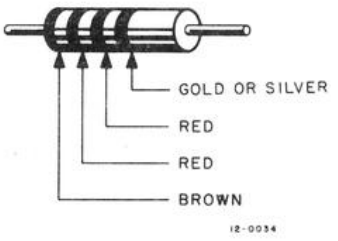


12K



62K

Step	Procedure
1	Prepare the "A26" board by mounting six 1200-ohm, 1/4W, resistors to a K990 Board as follows:



1.2K

a. Insert the 1.2K resistors in mounting holes of a K990 Board at the locations shown in Figure 2-31.

b. Bend the leads in the direction of the "tear" flow, and clip off the excess (see Figure 2-32).

c. Solder the leads in place at the tear (see Figure 2-32).

d. Insert a jumper (ground) at the location shown in Figure 2-31. Use 24 gauge solid wire.

e. Mount the module in slot A26.

2 Prepare the "A07" Board by mounting six resistors and a jumper to a K990 Board in the same manner as described in Step 1; the mounting locations are shown in Figure 2-31.

3 Prepare the "A30" Board by mounting six resistors, four capacitors, and nine jumpers to a K990 Board in the same manner as described in Step 1; the mounting locations are shown in Figure 2-31.

The resistors and capacitors connected to contacts P, U, and V are used to set the time on the heavy duty driver and the lamp driver one shots. For example, the one shot for lamp driver No. 3 (Application F, X602-0-2) can be set for 50 ms, 100 ms, or 250 ms by connecting Pin V of the one shot to pin P, U, or V, respectively, of the "A30" K990 Board connector block.

	Driver	One Shot Pin
Heavy Duty	No. 2	F29P
	No. 3	F28V
	No. 4†	F27J
Lamp	No. 4	E27V
	No. 5	E27P
	No. 6	E27J

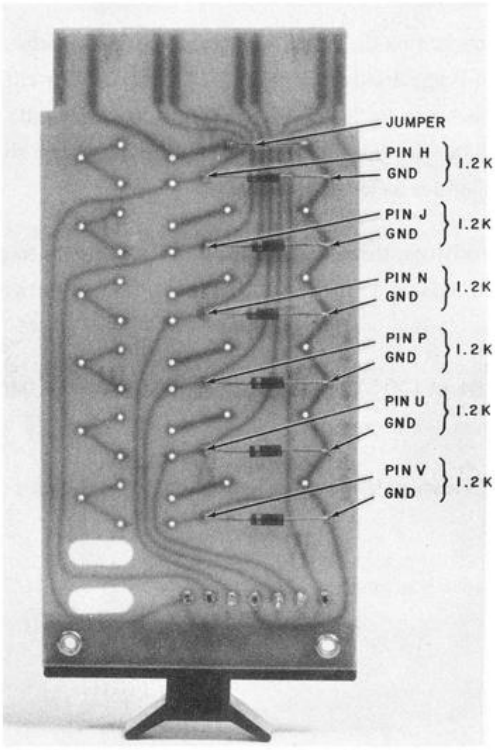
NOTE

†Driver No. 4 must be disconnected from the K432 adjustable potentiometer.

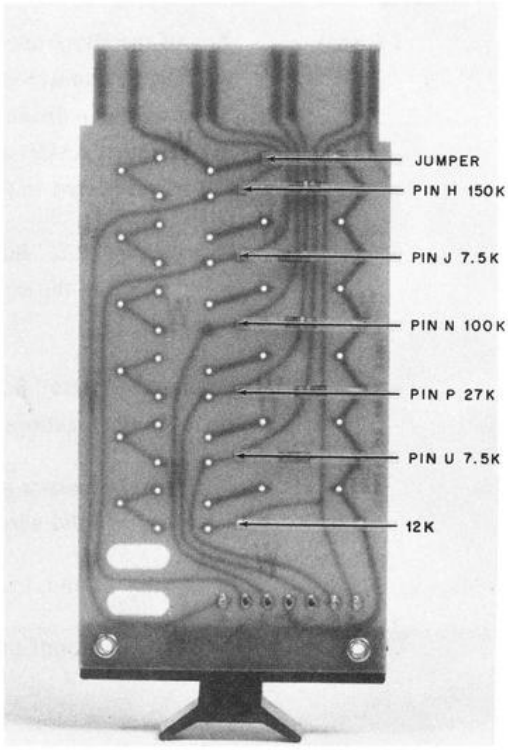
Connected To

A30P = 50 ms
A30U = 100 ms
A30V = 250 ms

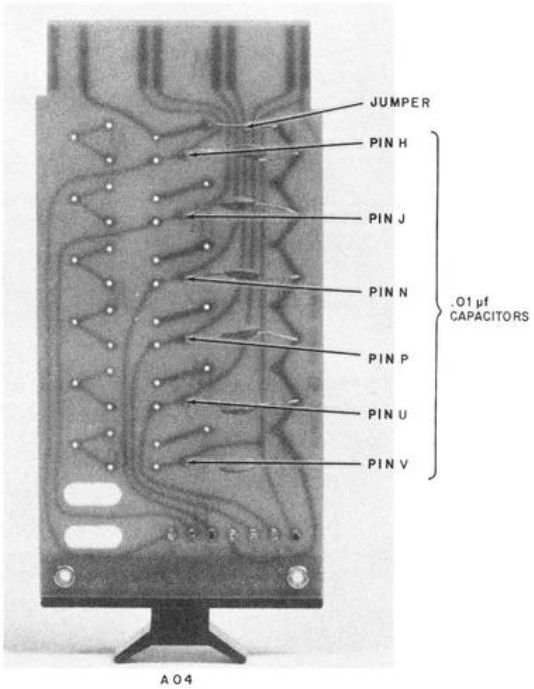
Step	Procedure
3 (cont)	Any of the above one shots can also be connected to the K432 adjustable potentiometer. These pins can be connected to one of the K432 pins specified in Section 2.11, Step 3. For example, to set the lamp driver No. 4 one shot for 1 sec connect E27V (driver No. 4 one shot pin) to pin A31J (or A31V) and A31L of the K432 (see Section 2.11, Step 3). The other one shot can be connected to the K432 in the same manner described above.
4	Prepare the "A22" Board by mounting six resistors, three capacitors, and six jumpers to a K990 Board in the same manner as described in Step 1; the mounting locations are shown in Figure 2-31.
5	Prepare the "A04" Board by mounting six .01 μf (20%) ceramic disc capacitors to a K940 Board in the locations shown in Figure 2-31. a. Insert a jumper (ground) at the location shown in Figure 2-31. Use 24 gauge solid wire. b. Bend, trim, and solder the leads as described in Step 1. c. Mount the module in slot A04.



A26

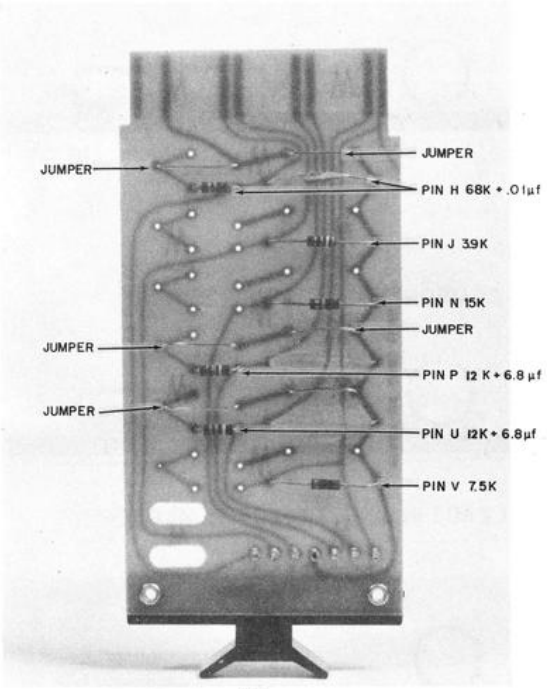


A07 BOARD

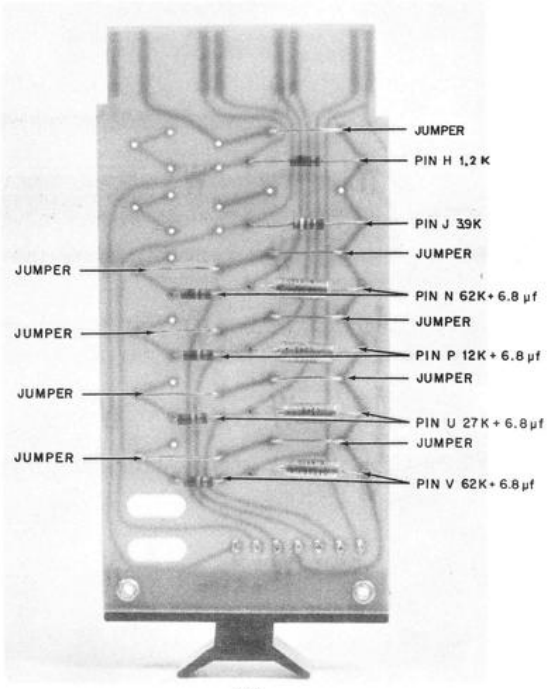


A04

Figure 2-31 Resistors and Capacitors – K990 Mounting Locations

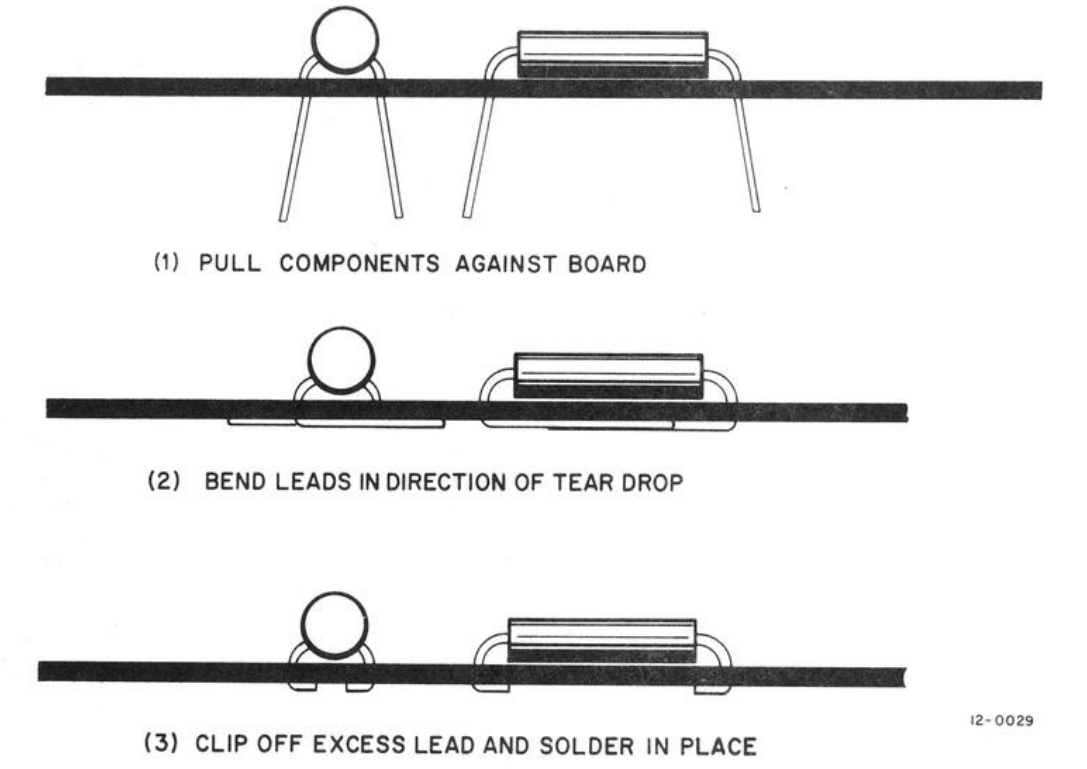


A22



A30

Figure 2-31 Resistors and Capacitors – K990 Mounting Locations (Cont)



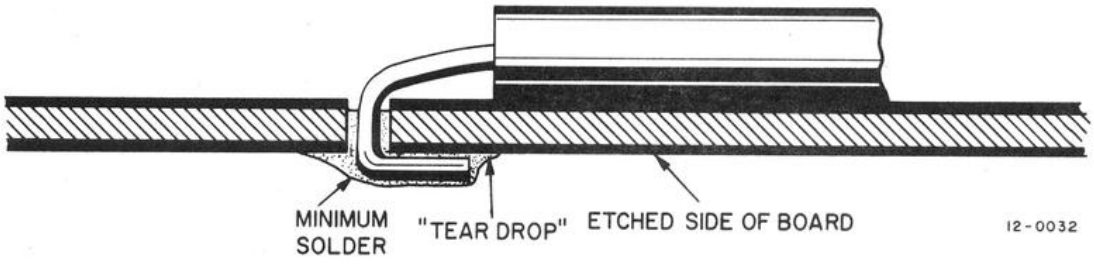


Figure 2-32 Capacitor, Resistor Mounting/Soldering Guide

2.11 INSTALLING K424 THUMBWHEEL SWITCHES, K420 TOGGLE SWITCH, AND K432 ADJUSTABLE POTENTIOMETER

Install the K424 thumbwheel switches, the K420 toggle switch, and the K432 adjustable potentiometer, as follows:

Step | **Procedure**

1 Install the K424 Decoders (thumbwheel switches) and the K422 Encoders (thumbwheel switches) at the following locations:

Number of K424s (Decoders)	Application	Module Rack Location
1	0 - 9 Sequencer (B)	A8
3	Up Counter (E)	A19, A20, A21
5	VI/VR Programmer (M)	A8, A9, A10, A12, A13
2	Session Timer (N)	A5, A6
3	Second VI/VR	A12, A13, A15, A16, A17
1	IRT Distributor (Q)	A17

Number of K422s (Encoders)	Application	Module Rack Location
6	Down Counter (C)	A23, A24, A25 A27, A28, A29

2 Plug the K420 Toggle Switch into module rack location A1.

3 Plug the K432 Adjustable Potentiometer into module rack location A31.

a. To set the K432 to any of seven time ranges, pins J and V must be connected as shown below.

Connect to Pin J or V	RC Time Range	
	Min.	Max.
None	10 μs	30 μs
D or R	100 μs	3 ms
E or S	1 ms	30 ms
F or T	10 ms	300 ms
H or U	100 ms	3 sec
L	1 sec	30 sec

Step	Procedure
3 (cont)	For example, if a 100 μs to 3 ms range and a 1 ms to 30 ms range is required, connect pin J to to D or R for the first range, and pin V to E or S for the second range. The top thumbwheel controls pin V, and the bottom thumbwheel controls pin J. Move the thumbwheel control up for the minimum range and down for the maximum range.

2.12 ASSEMBLING AND MOUNTING THE MODULAR PANEL KIT

Assemble and mount the Modular Panel Kit (see Figures 2-33 and 2-34), as follows:

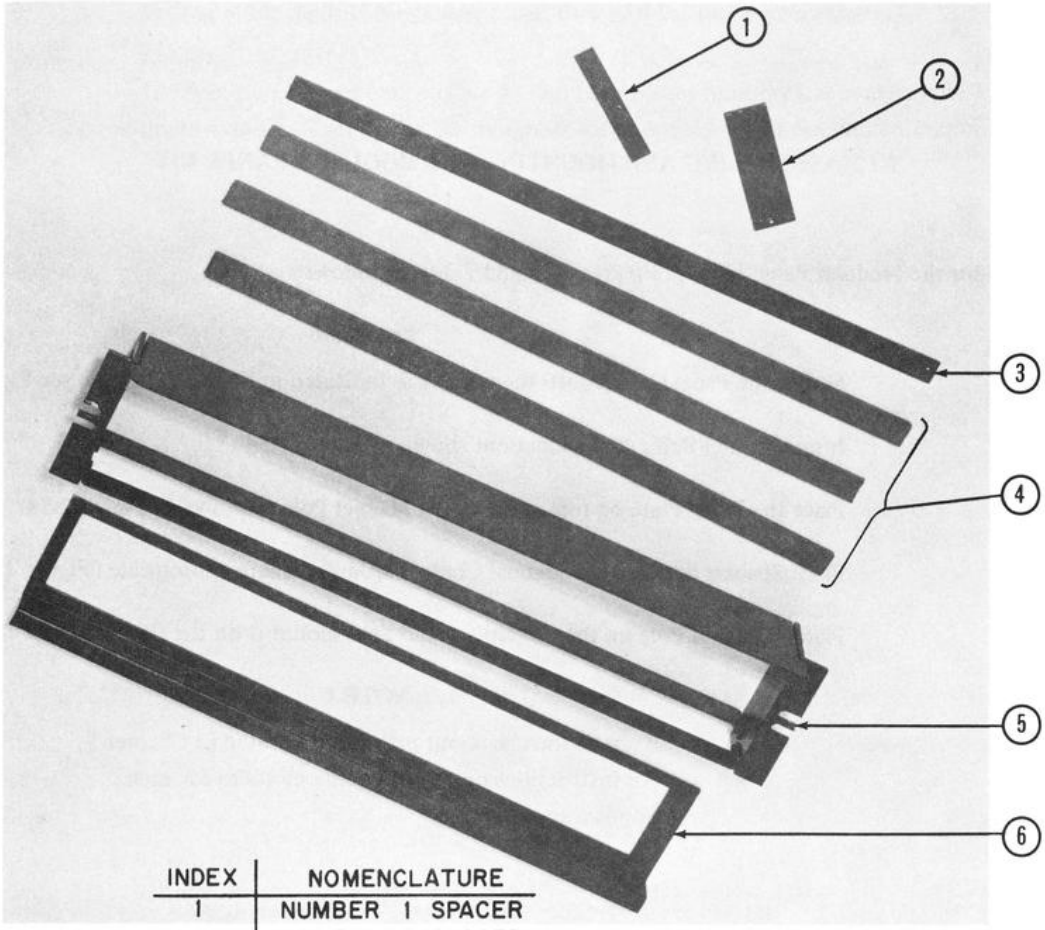
Step	Procedure
1	Mount the Panel Casing onto the cabinet as indicated in Figure 2-35 (also see Figure 2-34).
2	Insert Magnet Poles at the locations shown in Figure 2-34.
3	Place the Bezel Plate on top of the upper Magnet Pole as shown in Figure 2-34.
4	Place Spacers between the Manual Control Modules where appropriate (Figure 2-34).
5	Place a Magnet Pole on the Coverplate and then mount it on the Panel Casing.

NOTE 1

Turn to the check-out procedure, located in Chapter 5, for instructions on mounting the modules for each application.

NOTE 2

Figure 2-35 is a rear view of the Coverplate; therefore, when mounting the Coverplate - turn the piece to a position where the Magnet Pole is at the top and facing inward, then insert.



INDEX	NOMENCLATURE
1	NUMBER 1 SPACER
2	NUMBER 2 SPACER
3	BEZEL PLATE
4	MAGNET POLES
5	PANEL 1
6	PANEL 2

Figure 2-33 Modular Panel Kit – Assembly Units

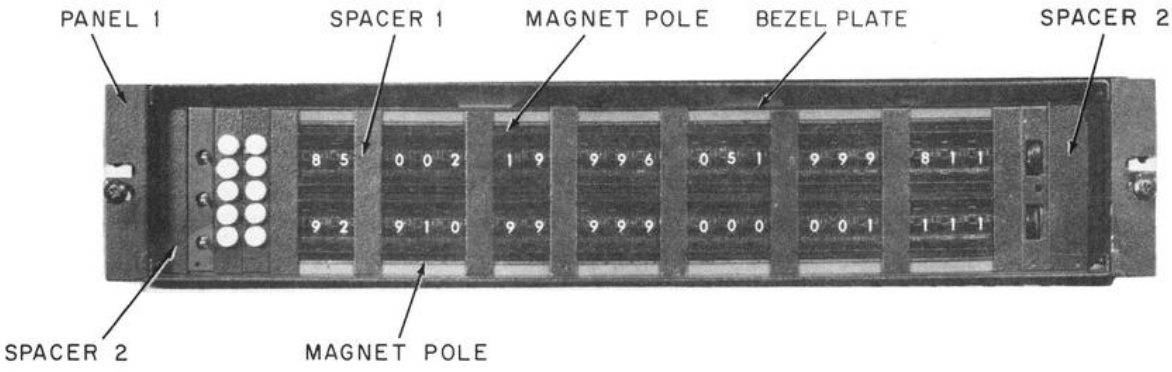


Figure 2-34 Modular Panel Kit – Mounting Guide

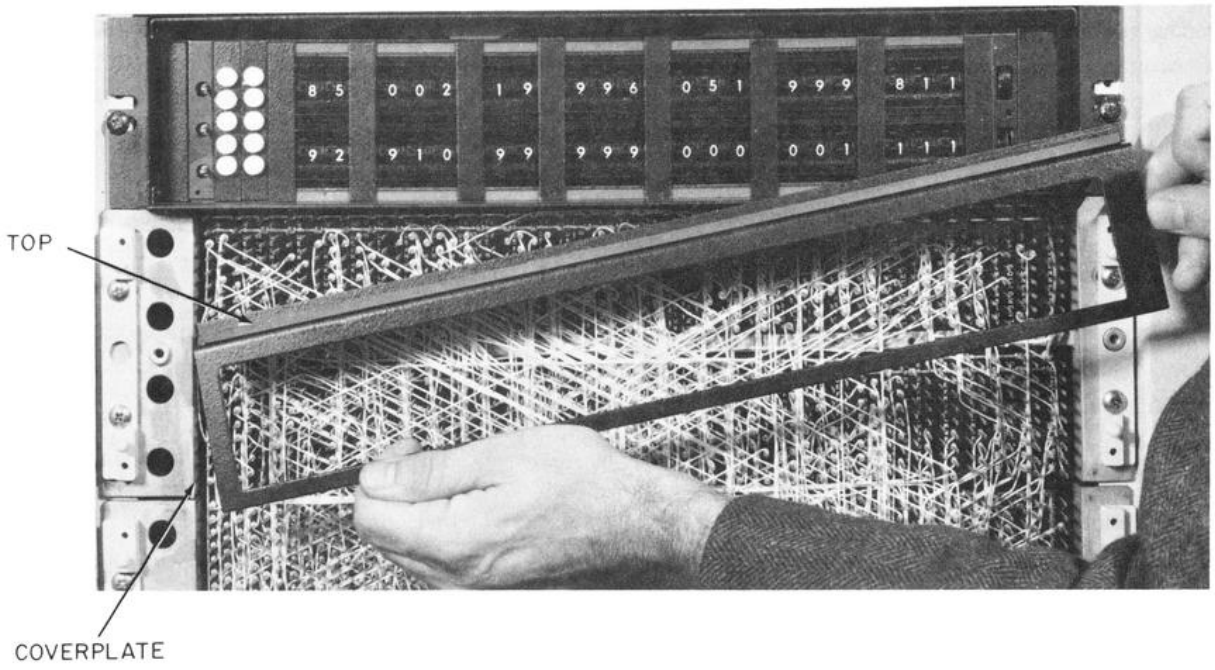


Figure 2-35 Panel 2 and Magnet Pole

CHAPTER 3
BUILDING BLOCKS OF DIGITAL LOGIC

3.1 LOGIC SYSTEMS – AN INTRODUCTION

All digital logic systems consist of three rudimentary building blocks – AND, OR, and NOT. These building blocks, called operators, are the elements used to build simple or complex logic systems. The basic building blocks of digital logic can be arranged in very complex logic system configurations; but it is possible to separate any logic system into its basic building blocks. The material in this chapter provides the research psychologist with the necessary information to functionally evaluate the electronic circuits that are described in the schematics of logic, i.e., determine what a circuit does logically and what its functional purpose is within a system. A detailed technical knowledge of electronic circuitry is not necessary to achieve this end. Logic systems are divided into three functional groups: a. input, b. application logic, and c. output.

The input logic is designed to facilitate the processing of signals which emanate from outside a system. This logic usually consists of switches, contact closures, schmidt trigger, etc. Basically, the input logic conditions signals so that the electronic components of a system will respond to the signals.

The application logic interprets external events, in the form of electronic signals, and responds electronically according to the nature of the event. The discriminatory sensitivity and response contingencies of the logic must be programmed. In the case of LAB-K, this programming is done on the patchboard. The application logic is also used to "remember" and record events. These tasks are accomplished with flip-flops and counters.

The output logic is used to process a response signal of a system. The response signals are inputted to drivers. These drivers are connected, in turn, to external equipment, e.g., test chambers, lights, data recorders, display device, etc.

The majority of text in this chapter deals with the application logic. The material is divided into two major sections: application logic and input/output devices. Section 3.2, Application Logic, consists of: Logic Signals, Logic Operators AND, OR, NOT; Flip-Flops, Encoders and Decoders. Section 3.3, Input/Output Devices is a brief discussion of the types of devices (mostly electromechanical in nature) used in the input and output groups.

In both sections, the schematic symbols used to exemplify logical prototypes are exact reproductions from the LAB-K schematics; thus, the knowledge gained from this chapter can be directly related to the LAB-K schematics. Also, this chapter will serve as a convenient reference source when using the LAB-K schematics.

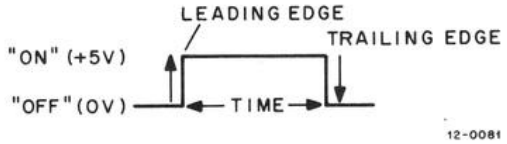
3.2 APPLICATION LOGIC

3.2.1 Logic Signals

There are two states in digital logic: ON or OFF. The ON state or OFF state is defined in terms of voltage levels and the subsequent transition from one state to the other.

Logic is divided into two classifications: a. positive logic, b. negative logic.

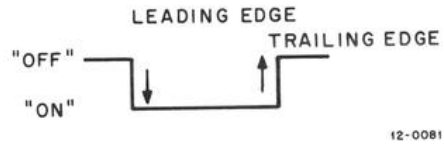
Positive logic is defined as having the most positive level as the ON state, and the most negative level as the OFF state. The ON and OFF states are usually referred to as Logic 1 and Logic 0, respectively. Logic 1 is also called High (H), and Logic 0 is called Low (L).



In the LAB-K logic, the ON state (Logic 1) is a voltage level of +5 volts (V) and the OFF state (Logic 0) is a voltage level of 0V. It should be understood that the terminology 0V is used in reference to the power supply and does not imply the absence of voltage. Logic 0 is always connected to an earth ground; consequently, the terms 0V and ground are synonymous.

The transistion from Logic 0 to Logic 1, or vice versa, is called the command signal. These transitions trigger electronic components; that is, they cause the component to change logic states from ON to OFF, or vice versa. The transition from OFF to ON is called the leading edge, and the transition from ON to OFF is called the trailing edge. The width of a pulse is the length of time that a level (1, 0) is maintained.

Negative logic is defined as having the most negative level as the ON state and the most positive level as the OFF state.

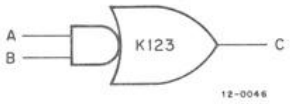


3.2.2 Logic Operators

3.2.2.1 **AND Gate** – A logic function that has an output of 1 (high), when all inputs are 1, is called an AND gate. If any of the inputs are 0, then the output will be 0 (low). The Boolean equation for an AND function is $A \cdot B = C$, which reads: If A and B, then C, i.e., if A and B are both true (1), then C is true.

The logic symbol for an AND gate is:

In the LAB-K, the K123 Module is a two-legged input AND gate. The K123 can also be used as an OR gate (refer to Section 3.2.2.2).



Logic functions, as a matter of expediency, are expressed in truth tables. The truth table for the two-legged AND gate is expressed

A	B	C
L	L	L
H	L	L
L	H	L
H	H	H

or

A	B	C
0	0	0
1	0	0
0	1	0
1	1	1

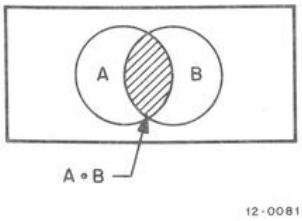
where: 1 = true H = 1
0 = false L = 0

C is true only when A and B are true; however, the truth table does not define true and false. In terms of the electronic system, the "false" state may be true; that is, if a transition from high to low is needed at the output, then this can only occur when the AND gate goes from the "true state" to the "false state".

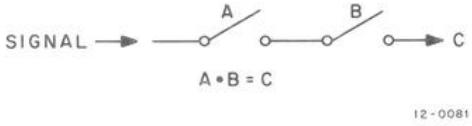
Inputs A and B can be symbolically represented in a Venn diagram.

NOTE

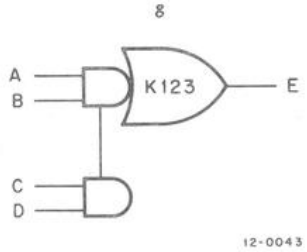
The AND gate is symbolized by the crosshatched area.



Another symbolic representation of an AND gate is a series connected electronic circuit. Both switches A and B must be closed before the signal will appear at C.

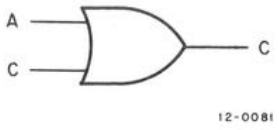


AND gates are not restricted to just two inputs; they may have any multiple input.



3.2.2.2 **OR Gate** – The OR gate is a logical disjunction. A function that has a high (1) output if any of its inputs are high (1), and a low (0) output if both inputs are low (0). The Boolean equation for the OR function is A+B=C, which reads: If A or B, then C, i.e., if either A or B is true (1), then C is true (1).

The logic symbol for an OR gate is:



The truth table for the OR gate is expressed:

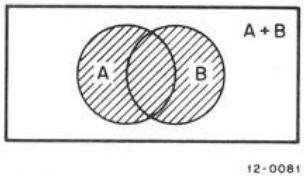
A	B	C
0	0	0
0	1	1
1	0	1
1	1	1

or

A	B	C
L	L	L
L	H	H
H	L	H
H	H	H

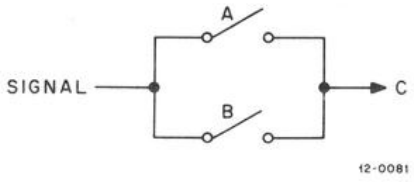
Thus, C is high when A or B is high, and it is low only when both A and B are low.

A Venn diagram of the OR function is:



Inputs A and B are represented by the crosshatched circles; thus, the OR gate is that area included within both circles. At all points within the circles, either A or B exists (1 or H). In the area outside the circle neither A nor B exists ($\overline{A + B}$).

An electrical representation of the OR gate is a parallel circuit.

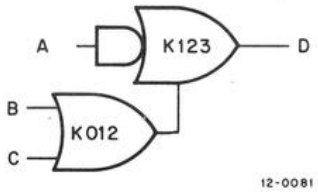


If either switch (or both) is closed (A + B), a signal will appear at C.

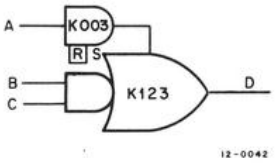
In the LAB-K, the K123 and K124 Modules are used as OR gates.

Examples:

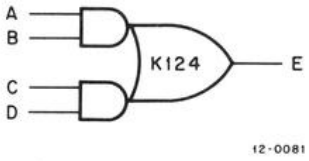
A+B+C (A or B or C) = D
If A or B or C are high, then the output (D) is high.
If A, B and C are all low, then the output is low.



A+BC (A or B and C) = D
If A is low, and BC are not both high, then the output (D) is low.
If A is high, or BC are high, then the output is high. If A is high, the output is always high.



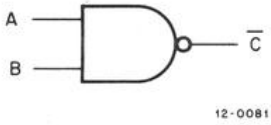
AB + CD = E
If AB or CD is high, then the output (E) is high. If AB and CD are both low, then the output is low.



3.2.2.3 **NOT – NAND, NOR Gates** – The NAND gate function is the inverse of an AND gate (NOT AND). If all the inputs to a NAND gate are high (1), then the output is low (0). If any of the inputs are low (0), then the output is high.

The Boolean equation for a NAND function is $\overline{A \cdot B} = C$, which reads: If not A and B, then C.

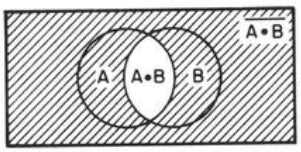
The logic symbol for the NAND gate is:



The truth table for the NAND gate is expressed:

A	B	C
0	0	1
0	1	1
1	0	1
1	1	0

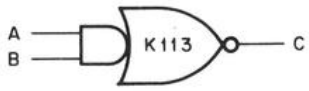
A Venn diagram of the NAND function is:

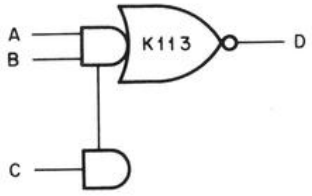


12-0081

The NAND gate is represented by the crosshatch area. (A and B never exist simultaneously in this area.) As a result, $\overline{A \cdot B}$ is equal to 1 (unity), which is the inverse of A·B. (Compare the Venn diagrams of the NAND and AND gates.)

In the LAB-K, the K113 Module is used as a NAND gate.





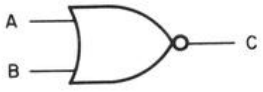
12-0081

The output of the above NAND gates is low only when all the inputs are high. If any of the inputs is low, then the output is high.

The NOR gate function is the inverse of the OR gate (NOT OR). If all the inputs to a NOR gate are low, then the output is high. If any of the inputs is high, then the output is low.

The Boolean equation for a NOR function is $\overline{A+B}=C$, which reads: If NOT A or B, then C.

The logic symbol for the NOR gate is:

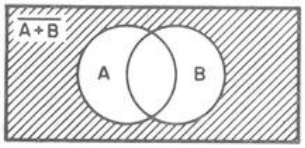


12-0081

The truth table for the NOR gate is expressed:

A	B	C
1	1	0
0	1	0
1	0	0
0	0	1

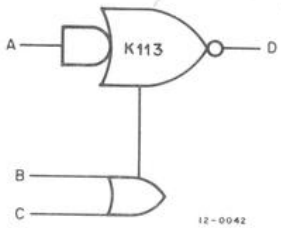
A Venn diagram of the NOR function is:



12-0081

The NOR gate is represented by the crosshatched area; neither A nor B exist in this area.

In the LAB-K, the K113 module is used as a NOR gate.



12-0042

$\overline{A}+\overline{B}+\overline{C}=D$

NOTE

Do not confuse this gate with the K113 NAND gate. When used as a NAND gate, the expander gate is shown schematically attached to the NAND expander node rather than the NOR expander node as shown here.

The output of the above NOR gate is high only when all the inputs are low. If any of the inputs is high, the output is low.

3.2.2.4 **Flip-Flops** – The logic gates discussed thus far all require a continuous input level to operate. If the input level is removed, the gate does not "remember" its previous input condition. A push-button switch is an example of a device that does not have a memory. The push-button operates as long as the button is depressed.

In addition to logic gates, the LAB-K utilizes devices that remember their condition after an input has been removed. A light switch illustrates a device with memory. When a light switch is turned on, it remains on until it receives an impulse to turn off. After it is turned off, it remains off until another ON impulse is received.

In the LAB-K, a device that has a memory is called a flip-flop. The flip-flop is a logic element which always exists in one of two stable states – the 1 condition or the 0 condition. This type of component is called a bistable device (the seesaw is a good physical analogy). If a flip-flop receives an instruction to go to the 1 condition it does so and stays there until instructed to go to the 0 condition. If a flip-flop is in the 1 condition and receives an instruction to go to the 0 condition, it does so and stays there until instructed to return to the 1 condition.

Flip-flops generally provide both a high (1) and low (0) output that are outputted on two lines. The two output lines are called the 1 output and the 0 output. The 1 and the 0 identify the output lines. They do not mean that one line is always high and the other is always low.

If the 1 output is high, it indicates that the flip-flop is in the 1 condition. If the 0 output is high, the flip-flop is in the 0 condition. The 0 output always presents the opposite, or complement, of the information at the 1 output, and vice versa. There are, therefore, only two possible output conditions, either the 1 output is high and the 0 output low, or the 0 output is high and the 1 output is low.

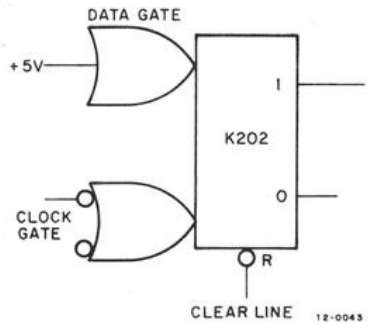
Outputs		Flip-Flop
1	0	State
H	L	1
L	H	0

Flip-flops are used for control, or they are combined and used as a binary counter, up-down counter, or divider.

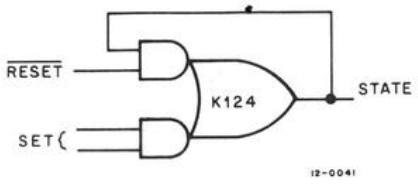
In the LAB-K, the K202, the K124 and the K113 Modules are used as flip-flops.

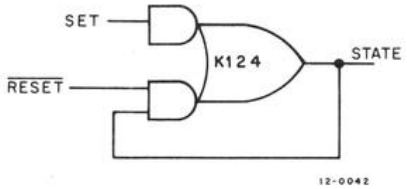
When the output of the K202 Clock Gate goes from high to low, the information on the data gate, which in the LAB-K is always high (+5V), is transferred into the flip-flop. And in this case, the flip-flop is always put in the 1 state (output 1 is high, and output 0 is low).

Whenever the clear line goes low (ground), the flip-flop is put in the 0 state (output 0 is high, and output 1 is low). The flip-flop stays in the 0 state as long as the clear line is low, regardless of the input at the data and clock gates.

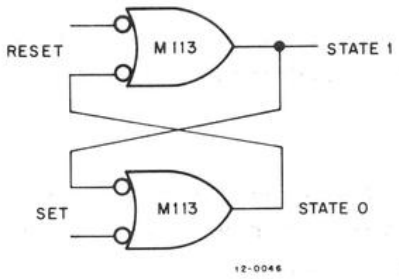


The output of the K124 flip-flop, which has a single output line, is high when both "set" inputs are high. A low at the reset input returns the output to low, provided at least one of the set inputs is also low.





The flip-flop illustrated below is made from two M113 inverting gates. A truth table is also provided for the flip-flop.



Truth Table

Set	Reset	State 1 Output	State 0 Output
0	0	1	1
0	1	1	0
1	0	0	1
1*	1*	No Change	No Change

*Stays in its previous state.

3.2.2.5 **Counters** – The gates (AND, OR, NAND, NOR) and the flip-flop discussed to this point are the basic components required to implement logic functions on the LAB-K. Circuits, designed to perform more complex functions, utilize these basic components. However, regardless of how complex the configuration of a circuit is, the operating principle of individual gates remains the same. A further clarification of Binary and BCD Numbering Systems can be found in Appendix A of this manual.

Counters are used to establish the event interval, or the duration criteria, of a schedule component by counting time or events. There are three types of binary counters used in the LAB-K:

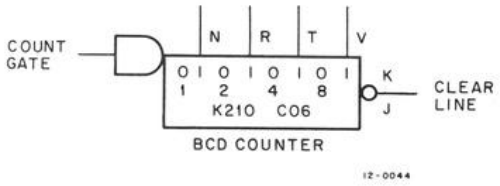
K210	a 4-bit Binary or BCD Counter, used solely for up counting;
K211	a 4-bit Binary Counter (Programmable Divider), used to develop six time bases; and
K220	a 4-bit Up/Down Binary or BCD Counter, which can be used as either the Down Counter or Up Counter.

K210, 4-bit Binary or BCD Counter – Each K210 has 4 bits (flip-flops), each flip-flop representing one bit. The 8,4,2,1 Numbering System (when used as a Binary Counter), can register and hold 15 pulses, with the 16th pulse resulting in 1 pulse out from the last stage. Consequently, all flip-flops return to the 0 state and the clear line goes low (resets).

K210 counts up when the count gate steps from high to low. Every sixteen pulses input to the first stage (flip-flop) produce eight outputs from the first stage: four pulses from the second stage, two pulses from the third stage, and one pulse from the last stage. Thus, each stage divides its input by two, a value assigned to each bit. For a four-stage counter, the values of each successive stage are 8,4,2 and 1, i.e., the first stage is 1, the second is 2, the third is 4, and the fourth is 8. These values enable the user to determine the number of pulses input to the counter. If the input to the 4-bit counter, for example, is 1011, then the count is 11.

1 0 1 1 = 1 1
8+4+2+1 = 1 1

In the diagram below 0 indicates an off condition while 1 indicates an on (or count) condition.

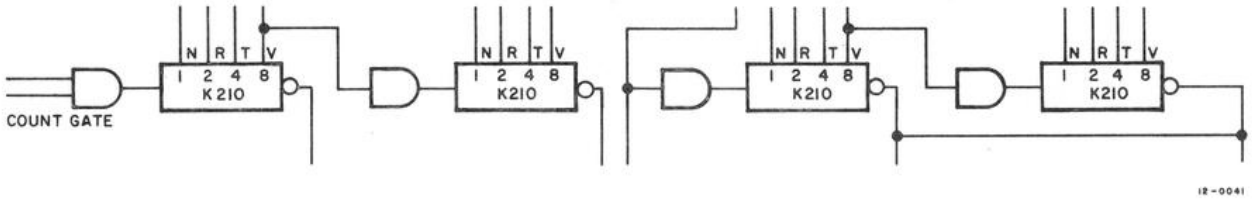


The K210 stores a total of 15 pulses and acts as a Binary Counter when Pin D (on the module) is grounded. The 16th pulse input to the K210, acting in the Binary mode, results in a transfer pulse being output from the counter; thus, all bits reset to the 0 (lower) stage.

In the LAB-K, K210 counters are Binary-Coded-Decimal (BCD) Counters (with Pin D not grounded); the first K210 flip-flop (binary 1) in the counter goes from the 0 state to the 1 state on the first high-to-low transition at the count gate. It then alternates back and forth at each transition. The second flip-flop (binary 2), connected to the 1 side of flip-flop 1, must wait for the 1 state on the first flip-flop to go from high to low, i.e., when the second pulse appears at the count gate. For the same reasons, the third flip-flop (binary 4) must wait four pulses before it goes to the 1 state; and the fourth flip-flop (high on the count of eight) now goes low and transfers a count into the second K210 (BCD Counter) on the count of ten.

Additional 4-bit stages can be added to the first K210 in either the Binary or BCD mode. Three stages (three-bit BCD Counter) function in the same manner as the flip-flops within a single K210. The output of the 4-bit (8) in the first K210 would then be the input to the count gate of the second stage, and the second stage 4-bit output would be input to the third stage. Each successive stage divides the signal present at the output of the previous stage by ten.

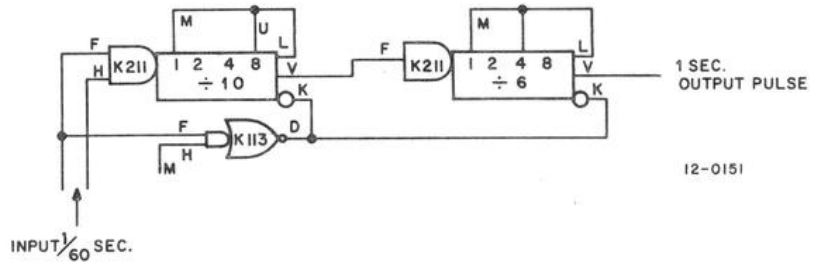
When required, the binary pulse can be interpreted as a decimal number, using the K424 thumbwheel decoder, which compares a BCD number with the thumbwheel number and outputs a coincident signal.



K211 Binary Counter (Programmable Divider) – The K211 Programmable Divider is a counter designed to function as a real-time clock. It operates in the same manner as the K210, but it is prewired to a specific count. The specific count (10 or 6) divides the pulses generated from a clock frequency or a line sync source. The output of the final stage provides a train of pulses that act as a time base.

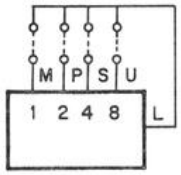
In the LAB-K, a 10 kc (kilocycles) clock is used for Application L, and a 60 cps (cycles per second) line sync is used for Application D.

The K731 line frequency produces high-to-low output transitions at the output line of the K211 count gate. The count gate of Stage 1 produces a pulse every 1/60th of a second. If the latter pulses are divided by ten, only six pulses per second are produced instead of sixty. If the latter six pulses are divided by six, only 1 pulse per second is produced.



In the above diagram, Stage 1 (÷10) of the time generator divides the sixty pulses of the Stage 1 count gate by ten. The output of Stage 1 (pin V) is six pulses per second. These pulses are divided again by Stage 2 (÷6) of the time generator. The output of the above time generator (pin V) is one pulse per second.

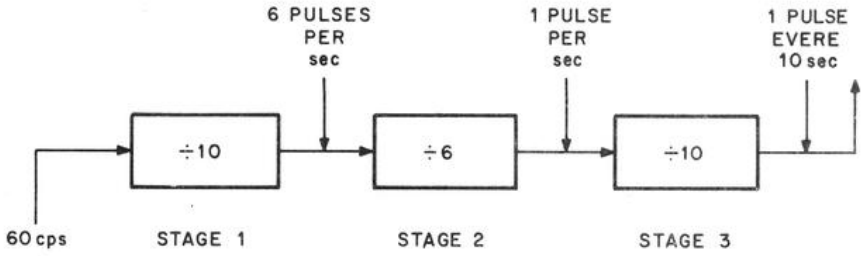
The connection from pin L of the K211 Programmable Divider can be programmed to output on any pulse from two to sixteen. It requires connecting in order that the counter decode a number that is one less than the number of divisions. For example, to divide by two (÷2), remove the connection between pin L and pin S (4) on Stage 2 (shown in the above sketch). This leaves pin L connected to pin M (1), or one less than the number of divisions. If the K211 Divider is connected in the manner described above, the output is 1 pulse every three seconds or a three-sec time base. To get a two-sec time base, divide by 3. (1 second pulses ÷ 5), etc.



12-0081

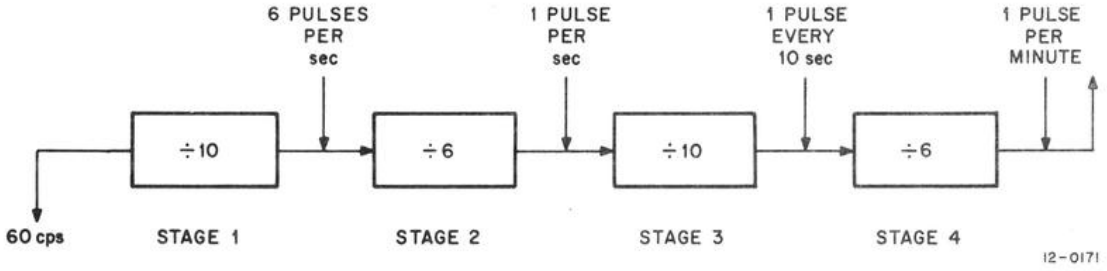
The table below lists some of the wiring changes that produce a new time base.

Divide by		Time Base		
Stage 1, Pin Connection to L		Stage 2, Pin Connection to L		
÷2	M	÷2	M	15 sec
÷2	M	÷3	P	10 sec
÷2	M	÷6	M and S	5 sec
÷5	S	÷3	P	4 sec



12-0170

In the above time generator, a time base other than 10 sec (a 6-sec time base, for example) is produced by rewiring Stage 3 so that it divides by six (connect pin L to pin S and M, which is five, or one less than the number of divisions).



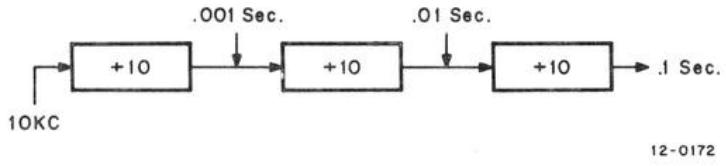
12-0171

In the above time generator, a 40-sec time base is produced by rewiring Stage 4 so that it divides by four (÷4). Connect pin L to pins P and M, which is three, or one less than the number of divisions. Stage 4 divides the 10-sec pulse from Stage 3 four times, and thus, Stage 4 produces a pulse every 40 seconds.

Application L, an option, consists of three time generators. These time generators (constructed with K211 Programmable Dividers) provide .1-sec, .01-sec and .001-sec time bases. The input to the count gate of Stage 1 is provided by a 10 kc clock (M405).

If the 10 kc line frequency is divided by ten (÷10), one pulse per millisecond is produced at the output line (v) of the K211 Programmable Divider, or 1000 pulses per second (1 kc – .001 sec).

By adding a second stage to Stage 1, and wiring it to divide by ten, a .01-sec time base is produced (.001 ÷ 10). A three-stage time generator, in which all three stages divide by 10, produces a .1-sec time base (.01/10).



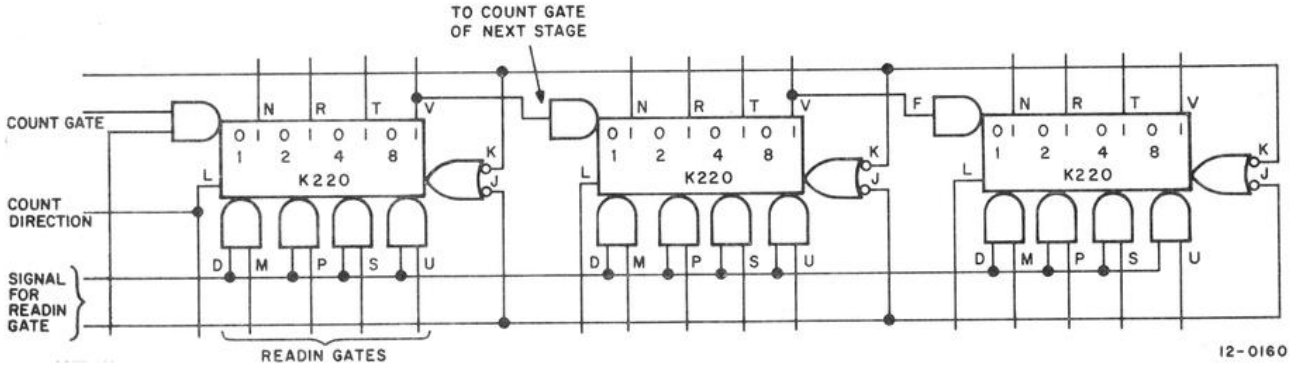
The time generators in Application L are wired for additional time bases in the same manner as Application D. For example, by using one K211 Programmable Divider the time bases shown below can be produced. The following table is not limited to the examples given.

Divide 10 kc by	Pin Connection to L	Time Base
5	S	.0005 sec.
2	M	.0002 sec.

K220 Up/Down Binary or BCD Counter – The K220, in most applications on the LAB-K, will be utilized as a down counter. Because the K220 module can have a number strobed into the counter, it can be used with encoding thumbwheel switches (in counting down to zero from the number in the switches) to determine the length of time or the number of events that remain until the output pulse is initiated.

By using the control line, implemented through the programmable patchboard, the LAB-K user can count up or down with the K220; this feature is important when performing titrations or threshold studies.

The direction of the count is established by a signal at pin L (high for up counting and low for down counting).



Up-counts occur when the output signal of the count gate makes the transition from a high output to a low output, as in the K210. Down-counts, however, take place when the count gate goes from low to high.

The read-in gates contain information (in BCD form) that has been set on thumbwheel switches. For example, if six were to be read into the counter, gates S and P each have one leg high. At the appropriate time, the signal at pin D, which normally sits low, goes high. The signal, from a control flip-flop goes low again in approximately 150 μs and the count begins. The K220, like the K210, consists of interconnected flip-flops; thus, it counts in essentially the same fashion as the K210. The K220 is used in LAB-K as a BCD Counter only.

3.2.2.6 **Power Output Drivers** – The K683 Power driver modules drive external loads through a conductor cable soldered to split lugs at the handle. Logic "0" turns the driver off; logic "1" turns it on.

OUTPUT RATINGS

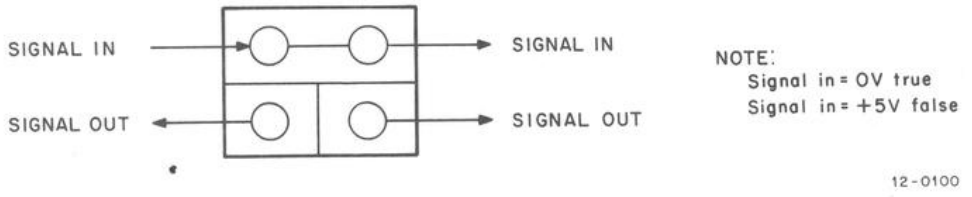
K683	Resistive	Inductive	Typical Incandescent Lamp Loads
	55V, 250 MA	55V, 250 MA with added suppression diodes (K784)	Lamps rated 40 MA to 48V Lamps rated 60 MA to 28V Lamps rated 80 MA to 18V Lamps rated 100 MA to 12V

The K644 DC driver is used with a K782 to obtain the screw terminals needed for connecting heavy duty field wiring. The K644 DC driver permits stepping motors, DC solenoids and similar devices rated up to 2.5 amperes at 48 volts to be driven directly from K-Series logic. Built in clamping diodes protect switching transistors from transient over-voltage.

CHAPTER 4
APPLICATION NOTES

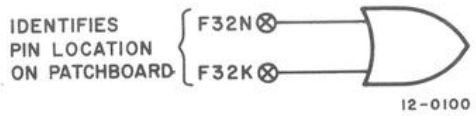
4.1 PLUGBOARD PROGRAMMING

The LAB-K is used to control the functional components of a schedule by means of plugboard programming. Basically, the plugboard is a central terminal point for the control logic housed in the LAB-K cabinet. It affords the researcher a convenient means to utilize the LAB-K logic without having to rewire the logic each time a new experiment is run. The plugboard has 200 logic points that are interconnected with connector plug wires: Logic points on the plugboard are identified by coordinates – L8, B8, etc. Step 0 of the sequencer, for example, is located at L10. Each point on the plugboard is identified and defined on schematic X602-0-6. On this schematic, input and output points are identified as shown below.



The points that are shown "connected" together are used as both input and output points; that is, the signal comes in one "side" and goes out the other. Either side serves as an input or output point. Points that are not shown connected are outputs.

Logic points that have been brought out to the plugboard are identified on all LAB-K schematics as shown below.



This symbol means that the logic point has been brought out to the plugboard. The alphanumeric designation identifies the plugboard pin location on the module mounting rack. Its plugboard coordinate is determined by referring to Table 4-1.

Table 4-1
Plugboard Coordinates

Pin	Coordinate	Pin	Coordinate	Pin	Coordinate	Pin	Coordinate
E29		**F31**		**E30**		**F29**	
E29B	I/J8	F31B	QR6	E30D	J7	F29B	K4
E29D	IJ10	F31D	ST6	E30E	IJ6	F29D	K5
E29E	J9	F31E	QR7	E30F	H10	F29E	L5
E29F	I9	F31F	ST7	E30H	FG10	F29F	L4
E29H	I7	F31H	QR8	E30J	D/E 10	F29H	MN4
E29J	A10	F31J	ST8	E30K	C10	F29J	MN1
E29K	D/E9	F31K	QR9	E30L	A9	F29K	MN2
E29L	B/C9	F31L	ST9	E30M	FG8	F29L	MN3
E29M	FG9	F31M	QR10	E30N	C8	F29M	OP1
E29N	H9	F31N	ST10	E30P	D/E8	F29N	P2
E29P	A8	F31P	L9	E30R	H8	F29P	QR2
E29R	D/E7	F31R	L10	E30S	A7	F29R	QR1
E29S	B/C7	F31S	L8	E30T	H6	F29S	QR3
E29T	FG7	F31T	K7	E30U	FG6	F29T	ST2
E29U	H7	F31U	K10	E30V	C6	F29U	ST1
		F31V	K9			F29V	ST3

F30		**F32**		**E31**		**E32**	
F30B	K2	F32B	LP6	E31B	A4	E32B	DE6
F30D	K1	F32D	N6	E31D	A2	E32D	A5
F30E	K3	F32F	OP7	E31E	BC3	E32E	A1
F30F	L3	F32H	M6	E31F	BC2	E32F	A3
F30H	L1	F32J	OP8	F31H	BC1	E32H	BC4
F30J	L2	F32K	OP9	E31J	DE3	E32J	D4
F30K	O2	F32L	OP10	E31K	DE2	E32K	BC5
F30L	OP3	F32M	MN9	E31L	DE1	E32L	DE5
F30M	OP4	F32N	MN10	E31M	E4	E32M	FG5
F30N	P5	F32P	MN8	E31N	F4	E32N	H5
F30P	QR4	F32R	MN7	E31P	FG1	E32P	GH4
F30R	QR5	F32S	L7	E31R	FG2	E32R	IJ5
F30S	ST5	F32T	L6	E31S	FG3	E32S	I4
F30T	ST4	F32U	K6	E31T	HI1	E32T	J4
F30U	O5	F32V	K7	E31U	HI2	E32U	J3,2
F30V	MN5			E31V	HI3	E32V	J1

To program a functional component, three basic steps are necessary.

1. Identify the component: fix interval, fix ration, variable interval, etc.
2. Define the component: duration, time base, contingencies, etc.
3. Select the LAB-K logic that is necessary to implement the component.

A majority of the material contained in this chapter deals with the subject matter mentioned in Steps 2 and 3. In general, the text contains the following information.

Abstract	An explanation of the Application logic on a functional level.
Programming Points	A list of the plugboard points that are used to control a functional component. This information is present in tabular form.
Contingencies	A list of contingencies that a kit can be programmed to facilitate.
Programming Sample	An example of how a functional component(s) is programmed on the plugboard.
Discussion	An explanation of how the plugboard program controls and implements a functional component.

4.2 APPLICATION A – INPUT LOGIC

The input logic (X602-0-5) contains dry contact switch closures for processing external signals and three spring-loaded toggle switches for setting and resetting the control logic and controlling extinction.

NOTE

The schematics for each logic kit are located in Chapter 6.

External signal sources are wired to a terminal board (K782) located in the output mounting rack. The external signals are referred to as left and right events. The left event is wired to terminal 7, and the right event is wired to terminal 8. These terminal points are connected, via the K782 module, to two dry contact switches located in the Input Logic. Each of the latter dry contact switches is connected to a Schmitt trigger, which triggers a one-shot if an event occurs. Since the output signal of a one-shot is only on for a predetermined period, the organism's holding time has no effect on the duration of the event signal once it has been generated. The response lever must be released before another event signal can be generated.

There are six additional contact switches in the Input Logic which are available to the researcher. If the switches are needed, they can be directly connected to the leg of a logic gate. If they are used with a one shot, then the signal must be conditioned by a Schmitt trigger (see Chapter 3, Building Blocks).

4.2.1 Control Switches

The three toggle switches (Figure 4-1) are designated as MASTER RESET, SYSTEM ON, and SPARE.

MASTER RESET is used to reset all of the counters and flip-flops contained in the LAB-K; thus, it ensures that the starting point of an experiment is accurate. MASTER RESET is set to ON at the beginning of every experiment by momentarily depressing the toggle switch (see illustration below).

SYSTEM ON is used to logically enable the event signals (left or right) to enter the LAB-K system (the event signals are ANDed with SYSTEM ON). SYSTEM ON also enables the time generators (kits D and/or L).

SPARE (user applied)

To control an experiment with the LAB-K, the following preliminary steps are necessary.

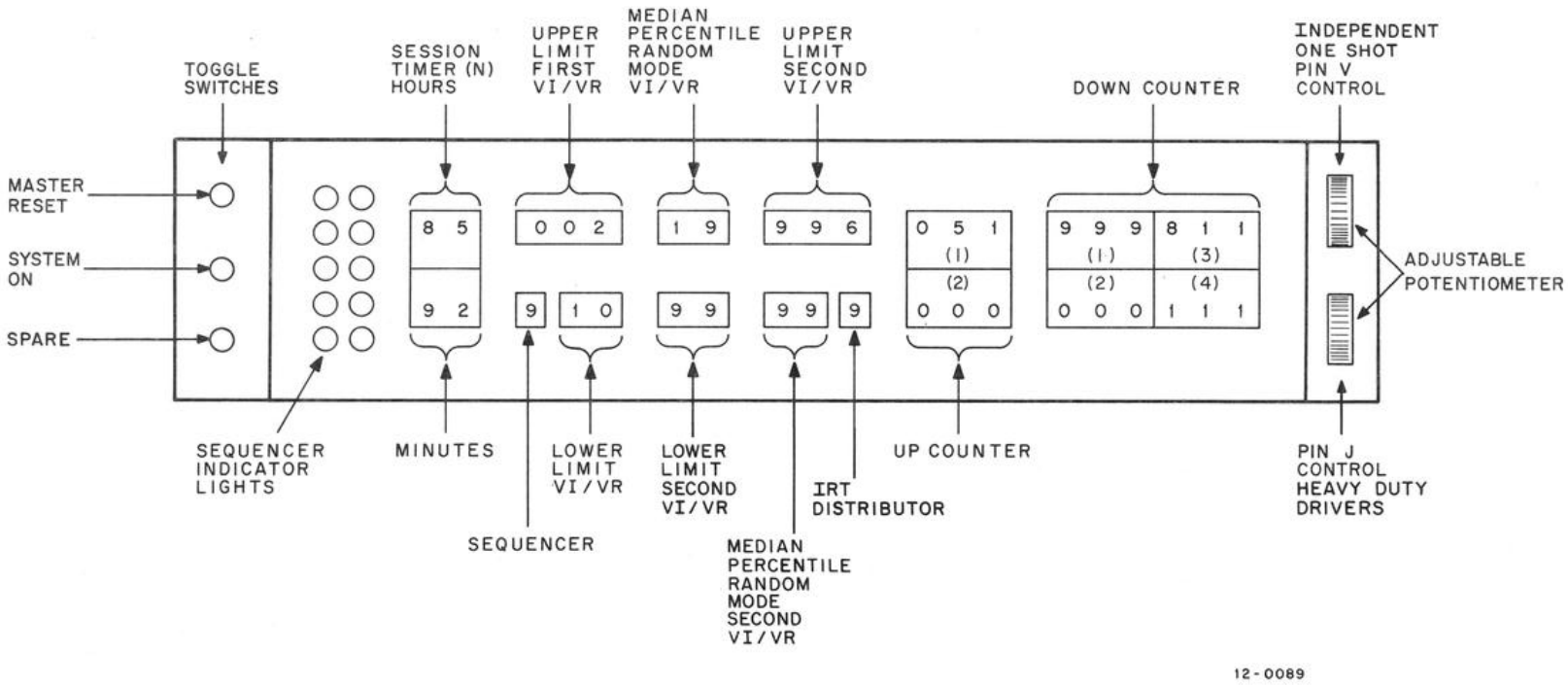


Figure 4-1 Front Panel Indicators and Controls

1. MASTER RESET is momentarily depressed (ON position).
2. Then, and only after MASTER RESET has been momentarily depressed, SYSTEM ON is momentarily depressed (ON position).

NOTE

Steps 1 and 2 are performed prior to the implementation of any plugboard program.

Lock-in Position, NOT USED (OFF) Spring-Loaded (momentarily ON)	MASTER RESET
Lock-in Position, NOT USED (OFF) Spring-Loaded (momentarily ON)	SYSTEM ON
Locked-in (ON) (OFF)	SPARE (user applied)

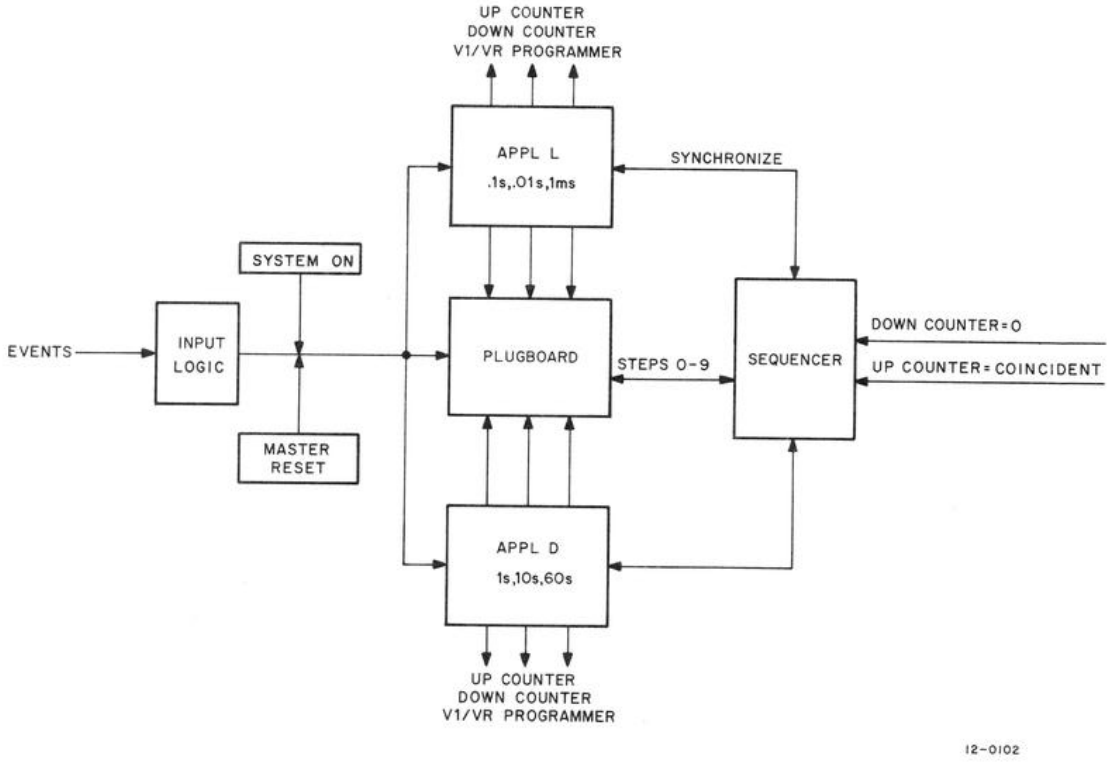


Figure 4-2 Flow Diagram of Manual Control, Input and Timing

4.3 APPLICATIONS D AND L – TIMING KITS

4.3.1 Application D

Application D consists of a 60 kc line Sync (K731) generator and three sets of programmable dividers (K211 – see Building Block section for description). This kit provides three time bases – 1 sec, 10 sec, and 60 sec. All three time bases are hard-wired (permanently wired) to the down counter and up counter*. If the VI/VR programmer option is used, the 1 sec and 10 sec time base are hard-wired to this kit.

The time bases which are hard-wired to the counters are also brought out to the plugboard (enable 1 sec to down counter, etc.). A time base is enabled into a counter by a step on the sequencer.

A timing kit provides time bases which are used where time durations are needed in experiments. The pulses generated by a kit are used to step the down counter from a maximum count of 999 to zero and the up counter from zero to a maximum count of 999.

Patchboard resets have been provided for each timer that will provide accurate time correlation for any time related action. (Pulse required – hi to lo transition.)

4.3.2 Application L

Application L, an option, consists of a 10 kc crystal clock (M405) and three sets of programmable dividers. This kit consists of three time bases: 0.1 sec, .01 sec, and .001 sec. All three time bases are hard-wired to the down counter and up counter, and they are also brought out to the plugboard. If the VI/VR programmer is used, then the 0.1 sec time base is hard-wired to this kit.

This timing kit is used in the same manner as Application D. Both timing kits are synchronized whenever the sequencer is stepped. This ensures the accuracy of the first time pulse.

***NOTE**

See Chapter 3, Section 3.2.2.5, for discussion on modifying the K211 programmable dividers for various time bases.

Patchboard resets have been provided for each timer that will provide accurate time correlation for any time related action. (Pulse required – hi to lo transition.)

4.4 APPLICATION B – 0–9 SEQUENCER

The 0–9 sequencer is a ten-position stepper which acts as the "Executive Director" of an experiment by sequentially enabling most of the functional components of the logic at intervals that are contingent upon time and/or events. It controls simple one component or complex multiple component schedules. The sequencer is also used to synchronize the timing generators at the completion of each sequencer step.

Application B consists of logic gates, a BCD counter (K210), a decoder (K161), and a thumbwheel switch (K424) (Figure 4-3).

The sequencer is stepped by a signal from either the down counter or the up counter (both counters count time or events). The researcher predetermines which of these two counters is going to step the sequencer at the termination of the preselected time or event.

Two groups of logic gates (K113) are used to control the stepping of the sequencer when the Down Counter reaches zero, or when a count is decoded in the Up Counter. Both groups of logic gates are enabled by a sequencer step. One logic gate (4 legs) is used to step the sequencer when the Down Counter reaches zero from a predetermined number. The legs of this gate, which are called Down Counter control legs (1–4), are represented on the plugboard at coordinates MN7 through MN10.

The Down Counter control gate is used when the Down Counter is being used to time the duration of an Up Counter component. Since the control gate has four input legs (control legs), it can be used on four separate sequencer steps.

A signal line from the Down Counter is permanently wired (hard-wired) to the latter control gate, and it goes high when the Down Counter reaches zero. If the Down Counter control gate is enabled (one leg sitting low) by a sequencer step, then the Down Counter to zero line steps the BCD counter, which causes the sequencer to step.

The BCD counter (K210) is stepped whenever the output of its count gate goes from high to low. This transition occurs if the Down Counter control gate is true and the Down Counter is at zero; or the Up Counter control gate is true and the count is decoded in the Up Counter.

The other logic gate (5 legs) steps the sequencer when a count is decoded in the Up Counter. The legs of this gate, called Up Counter control legs (1–5), are represented on the plugboard at coordinates OP6 through OP10. The Up Counter control legs are connected to a step on the sequencer via the patchboard.

The Up Counter control gate operates when the Up Counter is used to time the duration of a Down Counter component. It can be used on five separate sequencer steps.

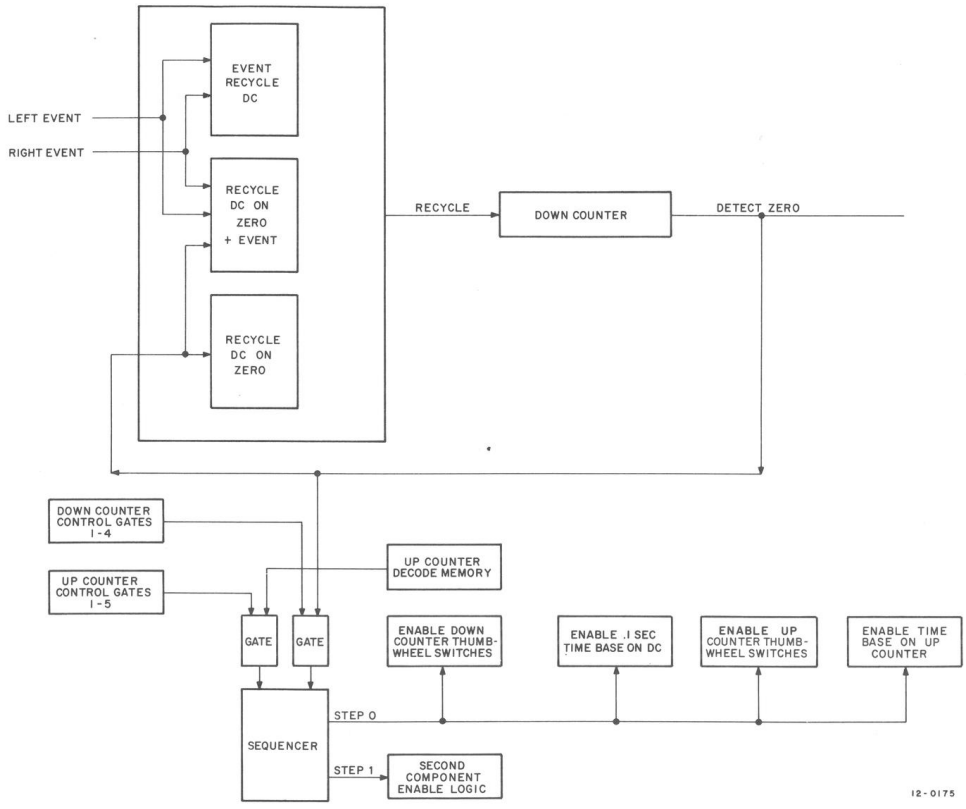


Figure 4-3 Logic Gates of Application B

A signal line from the Up Counter is hard-wired to the control gate. This line goes high when a count is detected in the Up Counter. If one of the Up Counter control legs (1–5) is sitting low (control step is true), and the preselected count is detected in the Up Counter, the BCD counter is stepped, and subsequently the sequencer.

The K161 decoder (see Building Blocks) has seven output lines (see Figure 4-3) that normally sit low. The output signals, however, are inverted (K134) and brought out to the plugboard, indicating that the sequencer plugboard points normally sit high when in the off condition. The seven K161 decoder output lines represent Steps 0 through 7.

When any count from 0 to 7 is present in the BCD counter, the K161 output line (which represents the number present in the counter) goes from low to high. The latter signal is inverted and the equivalent plugboard point goes from high to low. At any given time, only one sequencer step on the plugboard is low.

Steps 8 and 9 are brought out to the plugboard from two K113 gates. These plugboard points normally sit high. They go from high to low when the numbers they represent are present in the BCD counter.

The LAB-K logic, necessary to control the component of an experiment, is connected to one of the sequencer steps (0 through 9). The control logic connected to a sequencer step is enabled when the sequencer step goes from high to low.

For example, in an experiment consisting of four components, sequencer Steps 0–3 are used to control the four components. All the control logic necessary to implement component one is connected to Step 0, and the logic for component 2 is connected to Step 1, etc. The duration of each component is timed on the Down Counter or Up Counter, which in turn steps the sequencer and enables the next component (see Figure 4-4).

NOTE

The components of an experiment are executed in succession by the sequencer. It is not possible to program a schedule that permits the sequencer to skip steps. For example, it is not possible to go directly from Step 1 to Step 4, or vice versa.

The sequencer thumbwheel switch (Figure 4-1) is used when it becomes necessary to repeat a schedule. If a schedule consists of five components (0,1,2,3,4), setting four on the sequencer thumbwheel switch causes the BCD counter to reset to zero at the completion of the fifth component. As a result, all five components are implemented again.

CAUTION

If you do not want to repeat a schedule, the sequencer thumbwheel switch must be set one number higher than the number of components. For example, if a schedule consists of three steps (0–2), the thumbwheel switch must be set on 3, or higher. To repeat the schedule, set the switch on 2.

Figure 4-4, a block diagram, shows how the sequencer enables and controls the components of an experiment. In this diagram, the thumbwheel switches, time base, contingency gates, etc., represent the control logic used to implement a functional component such as a Fixed Interval. The logic points connected to a step on the sequencer (Step 0 in this case) are enabled when a step is true (goes low). As a result, the number set on the thumbwheel switch is set into the Down Counter, a time base is enabled into the Down Counter, and one of the Down Counter contingency gates (see Section 4.5) is enabled.

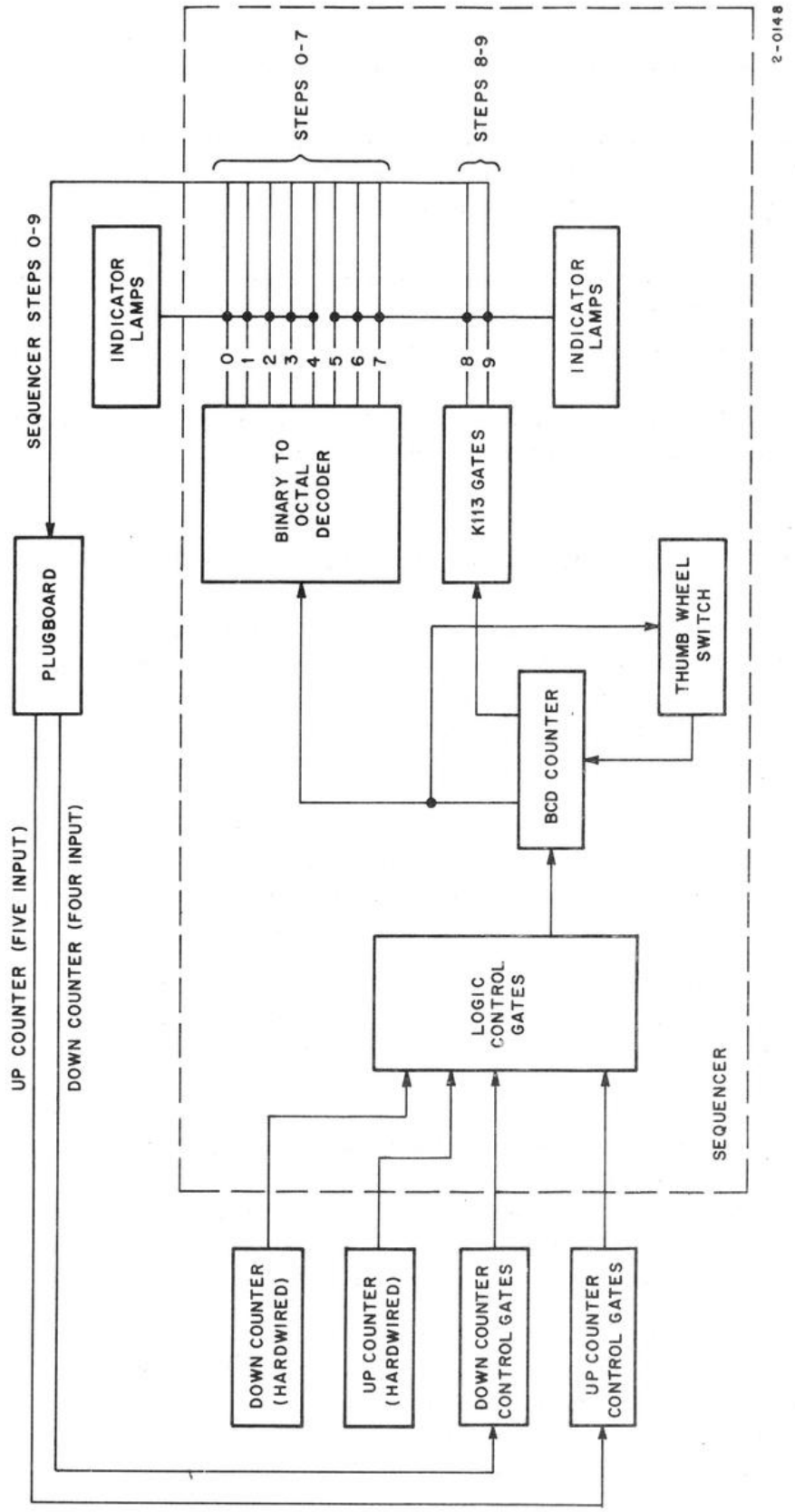


Figure 4-4 Sequencer Control Flow Chart

The Up Counter control gate is also enabled. The sequencer steps from Step 0 to Step 1 when the programmed contingency criteria is satisfied, and when the up count is detected in the Up Counter. Step 1 enables the control logic of the second component.

In the previous example, the Down Counter is used to time the Fixed Interval, and the Up Counter is used to time the duration of the component.

4.5 APPLICATION C – DOWN COUNTER

The Down Counter (schematic X602-0-3) is used to count fixed intervals and events; therefore, it is used to control the following types of components: fixed ratio, fixed interval, conjunctive FI/FR, threshold and titration, and avoidance.

Events and intervals are counted on the Down Counter by setting the number of events to be counted, or an interval limit, on one of the thumbwheel groups. The number set on the thumbwheel switch group is set into the Down Counter when the thumbwheel switch group is enabled by a sequencer step. On the same step, the time base or event signal, which steps the Down Counter to zero, is also enabled into the Down Counter. If the Up Counter is being used to time the duration of the Down Counter component, the sequencer step enables the Up Counter thumbwheel switch group and a time base into the Up Counter. The sequencer step also enables the contingency gates.

Four groups of thumbwheel switches (Figure 4-1) are assigned to the Down Counter (two groups are optional). A thumbwheel group can accommodate any three-digit number. If all four groups of thumbwheel switches are available, then four distinct three-digit numbers can be set into the Down Counter on separate sequencer steps.

The Down Counter is stepped down to zero by either event signals or clock pulses. Clock pulses are produced by time generators (Application D or L), and are enabled into the Down Counter by a step on sequencer. Clock pulses step the counter, which contains a number that is set in from a thumbwheel group, to zero. Event signals, input to the LAB-K through a terminal module (K782) at the input/output panel, step the Down Counter to zero in the same manner as the clock pulses (see Down Counter Programming Points).

When the Down Counter is stepped to zero, it is usually programmed to facilitate one of two contingencies: Down Counter on zero or Down Counter on zero plus an event. The Down Counter is recycled if either of the latter contingencies occur. The latter contingencies are programmed by utilizing the contingency control gates located in the Down Counter logic, and they are used in Fixed Interval and Fixed Ratio type schedules. The contingency gates provide the ability to recycle the Down Counter and turn the LAB-K drivers on if a given criteria is met.

4.5.1 Down Counter on Zero Plus Event

The Down Counter on Zero Plus Event control gate (Figure 4-5) has three input legs, which are brought out to the plugboard. Any one of the input legs can be enabled on any three sequencer steps.

The output line of the contingency gate is connected to leg B of a two-legged AND gate. Leg A of the gate is connected to a logic gate whose input legs are enabled by an event signal and the zero detected signal. Normally, both input legs of the two-legged AND gate sit low; consequently, the output line is low. When the Down Counter on Zero Plus Event contingency

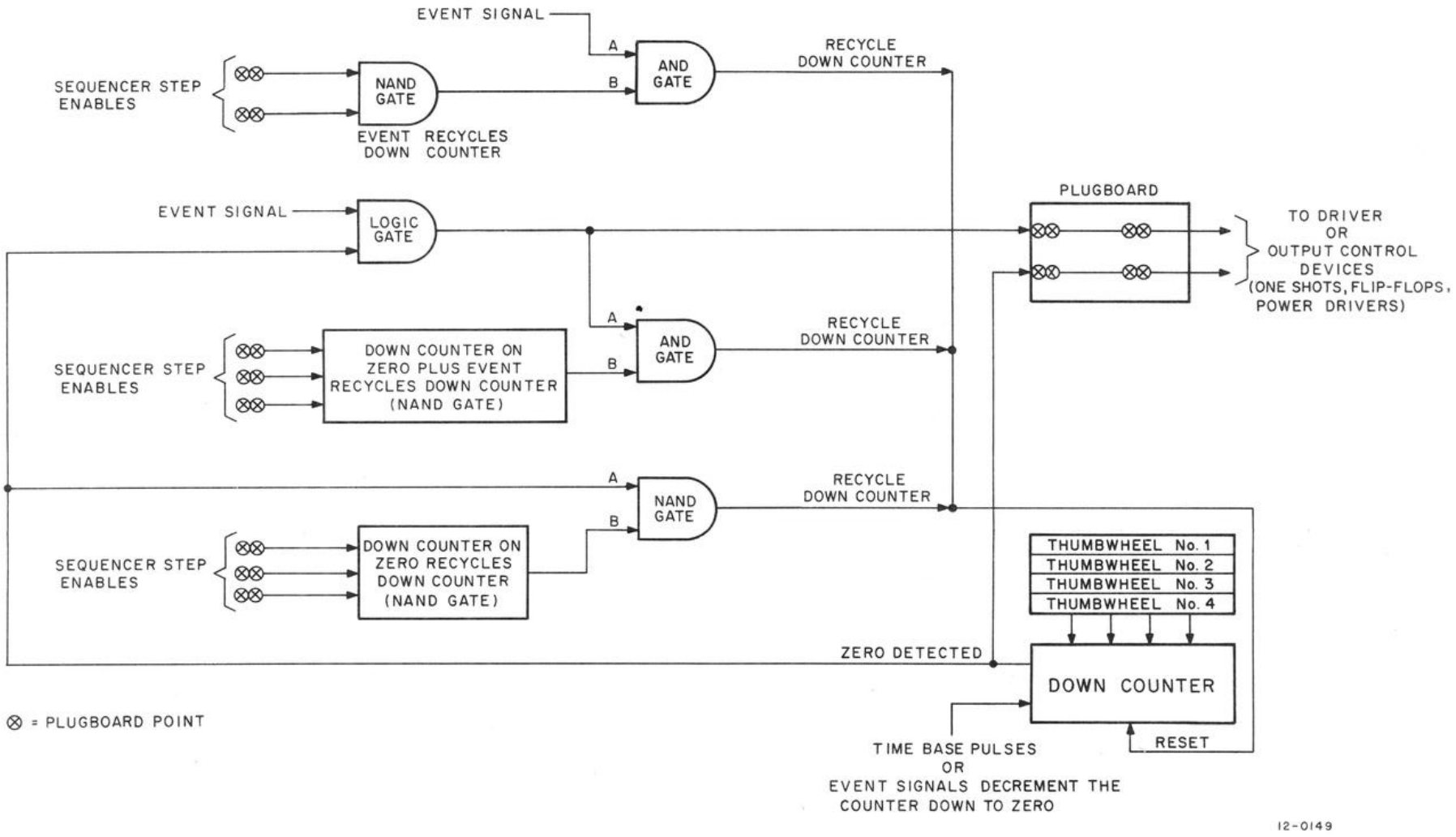


Figure 4-5 Down Counter Control Flow Chart

control gate goes high, leg B of the two-legged AND gate goes high, but the output of the gate remains low. If the Down Counter is at zero and an event occurs, then leg A of the two-legged AND gate goes high. Because both legs of the AND gate are high, its output goes high (A·B = C). The output eventually results in a recycling of the Down Counter.

Thus, the purpose of the Down Counter on Zero Plus Event contingency control gate is to recycle the Down Counter when the Down Counter is zero and an event occurs.

The output of the Detect Zero Plus Event gate is brought out to the plugboard. When it becomes necessary to turn a driver on, the output of the gate is connected to an input leg of a driver one-shot which is also brought to the plugboard. After the Down Counter reaches zero, the first event that occurs turns the driver on.

4.5.2 **Down Counter on Zero**

The Down Counter on Zero recycles the Down Counter contingency control gate. The control gate has three input legs, which are brought out to the plugboard, and it can be enabled by the sequencer on any one of three separate steps.

The output of this control gate goes true (Figure 4-5), if one of its control legs is connected to the sequencer step that is true. This output is connected to leg B of a two-legged NAND gate. Leg A of the latter gate is connected to the ZERO DETECTED line, which is connected to the Down Counter output. The output of the two-legged NAND gate remains high until both its input legs are high. Leg B can go high when the sequencer steps, and leg A goes high when zero is detected in the Down Counter. If there is a number in the Down Counter, the detect zero output sits low.

The ZERO DETECTED signal is not brought to the plugboard from the contingency control gate, instead the signal comes from a separate gate. The ZERO DETECTED output point on the plugboard normally sits high and goes low when the Down Counter reaches zero. If it becomes necessary to turn a driver on, when the Down Counter reaches zero the ZERO DETECTED output is connected to the input leg of any one of a number of drivers.

If it is desirable to reset the Down Counter whenever an event occurs, the Event Recycles Down Counter contingency control gate is used. When this gate is enabled by a sequencer step (it can be enabled on two separate steps), a response signal resets the Down Counter. This gate is used in avoidance type schedules where the organism is reinforced if a predetermined period of time elapses without a response occurring. Thus, reinforcement is provided when the Down Counter reaches zero (see contingencies).

4.6 DOWN COUNTER PROGRAMMING POINTS

The following LAB-K logic is used to control Down Counter components. The points listed below are enabled by connecting them to a sequencer step.

1. Down Counter Thumbwheel Switch Group

Thumbwheel	Plugboard Coordinates	Schematic Designator	Drawing
1	FG10	E30H	X602-0-3
2	FG9	E29M	X602-0-3
3	FG8	E30M	X602-0-3
4	FG7	E29T	X602-0-3

2. Time base and/or event output to Down Counter

Time Base	Plugboard Coordinates	Schematic Designator	Drawing
60 sec	BC1	E31H	X602-0-3
10 sec	BC2	E31F	X603-0-3
1 sec	BC3	E31E	X602-0-3
.1 sec	BC6	E30V	X602-0-3
.01 sec	BC7	E29S	X602-0-3
.001 sec	BC8	E30N	X602-0-3
Event			
Left Event	BC4	E32H	X602-0-3
Right Event	BC5	E32K	X602-0-3

3. Down Counter on Zero steps the sequencer. These control points are used when the Down Counter is being used to time the duration of a component; that is, a component being run on the Up Counter.

Control Step 1	MN10	F32N	X602-0-9
Control Step 2	MN9	F32M	(APPL B)
Control Step 3	MN8	F32P	
Control Step 4	MN7	F32R	

4.7 CONTINGENCY GATES

The Down Counter is recycled if any of the following events occur:

a. Response Occurs

	Plugboard Coordinates	Schematic Designator	Drawing
	BC9	E29L	X602-0-3
	BC10	E30K	X602-0-3

b. Down Counter on Zero

Control Step 1	DE3	E31J	X602-0-3
Control Step 2	DE2	E31K	X602-0-3
Control Step 3	DE1	E31L	X602-0-3

c. Down Counter on Zero Plus Event

Control Step 1	FG3	E31S	X602-0-3
Control Step 2	FG2	E31R	X602-0-3
Control Step 3	FG1	E31P	X602-0-3

NOTE

A control step represents the input of a logic gate. If a logic gate has three inputs (control steps), then the logic gate can be used on three separate sequencer steps.

4.8 APPLICATION E – UP COUNTER

The Up Counter is normally used to determine the duration of a fixed component; that is, it determines the duration of a Down Counter component. It is also used for the upper limit of a VI/VR component or, when it is not being used with the Down Counter, for a lower limit of an IRT component. If the Up Counter is being used to time a Down Counter component, then it cannot be used with the VI/VR or IRT kits at the same time.

The duration of an Up Counter interval, when used with either the VI/VR or the IRT kits, is timed on the Down Counter. The Up Counter logic consists of a BCD Up Counter (K210) and the thumbwheel decoders (K424).

The thumbwheel switches are used to decode predetermined numbers. When a thumbwheel switch decodes an up count, its output is ANDed with the output of the Up Counter control gate – the resulting output causes the sequencer to step.

There are five Up Counter control gates in the sequencer logic. Thus the Up Counter can be used to step the sequencer on any five sequencer steps.

The BCD counter is stepped up (see Building Blocks) by time pulses from one of the time generators, or by event signals from an external source. Both the time bases and the event signals are enabled into the Up Counter by a sequencer step via the plugboard connections.

If the Up Counter is used to time the duration of a Down Counter component, it is enabled by connecting the pertinent logic points to the Down Counter chain, which originate from a sequencer step; i.e., the duration is set on an Up Counter thumbwheel switch group, a time base is enabled into the Up Counter, the Up Counter thumbwheel switch is enabled, and the Up Counter sequencer control gate is enabled. When the up count is detected, the sequencer is stepped.

4.8.1 Up Counter Programming Points

1. Up Counter thumbwheel switch group

Thumbwheel	Plugboard Coordinates	Schematic Designator	Drawing
2	QR1	F29R	X602-0-7
1	OP1	F29M	X602-0-7

2. Enable time base to Up Counter

Time Base	Plugboard Coordinates	Schematic Designator	Drawing
60 sec	QR2	F29P	X602-0-7
10 sec	QR3	F29S	X602-0-7
1 sec	QR4	F30P	X602-0-7
.1 sec	QR5	F30R	X602-0-7
.01 sec	QR6	F31B	X602-0-7
1 ms	QR7	F31E	X602-0-7

4.8.2 Contingency Gates

1. Up Counter Steps Sequencer when count is decoded

	Plugboard Coordinates	Schematic Designator	Drawing
Control Step 1	OP10	F32L	X602-0-9
Control Step 2	OP9	F32K	X602-0-9
Control Step 3	OP8	F32J	X602-0-9
Control Step 4	OP7	F32F	X602-0-9
Control Step 5	OP6	F32B	X602-0-9

2. Set memory for Up Counter (or VR)

P2	F29N	X602-0-7

3. $\overline{\text{Set}}$ memory for Up Counter (or VR)

O2	F30K	X602-0-7

4.9 APPLICATION M – VI/VR PROGRAMMER

The VI/VR Programmer is used to run variable interval or variable ratio in a pseudo random mode; for example, experiments where the researcher does not want the subject to anticipate a time period, or the number of responses required for reinforcement.

The VI/VR Programmer is used to determine:

a. The lower limit of a variable interval or variable ratio,

b. The percentile setting for a median variable interval or the variable ratio,

c. The upper limit of a variable interval or variable ratio.

There are only three time bases available for VI programs: 0.1 sec, 1 sec, and 10 sec. If a time base having an accuracy greater than a tenth of a second is used, the VI/VR programmer will not work. Either the left or right event signals can be used for variable ratio programs.

The interval and response gates are connected to the count gate of a two-stage BCD Up Counter; the BCD Up Counter serves as a lower limit counter (Figure 4-1). The output of this counter is decoded by two thumbwheel switches. The decoded output triggers a one-shot (M302), which is connected to a logic gate. The other leg of the latter logic gate is also connected to a one-shot, which is triggered by a 6 kc clock (pseudo-random generator). The 6 kc clock continuously steps a two-stage BCD counter. The output of this counter is decoded by two thumbwheel switches. It is this output that is connected to the one-shot mentioned above.

If the lower limit one-shot and the 6 kc clock one-shot outputs (50 ns) coincide, then the output of the logic gate triggers a one-shot which subsequently sets a memory flip-flop. When the memory flip-flop is set, the variable interval or variable ratio condition has been met and, in the case of the variable ratio, reinforcement is immediate; however, in the case of the variable interval, the next response provides reinforcement.

4.10 IRT DISTRIBUTOR

The IRT Distributor is used to determine the distribution of events in time. The IRT logic divides events into ten classes or bins. A bin width is represented by a position on a ten-stage ring counter, which consists of ten logic gates. The bin width is established by using a standard time base and/or in combination with the Up or Down Counter (distribution can also be refined on the IRT). The ten logic gates are connected to output drivers, which are routed to output terminal connectors which will be connected to external electronic or mechanical decimal counters.

In general, the IRT Distributor operates as follows. A bin width is established by enabling a time base into a BCD counter. For example, if a 1 sec time base is enabled into the IRT BCD counter, then the bin width is 10 sec. Each bin gate represents 1 sec, beginning with bin gate 1, which represents 1 sec, to bin gate 10, which represents 10 sec.

The counter output is decoded, and the decoded output, when true (H), enables one leg of a bin gate. The normal output line of the event one-shot is connected to the other input leg on each bin gate. If an event occurs, the normal output of the one-shot goes high and causes the output of any bin gate whose decoder leg is high to go from low to high. A high level turns a driver on. The IRT counter is reset whenever an event occurs.

4.10.1 IRT Distributor Programming Points

1. IRT thumbwheel switch (only used if the number of bins is less than 10).

	Plugboard Coordinates	Schematic Designator	Drawing
	J9 to reset I9	E29E	X602-0-4

2. Time and/or event input to IRT Distributor.

Time Base	IJ5	E32R	X602-0-4
Event Input	IJ8	E29B	X602-0-4

3. Step (sequencer) or Up Counter enable IRT Distributor.

IJ6	E30E	X602-0-4

4.11 SESSION TIMERS – OPTIONS N1 AND N2

The N1 option is a Session Timer that can count up to 9 hours and 59 minutes. It can also be used to count events. The unit consists of three BCD Up Counters (K210) and two groups of thumbwheel switches (K424) (Figure 4-1).

The BCD counters are stepped by a 60 sec time base, which is hard-wired into the logic. When the Session Timer is being used, the 60 sec pulses are input to the counters when the SYSTEM ON toggle is turned on. The count continues until the number set on the thumbwheel switch is decoded. For example, if 532 is set on the thumbwheel switch, then after 5 hours and 32 minutes, the output of the thumbwheel switches goes from low to high. This output point is connected to a point on the plugboard – Session Terminated. To shut the system down, the researcher simply connects the latter point to auto reset, which is connected to the reset side of the SYSTEM ON flip-flop.

If it is necessary to use a time base other than 60 seconds, the 60 sec connection must be disconnected from the BCD count gate and replaced by a connection from the desired time base.

The Session Timer can be expanded for counts up to 99 hours and 59 minutes by adding a fourth counter to the three BCD counters. This configuration represents the N2 option. Nixie tube readouts are available for both the N1 and N2 options.

The Session Timer can be modified and used for counting events. A researcher in operant work, for example, may want to limit the number of shocks that an animal or subject acquires, i.e., after X number of shocks he wants to terminate the schedule. Each time the organism received a shock, a count would go into the BCD counter. The counter thumbwheel switches are set so that the desired number is decoded.

To use the Session Counter for counting events, the time base connection must be removed from the count gate of the BCD counter. This connection is replaced by a connection from the normal output side of a driver one-shot in Application F. For example, the input to Heavy Duty Driver No. 4, Application F, is connected to a one-shot located in row F, slot 27 of the module mounting rack. To count the number of reinforcements provided, the normal output of the one-shot, which is on pin E of slot 27, is connected to pin H, slot 4, row B, which is where the count gate of the Session Timer is located. When reinforcement is provided, the one-shot is fired, and its normal output goes high, which turns a driver on. Since the normal output is connected to the BCD count gate in the Session Timer, it is stepped by one each time reinforcement is provided.

The Session counter can also be used for counting positive reinforcements. If, for example, the researcher only wants to run the animal until he receives 300 pellets, he can connect the driver one-shot to the Session Counter as described above. This allows him to terminate the schedule when the subject has received 300 pellets.

The Session Timer can also be used for criteria type experiments. For instance, if a subject is trying to learn a concept, and the criteria consists of correctly identifying the concept 50 times, the Session Counter terminates the schedule after the subject has correctly identified the concept 50 times.

This type of experiment is configured by wiring the response mechanism to either the left or right event terminals located in the input logic (Application A). The event pin (A4 or A7) is connected to the count gate of the Session Timer. Thus, F17D or F17K is connected to B4H. The time base wire must be disconnected from B4H.

4.12 COMPUTER INTERFACED BLOCK ON THE X602

Some LAB-K users will desire to incorporate computer control into their research. For these researchers, the X602 Computer Interfaced Block provides an outlet to which an interface can be readily connected to control the use of logic and the sequence of events in experiments.

In normal operation, the LAB-K Sequencer acts as the Executive for the controller kit. It determines what logic functions are to be executed, in what time frame, and in what sequence. When the LAB-K is interfaced to a computer, it is the computer software that takes over the sequencer's function and gives the researcher added flexibility in program control and scheduling. In such an experimental setup, the LAB-K would be used to set up the experimental parameters, classroom trainer, training a subject, and, in addition, to act as a backup system for the computer during the data acquisition process.

The interface between the LAB-K and the computer is the subject of a special LAB-K Application Note which is available on request from Digital Equipment Corporation.

CHAPTER 5
CHECKOUT PROCEDURES

5.1 GENERAL DESCRIPTION

The checkout procedures contained in this chapter are a guide for the checkout of a completed LAB-K Logic Controller Kit. This chapter also includes troubleshooting procedures used when setting up experiments on LAB-K.

To utilize the checkout procedures fully, the user must have an adequate understanding of LAB-K logic.

Each LAB-K Application Kit comprises functional sections whose operation can be fully checked out (in most cases) by testing the appropriate logic gates with a Multimeter or K791 Test Probe.

Logic elements are usually checked by ensuring that the appropriate voltage level is enabling the logic gate. The voltage levels that enable a logic element are generally tabulated in a truth table (showing the binary relationships between the input and output signals). All possible combinations of inputs are entered in the truth table, and the resultant binary output is listed adjacent to the input combinations. The truth table enables the user to determine the binary output of a logic element for any input combination. For example, the input combinations for an AND gate are as follows:

Input			Output
A	B		C
0	1	=	0
1	0	=	0
0	0	=	0
1	1	=	1

By examining the AND gate truth table, it is determined that if both input legs are in the binary 1 state (in the LAB-K, binary 1 has been assigned a +5V or "high" value), then the output is binary 1 (+5V, or "high"). But when one or both input legs is in the binary 0 state (+0V, or "low"), then the output is binary 0.

If an AND gate is used to perform a logic function that requires a low signal, the gate is enabled when a low (0) voltage level is present at one or both of its input legs. The gate is inhibited if both its input legs are sitting high.

Conversely, if an AND gate is used to perform a logic function that requires a high signal, the gate is enabled when both input legs are high. The gate is inhibited when either of its input legs is low. Truth tables for all the logic gates used in the LAB-K are located in Chapter 3.

Electrical checks can be made with a Multimeter, a K791 probe, or an oscilloscope. If possible, it is recommended that the K791 probe be used. This probe is equipped with two indicator lights that indicate the presence of a high or low signal when it is connected to an input or output line.

The procedure for setting and checking a one-shot is located at the conclusion of this chapter.

5.2 CHECKOUT PROCEDURES

The logic modules used for each Logic Application in the LAB-K are identified in Table 5-1. The correct module slot for each module is determined by referring to the module utilization (MU) drawing (X602-0-10).

CAUTION

The slots in the MU drawing are numbered from the wiring side, i.e., the pin side of the connector block. When plugging modules into the rack, slot 1 is located on the right-hand side of the rack and slot 32 is on the left-hand side.

Before plugging any modules into the rack, the dc and ac checks must be made.

5.2.1 DC Checks

Test Equipment: Multimeter, used on the Ohmmeter range.

NOTE

Do not turn the power on until the dc checks 1, 2, and 3 are completed.

The user should check the continuity of bus connection and ensure that the +5V bus is not shorted to ground.

Step	Procedure
1	Check continuity on the +0V bus (C).

( ) a. Connect the first Multimeter probe to one of the terminal lugs located on the H020 mounting bar. The mounting bar is connected to the ground pins (C) of the power supply.

( ) b. Touch the second Multimeter probe to pin C in the following locations:

Row	Slot
A	1
B	1
C	5
D	5
E	2
F	2

Step	Procedure
1 (cont)	When the Multimeter probe is touched to each of the above pins, the indicator deflects across the face of the meter to zero ohms (full-scale deflection).
	If there is not a full-scale deflection, check for a break in the bus chain or faulty soldering.
2	Check for continuity on the +5V bus (A).
	( ) a. Connect one Multimeter probe to pin A, row B, and touch the other probe to pin A, slot 1, in rows A and B.
	If there is not a full-scale deflection, check for a break in the bus chain or faulty soldering.
	( ) b. Connect one Multimeter probe to pin A, row D, and touch the other probe to pin A, slot 5, rows C and D.
	( ) c. Connect one Multimeter probe to pin A, row F, and touch the other probe to pin A_2, slot 2, rows E and F.
3	Check to ensure the +5V bus is not short-circuited to the chassis (ground).
	( ) a. Connect one Multimeter probe to the LAB-K cabinet, and touch the other probe to pin A, slot 32, rows A, C, and E.
	The Multimeter indicator should not deflect fully to zero ohms. If there is a full-scale deflection (zero resistance 0Ω), then there is a short. This indicates that pins A (+5) and C (ground) are connected together. The faulty pin connection(s) must be located and corrected. This check is performed by examining each individual A pin (or C) in the row in which the full-scale deflection occurred. One Multimeter probe is connected to the cabinet frame, and the other probe is used to check each A pin. If a full-scale deflection occurs when any A pin is touched, then the pin is improperly connected to a C pin (ground).
4	Turn the power on. Check the +5V bus to ensure that +5V is present.
	( ) a. Connect the negative (-) Multimeter probe to the LAB-K frame and touch the positive (+) probe to pin A in each row. The Multimeter should indicate that +5V is present. If there is no voltage (or a negative voltage) present, then check:
	1. the pin A for a faulty connection; or
	2. the power supply, which may be wired backwards.

5.2.2 AC Checks

Test Equipment: Multimeter, used in the voltmeter mode.

NOTE

If a meter is being used, it should not be pegged. Set the meter at approximately 60 Vac.

Table 5-1
Logic Application Modules of the LAB-K

Item No.	Dwg. No./Part No.	Description	QUANTITY/VARIATION																			
			LABK-A	LABK-B	LABK-B1	LABK-C	LABK-C1	LABK-C2	LABK-D	LABK-E	LABK-E1	LABK-F	LABK-F1	LABK-L	LABK-M	LABK-N	LABK-N1	LABK-N2	LABK-N3	LABK-P	LABK-Q
	K003	Gate Expander	1	2		2						2		1							
	K012	Gate Expander				2															
	K028	Gate Expander				1				1					1						
	K113	Inverting Gate		2		4				3					1	1				1	
	K123	Non-Inverting Gate	1	1		3			2	1		2		1		1					4
	K124	AND/OR Non-Inverting Gate	1			1														1	
	K134	Inverter		2		6				3		2			1					1	
	K135	Inverter										1									
	K161	Binary to Octal Decoder		1																	1
	K202	Flip-Flop		1		1															
	K210	Binary or BCD Counter		1						3					4	3		1		7	1
	K211	Programmable Driver							9					6							
	K220	Up/Down Counter				3															
	K303	Three Timers													1						
	K323	One Shot	1			2						3									
	K371	Timer and Control													1						
	K410	Indicator Light			2																
	K420	Toggle Switch	1																		
	K422	BCD Thumbwheel Encoder				3	3														
	K424	BCD Thumbwheel Decoder		1						3					4	2				3	*1
	K432	Potentiometer Card										1									
	K501	Schmitt Trigger	1																		
	K731	Source Module							1												
	K990	Timer Comp Board	1			1				1		2									
	M113	NAND Gate													1					1	
	M302	Dual Delay Multivibrator												1	2					2	
	M405	Crystal Clock												1							
	K604	(In Place of K644 in LABK-F)											1								
	K671 (REF)	Decimal Decoder & Nixie Display						3			3						3		1		
		*Not required if 2nd VI/VR Option ordered.																			

Step	Procedure
1	Check the K410 indicator lights for 12 Vac.
	( ) a. Place the probes across the connector tabs (points 2 and 5, Chapter 2, Figure 2-19). Read approximately 12 Vac.
2	Check the K731 Sync Line for 12.6 Vac.
	( ) a. Place the Multimeter probes across pins U_2 and V_2, row F, slot 2.
3	Check the K771 Nixie power supply for a 120 Vac, and set the voltmeter to accept a 300V full-scale range reading.
	If a positive voltage reading is not obtained in either Steps 1, 2, or 3, the following procedure is recommended:
	( ) a. Refer to Chapter 2, Figure 2-21 for transformer wiring points G and H which should read 120 Vac. If a zero reading is obtained;
	( ) b. Check the incoming ac cable. If the incoming cable registers 120 Vac, then transformer wiring points G and H are correct;
	( ) c. Test for 120 Vac on terminal block pins No. 5 and 6 of the 5 Vdc power supply (shown in Chapter 2, Figure 2-24);
	( ) d. Check pins No. 3 and No. 4 for 120 Vac.
	If a positive reading is obtained, faulty wiring exists between terminals No. 3 and No. 4 and the Nixie power supply ac tabs shown in Chapter 2, Figure 2-23.

5.2.3 Application Logic Checks

Test Equipment: K791 Test Probe or Multimeter (oscilloscope can also be used).

NOTE 1

Whenever installing modules in a frame, **remove ac power from wall.**

NOTE 2

The K791 Test Probe will recognize the +5V and 0V as a high or low on the two indicator lights. A stream of pulses of 1-sec or greater can be seen by the high light going on and off.

Any pulse stream of higher frequency is indicated by the high and low light remaining on steady state. To insure exact timing use an oscilloscope.

Application A: Input Logic – Install Application A modules and institute the following checks on the input logic (refer to Table 5-1 and module utilization schematic X602-0-10). Use logic schematic X602-0-5 for reference also.

Step	Procedure
1	Check the MASTER RESET toggle switch (see Chapter 4, Figure 4-1).

( ) a. Connect the K791 Test Probe to pin D, row A, slot 1 (A01D).

( ) b. Depress the MASTER RESET toggle switch and ensure that the toggle output line goes from high to low (high light on the K791 Test Probe will flash).

( ) c. Connect the test probe to pin E, row A, slot a (A01E).

( ) d. Depress the MASTER RESET toggle switch and ensure that the toggle output goes from low to high (low light on the K791 Test Probe will flash).

NOTE

If the Nixie read-outs and the K410 indicator lights are being used, the read-outs clear to zero and the indicator lights extinguish when the MASTER RESET toggle is depressed.

( ) e. Connect the test probe to pin R, row F, slot 17 (F17R).

( ) f. Depress the MASTER RESET toggle switch and ensure that the output of the K123 gate goes from high to low.

2 Check the "SYSTEM ON" toggle switch (see Chapter 4, Figure 4-1).

( ) a. Connect the test probe to pin L, row A, slot 1 (A01L).

( ) b. Depress the "SYSTEM ON" toggle switch to the "ON" position, and ensure that its output line goes from low to high (high light on K791 Test Probe will flash).

( ) c. Connect the test probe to pin D, row F, slot 18 (F18D), and ensure that the K124 output line is sitting high.

If the proper signal levels in Steps 1 or 2 are not obtained, check logic schematic X602-0-5 and check the wiring for the "SYSTEM ON" flip-flop located at coordinates B, 8 (on the schematic). For a further explanation refer to Page 2-13 of the LAB-K Handbook.

5.2.4 Application D and/or L – Timing Kits

By using Table 5-1 as a reference for Application D and/or L, the user can install the modules in the locations designated by module utilization schematic X602-0-10.

NOTE

Module K123 located D12 is required for this application.

Application D checks

Step	Procedure
1	Ensure that the MASTER RESET toggle switch is in the neutral (middle) position.
2	Depress the "SYSTEM ON" toggle switch (to enable the timing kits).
3	Ensure that the clock pulses are present at the plugboard.

Step		Procedure
3 (Cont)	( ) a.	Insert the K791 Test Probe on the plug wires inserted into plugboard coordinates A7, A6, and A5.
	( ) b.	At each of the above time base outputs, make certain that there is a pulse train, i.e., a series of level changes. For example, if the 10-sec time base is being checked, there is a high-to-low transition every 10 seconds, etc.
4		If there are no timing pulses for Kit D, check for a high level (+5 Vdc) on pin E05F. If a low level exists, check for a connection between the "SYSTEM ON" flip-flop and pin E05F.
5		If there are still no pulses coming out of Kit D, check the pins E09K, E12K, and E16K to sample the clear lines of the time generators. These pins should be sitting high (+5 Vdc).
6		If the clear lines mentioned above are sitting low, check F16, pin R – which should be sitting high (+5 Vdc). If it is low, checkout one-shot logic in slot F16.
7		Check pin F02D, which should be sitting high. If it is low, the K731 module is defective.

Review the logic description of the K211 Programmable Dividers in Chapter 3.

Application L Checks

Step		Procedure
1		Ensure that the MASTER RESET toggle switch is in the neutral (middle position).
2		Depress the "SYSTEM ON" toggle switch, enabling the timing kits.
3		Ensure that the clock pulses are present at the plugboard.
	( ) a.	Insert plugwires into plugboard coordinates A10, A9 and A8.
	( ) b.	Check each plugwire with a test probe.
	( ) c.	At each of the above time base outputs, make certain that there is a pulse train, i.e., a series of level changes. For example, if the 0.10-sec time base is being checked, there would be a high-to-low transition every 0.10 seconds, etc.
4		If there are no timing pulses from Kit L, check for a high level (+5 Vdc) on pin D12U. If a low level exists, check for a poor connection between the "SYSTEM ON" flip-flop and pin D12U.
5		If there are still no pulses coming out of Kit L, check pins F10K, F12K, and F13K to sample the clear lines of the time generators. These pins should be sitting high (+5 Vdc).
6		If the above mentioned clear lines are sitting low, check F16, pin R, which should be sitting high (+5 Vdc). If it is low, checkout the one-shot logic in slot F16.
7		Check pin F02D which should always be sitting high. If it is low, the K731 module is defective.

5.2.5 Application B – Sequencer

Use schematic X602-0-9 as a logic reference and install the sequencer modules, then make the following checks.

Step	Procedure
1	The Sequencer steps from 0 to 9.
	( ) a. Set the Sequencer Thumbwheel Switch (see Chapter 4, Figure 4-1) at 9.
	( ) b. Use the jumper provided in the accessory kit from A01R to C06H:
	( ) Depress the MASTER RESET toggle switch. ( ) Depress the START toggle switch. ( ) Depress the SPARE (Third) toggle switch.
	(See Chapter 4, Figure 4-1 for toggle switch orientation.)
	NOTE 1 If you have obtained Option B1 (Sequencer Indicator Lights), you will find that every time the SPARE toggle switch is depressed the Sequencer will step. The indicator lights verifying this action.
	NOTE 2 If you do not have Option B1, the following test procedure is indicated:

Step	Procedure
1	Place the K791 Test Probe on a plugwire in position at L10 and verify a low (+0 Vdc) state. This is accomplished by plugging the *plugwire* (not the test probe) in position L10 and attaching a test probe at the other end.
	( ) a. Depress the SPARE toggle switch.
2	Place the test probe on a plugwire at Pos. 1 L9 on the plugboard.
	( ) a. Verify the low state in the same manner as above. ( ) b. Depress the SPARE toggle switch.
3-7	Repeat the above procedure for the remaining Positions 2–9 (L-8, L-7, L-6, K-10, K-9, K-8, K-7, and K-6), and verify the low position on each. Depress the SPARE toggle switch before testing each successive pin position.
8	Set the Sequencer Thumbwheel Switch to Position 1.
	( ) a. Depress the MASTER RESET toggle switch. ( ) b. Depress the START toggle switch. ( ) c. Verify low state (+0 Vdc) on pin L10. ( ) d. Depress the SPARE toggle switch. ( ) e. Verify low state (+0 Vdc) on pin L9. ( ) f. Depress the SPARE toggle switch.

Step		Procedure
8 (cont)	( ) g.	Verify that low state has reappeared on pin L10

NOTE

The above procedure ensures that the Sequencer resets to zero at the termination of the step set by the Sequencer Thumbwheel Switch. This makes it possible to automatically reset any length sequence from 0 – 9. (The example given above is a two (2) step sequence – 0 and 1.)

9 If the checkout procedure indicates a logic fault, refer to logic schematic X602-0-9. Check the wiring between the BCD Thumbwheel Switch K210 located at coordinates B5 (on the schematic), and the inverted outputs at coordinates C3 (on the schematic).

Refer to the sample Troubleshooting Section at the end of this chapter, it provides the user with a working rationale for troubleshooting logic faults, poor connections, etc.

NOTE

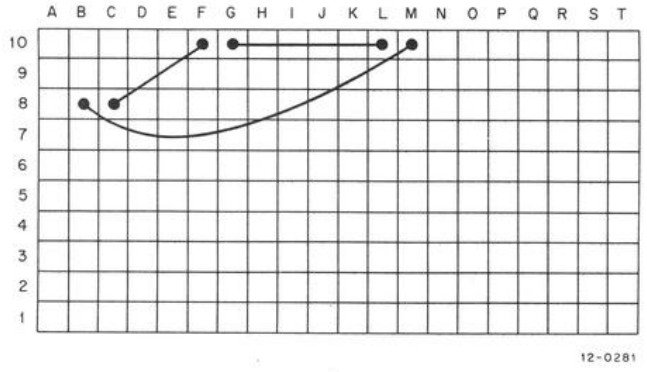
Remove jumper at the conclusion of testing. A description of the control logic at the Sequencer checkout appears in this chapter.

5.2.6 Application C – Down Counter

Install the Down Counter modules and institute the following checkout procedures.

Sequence 0

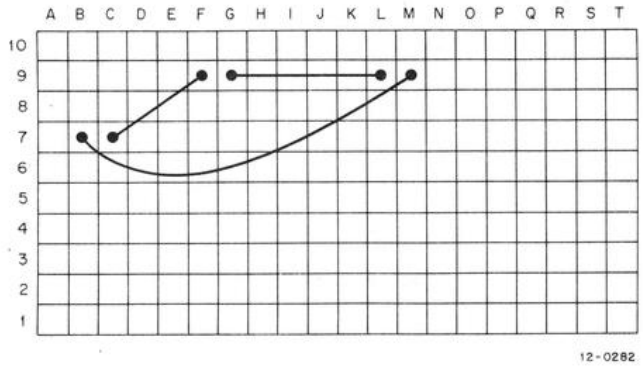
Step	Procedure
1	L10 (sequencer step 0) to G10 (enable down counter thumbwheel switch No. 1) R
2	F10 to C8 (enable .001 sec to down counter) R
3	B8 to M10 (down counter to zero steps sequencer) G
4	Set thumbwheel switch No. 1 for 800 (.001 sec)



R = RED
G = GREY

Sequence 1

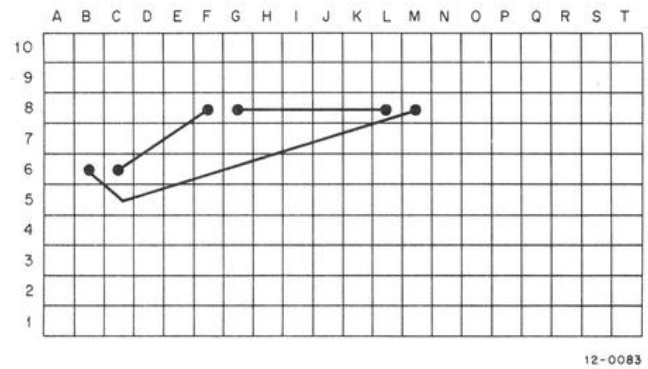
Step	Procedure
1	L9 (Step 0 of sequencer) to G9 (enable down counter thumbwheel No. 2) R
2	F9 to C7 (enable .01 sec to down counter) R
3	B7 to M9 (down counter to zero steps sequencer) G
4	Set thumbwheel switch No. 2 for 600 (.01 sec)



R = RED
G = GREY

Sequence 2

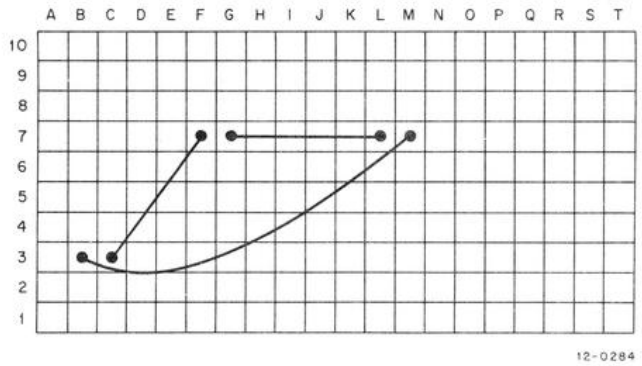
Step	Procedure
1	L8 (sequencer Step 2) to G8 (enable down counter thumbwheel switch No. 3) R
2	F8 to C6 (enable .1 sec to down counter) R
3	B6 to M8 (down counter to zero steps sequencer) G
4	Set thumbwheel switch No. 3 for 100 (.1 sec)



R = RED
G = GREY

Sequence 3

Step	Procedure
1	L7 (sequencer Step 3) to G7 (enable down counter thumbwheel switch No. 4) R
2	F7 to C3 (enable 1 sec to down counter) R
3	B3 to M7 (down counter to zero steps sequencer) G
4	Set thumbwheel switch No. 4 for 005 (1 sec)
5	Set sequencer thumbwheel for 3
6	Equipment List: LAB-K B, C, C1, D, G, H, K, L, R or J (needed for schedule) LAB-K B1, C2 (recommended for schedule)



R = RED
G = GREY

5.2.7 **Option C1**

If Option C1 (Encoder Sets 3 and 4 on the down counter) has been ordered for LAB-K:

Step	Procedure
1	( ) Set the Sequencer Thumbwheel Switch to 3.

If Option C1 has not been ordered:

Step	Procedure
1	( ) Set the Sequencer Thumbwheel Switch to 1.
2	( ) Depress the MASTER RESET toggle switch.
3	( ) Depress the START toggle switch.

5.2.8 **Option C2**

If Option C2 (Nixie digital read-outs for the Down Counter) has been ordered, the number is read into the Nixie display and is displayed and counted down to zero in 1-sec increments.

When the Nixie read-out detects zero, the Sequencer steps to Position 1. The number in the second set of encoders is displayed and counted down to zero in increments of 0.10 seconds.

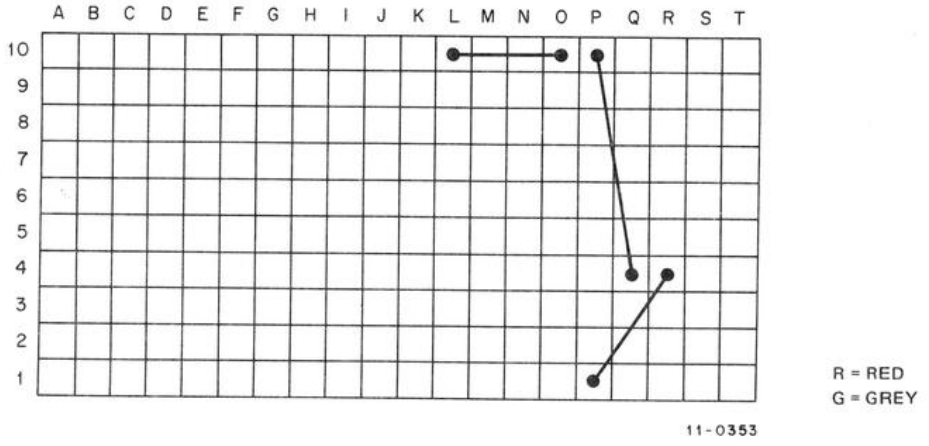
If the Sequencer Thumbwheel Switch has been set to 1, the previous sequence will be cycled continuously. If the Sequencer Thumbwheel Switch has been set to 3 (Option C1), the next two sequences will then take place. On Steps 2 and 3 of the Sequencer, the remaining sets (3rd and 4th) are read in and counted down to zero in .01- and .001-sec increments. respectively.

5.2.9 Application E – Up Counter

Install the Up Counter modules (with ac power removed) and institute the following checkout procedures.

Sequence 0

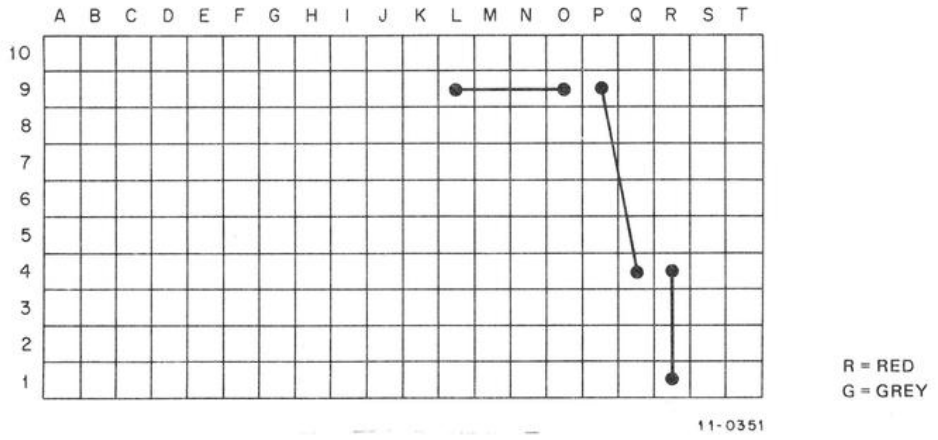
Step	Procedure
1	L10 (step 0 of sequencer) to 010 (decoded up counter steps sequencer) R
2	P10 to Q4 (enable 1 sec to up counter) R
3	R4 to P1 (enable up counter thumbwheel switch No. 1) R
4	Set thumbwheel switch No. 1 for 005 (1 sec.)



If Option E1 (Decimal Decoder and Nixie Display) has been acquired, the number 000 is displayed in the Nixie read-out and the counter counts up in 1-sec increments until the selected number has been reached in the thumbwheel switch. When the number in Thumbwheel Switch No. 1 has been reached, it resets the Up Counter and steps the Sequencer to 1. The counter in the second stage is activated and counts up in 0.10-sec increments until the number in Thumbwheel Switch No. 2 is reached. When this number is reached, the Up Counter resets and recycles the above procedure indefinitely – or until the MASTER RESET toggle switch has been depressed.

Sequence 1

Step	Procedure
1	L9 (step 1 of sequencer) to 09 (decoded up counter steps sequencer) R
2	P9 to O5 (enable .1 sec to up counter) R
3	R5 to R1 (enable up counter thumbwheel switch No. 2) R
4	Set thumbwheel switch No. 2 for 100 (.1 sec)
5	Set sequencer thumbwheel switch at 1
6	Equipment List: LAB-K B, D, E, G, H, K, L, R or J (needed for schedule) LAB-K B1, E1, (recommended for schedule)



The other four time bases available to the Up Counter can be checked out by substituting the appropriate plugboard locations (refer to Chapter 4, Section 4.8 for the appropriate locations of plugboard coordinates for time bases).

The user can also refer to the Troubleshooting Section at the end of this chapter if this procedure does not check out.

If Option E1 has not been acquired, the following checkout procedure should be instituted.

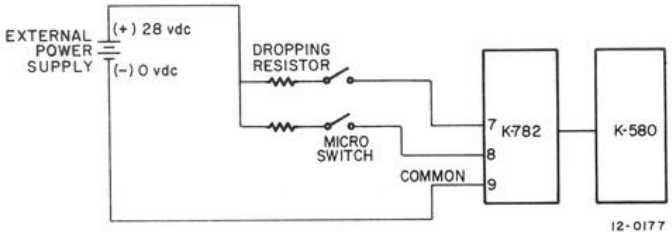
Step	Procedure
1	Connect the following wires to the plugboard: ( ) L10 to O10 ( ) P10 to Q4 ( ) P1 to R4 ( ) L9 to O9 ( ) P9 to Q5 ( ) R5 to R1
2	( ) Set Thumbwheel Decoder Switch No. 1 to 60 (refer to Chapter 4, Figure 4-1).
3	( ) Set Thumbwheel Decoder Switch No. 2 to 60.
4	( ) Set the Sequencer Switch to 1.
5	( ) Insert a plugwire in P2.
6	( ) Set test probe (or Multimeter) to the other end of the plugwire.
7	( ) Depress the MASTER RESET toggle switch.
8	( ) Depress the START toggle switch. Note one low-to-high transition every minute indefinitely or until the MASTER RESET toggle switch is depressed.

For further troubleshooting of Application E logic, the user can refer to the troubleshooting section at the end of this chapter.

5.2.10 **Application F – Input/Output Logic**

Install "F" logic using schematic X602-0-2 and module utilization diagrams X602-0-9

Before attempting to interface the microswitch inputs to the K782 module, refer to Chapter 2, Figure 2-29 (showing points 7, 8, and 9 (ground) on the K782 module), and Figure 2-25 (location of the K782 module in the I/O hardware panel) for orientation.



To determine the correct dropping resistor to use between the power supply and the microswitches, refer to Table 5-2.

Table 5-2
K580 Voltage Dropping Resistances

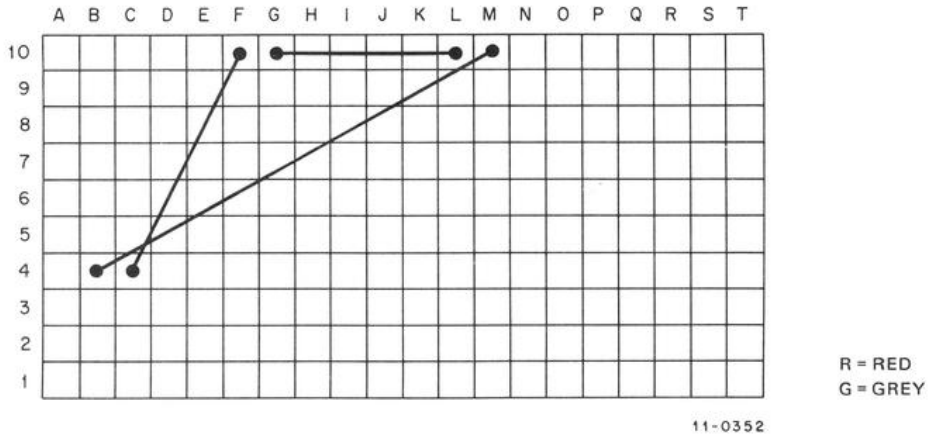
Contact Supply Voltage	10	12	15	24	28	48	90	100	120
Dropping Resistance	0	82Ω	220Ω	620Ω	820Ω	1.8KΩ	3.6KΩ	3.9KΩ	4.7Ω
Dissipation	–	0.05W	0.11W	0.3W	0.4W	0.85W	1.8W	2.0W	2.5W

After the microswitches have been connected to terminal block pins 7 and 8 (see Chapter 2, diagram and Figure 2-29), the input logic shown on logic schematic X602-0-5 (at coordinates B and C, 7 and 8) is ready to be checked out.

The user should institute the following test procedure:

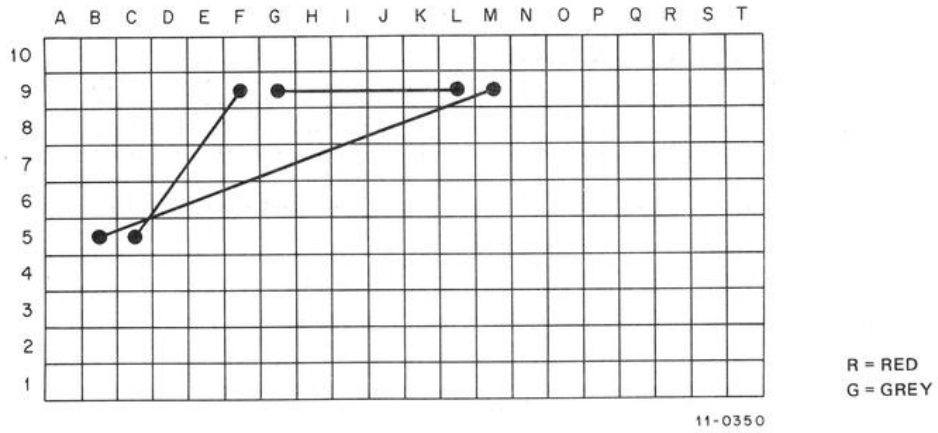
Sequence 0

Step	Procedure
1	L10 (step 0 of sequencer) to G10 (enable down counter thumbwheel switch No. 1) R
2	F10 to C4 (enable left event to down counter) R
3	B4 to M10 (down counter to zero steps sequencer) G
4	Set down counter thumbwheel switch No. 1 at 010



Sequence 1

Step	Procedure
1	L9 (step 0 of sequencer) to G9 (enable down counter thumbwheel switch No. 2) R
2	F9 to C5 (enable right event to down counter) R
3	B5 to M9 (down counter to zero steps sequencer) G
4	Set down counter thumbwheel switch No. 2 at 015
5	Set sequence thumbwheel switch at 1
6	Equipment List: LAB-K A, B, C, H, K, R or J (needed for schedule) LAB-K B1, C2 (recommended for schedule)



The Down Counter shows the number 010 and counts itself down one count for each time the external microswitch (connected to the left event) steps until it reaches zero. The Sequencer steps, causing a number 015 to again be placed in the Down Counter. The microswitch connected to the Down Counter now steps the Sequencer, resetting it to zero. This procedure is repeated indefinitely or until the MASTER RESET toggle switch is depressed.

5.2.11 Output Logic (K683)

The user should refer to Chapter 3, Section 3.3 which gives output ratings for each of the eight K683 Drivers.

Three Drivers (3, 7, 8) are driven directly from the programmable plugboard as long as ground at the input is present; three Drivers (4, 5, 6) are driven through the plugboard by one-shots – allowing drivers to be turned on for a predetermined period of time.

NOTE

Review Sections 3.2, 2.6 (One-Shot and Timers), and 2.10 to determine the duration of the one-shots that control output drivers 4, 5, 6 of the K683.

When the user knows the time base desired for a particular timer, he must hard-wire between the one-shot node point and the specific point on the K990 that contains the appropriate RC network.

The K990 circuit boards have five unassigned time bases available to the five one-shots. Information in Chapter 2, Page 2-56 shows the K990 circuit boards that require 50, 100, and 250 millisecond pulse leads. There are two additional locations where these time bases can be installed: A22, pins H and J.

Heavy Duty Driver No. 4 can be used to control a reinforcement device. The lower potentiometer brought out on the manual controls (as shown in Chapter 4, Figure 4-1), pin J, provides the control-in-time for the one-shot preceding that driver.

The timing range set on the K432 is 100 milliseconds to 3 seconds. To change the range, refer to timing chart below:

Connect to Pin J or V	RC Time Range Min.	Max.
None	10 μs	300 μs
D or R	100 μs	3 ms
E or S	1 ms	30 ms
F or T	10 ms	300 ms
H or U	100 ms	3 sec
L	1 sec	30 sec

A change will require removing the wire off of A31H and A31J and replacing it with a wire from A31J to the opposite pin (as shown in the chart) to obtain a different timing range.

Drivers 1 and 2 have been hard-wired to step 8 and 9 of the IRT Distributor. If you do not intend to acquire the IRT Distributor Kit, those drivers can be wire-wrapped to an empty location on the programming plugboard and used as additional drivers.

5.2.12 General Output Logic Checkout Procedure

Step 0 **Procedure**

Driver 3, 7, 8 and heavy duty driver No. 1 can be checked out as follows:

( ) a. Place an oscilloscope or lamp load (lamp to +5 volts) on the output screw terminals AA4-3 (light duty driver No. 3), AA4-7 (light duty driver No. 7), AA4-8 (light duty driver No. 8) and AA6-1 (heavy duty driver No. 1). Verify an off state (floating voltage on oscilloscope). Plus voltage.

( ) b. Apply a plugwire in the programming plugboard on to coordinate M6 (ground) and connect the following plugboard positions:

- ( ) M6 (ground) to Q9 (input to driver No. 7)
- ( ) R9 to S10 (input to heavy duty driver No. 1)
- ( ) T10 to T4 (gate input driver No. 8)
- ( ) S4 to R8 (input to driver No. 3)

( ) c. Check the four previous points on the screw terminals and verify the on state (a low on the oscilloscope). Ground voltage.

If loads are now on, drivers are operative.

The above procedure can be followed for drivers No. 4, 5, 6 and heavy duty drivers No. 2, 3 provided the necessary one-shot timing nodes have been connected to a K990 (if oscilloscope is not used, additional capacitance should be added so lamp will remain on for about 500 ms). (See K323, *1971 Control Handbook*.) For the drivers stated above, the plugboard connections would be as follows:

Sequence 1

Step	Procedure
1	Checkout plugboard connections

( ) A7 (1 sec. time base) to S9 (one-shot input to heavy duty driver No. 2)
( ) T9 to T8 (one-shot input to heavy duty driver No. 3)
( ) S8 to S6 (one-shot input to heavy duty driver No. 4)
( ) T6 to T5 (one-shot input to driver No. 4)
( ) S5 to S3 (one-shot input to driver No. 6)
( ) T3 to T1 (one-shot input to driver No. 6)
( ) L10 to K4 (L10 must be moved to K3 and K2 to test respective drivers to enable them).

5.2.13 Driver Output Checkout Procedure

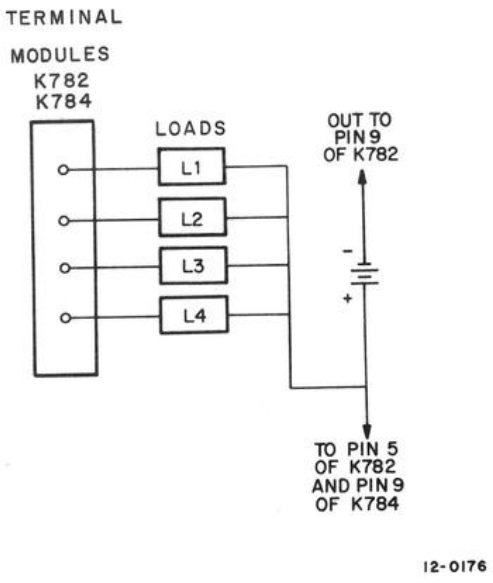
The user should review Chapter 2, Section 2.8 and note in particular Figures 2-25 and 2-27.

Step	Procedure
1	Connect the +28 Vdc power supply to terminal No. 9 on the K784 module and terminal No. 5 of the K782 module. The negative side of the power supply must be connected to terminal No. 9 as shown in Chapter 2, Figure 2-29. It is strongly recommended that the external power supply be mounted on the mounting bars at the top rear of the LAB-K cabinet.

NOTE

The Driver outputs are connected to the terminal modules which in turn are connected to one side of the load (lamp, solenoid, relay, counter, etc.). The other side of the load is returned to the positive side of the external power supply.

An additional K683 Driver connected to a K782 terminal board (as shown in Chapter 2, Figure 2-28) is provided when the IRT Distributor logic kit is ordered. This module provides Drivers 0 – 7. As mentioned above, Drivers 8 and 9 are provided on another card. These modules are designed to provide output drive capabilities sufficient to operate electromechanical counters. (An example would be a 4-digit, 28 Vdc Sedeco Counter requiring 250 milliamps.) The K683 is capable of handling this driver. Any driver with a load of more than 250 milliamps will require a Heavy Duty Driver (K644).



5.2.14 Application M – Variable Interval/Variable Ratio Programming

For reference the user should consult Chapter 4, Section 4.9.

Sample VI Component:

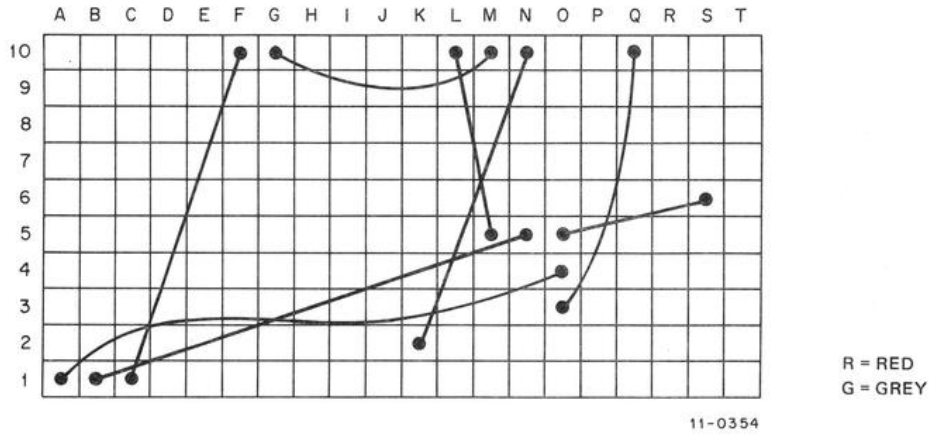
Assemble the 6 KHz clock by attaching the K371 timer control to the K303 timer as discussed in the *Control Handbook*, section on Timer Controls (K300 series). Set potentiometer to 6 KHz setting. The VI Component has a median of 30 seconds, a lower limit of 1 second, an upper limit of 120 seconds, and a duration of 15 minutes.

Sequence 0

Step	Procedure
1	L10 (step 0 of sequencer) to M5 (enable .1 sec to VI) R
2	N5 to B1 (enable 60 sec to down counter) G
3	C1 to F10 (enable down counter thumbwheel switch No. 1) R
4	G10 to M10 (down counter to zero steps sequencer) R
5	N10 to K2 (enable heavy duty driver No. 4) R
6	A1 (right event) to O4 (event input for gating V1) G
7	O5 (V1 gated output) to S6 (one-shot input to heavy duty driver No. 4) R

Sequence 0 (Cont.)

Step	Procedure
8	Q10 (one-shot output of heavy duty driver No. 4 on) to O3 (reset memory for up counter VI/VR)
9	Set the median percentile thumbwheel switch at O3
10	Set VI/VR lower limit thumbwheel switch at 10
11	Set upper limit thumbwheel at 120
12	Set down counter thumbwheel switch for run time (min.)
13	Equipment List: LAB-K A, B, C, D, E, F, G, H, K, L, M, R or J (needed for schedule) LAB-K B1, C2, E1 (recommended for schedule)



Discussion:

When the VI component is run on the LAB-K, the following sequence occurs logically. The 6 kc clock begins to run as soon as the power is turned on, and it steps a two-bit BCD counter. When the counter is at 3, which is the median percentile figure of component 1, the thumbwheel decoder goes high and sets the median percentile flip-flop. This puts a high on one leg of the coincident gate. If a count is decoded in the lower limit counter before the median percentile counter reaches a count of 99, the coincident gate goes high and sets the control flip-flop which subsequently provides reinforcement and resets the upper limit counter. When the median percentile counter reaches 99, it is reset (goes low) which disables the coincident gate. It is not set again until the thumbwheel decoder detects the percentile setting (3%). Thus, with a 3% percentile setting, the aperture window is open from a count of 4 to 99. It is closed from 0 to 3.

The lower limit counter is reset when the lower limit count is detected. Whenever the lower limit counter is reset, a count is put into the upper limit counter. The above cycle continues until the upper limit count (120 sec) is decoded. The upper limit counter then sets the control flip-flop, which provides a reinforcement signal.

The schedule is terminated when the Down Counter, which times the duration of the component, reaches zero and steps the sequencer. In essence, the upper limit counter ensures that if there is no coincidence at the coincidence gate by the time the upper limit count is reached, then the organism is reinforced. For this reason, the median is used with VI/VR programmer

rather than the statistic mean. If the statistic mean was used, it would reflect any interval that reached the upper limit, which would affect the distribution. Since the mean represents the average of a distribution, and the median is the middle of a distribution, in cases of an exact normal distribution, the mean and median are equivalent. However, when the distribution is skewed the mean and median are not equivalent. Since the VI/VR programmer has upper and lower limits, there is a degree of skewed distribution. The median provides the middle of the distribution and ignores the skewed end.

Step	Procedure
1	( ) Connect the test probe of the pulser to F18R. Observe the upper limit "Nixie" tube read-out. F18, pin R should go high at the same time the "Nixie" tube read-out is reset to zero. (See logic schematic X602-0-7 for reference.) The maximum reading in the counter should never exceed the upper limit setting (120).

NOTE

The "Nixie" read-out provides an Up Counter (or upper limit) reading, depending on the use of the logic.

If the user does not set the memory flip-flop at F18, the next point to check is C18T to determine whether a coincidence ever occurs. A coincidence provides the user with a low-to-high signal – appearing within a 120 second period. If it does not appear, place the test probe on C20U to determine if the aperture window is ever set (high).

If this signal (C20U) is not high, determine if the percentile counter is giving an output by placing the test probe at B15D. If this signal goes from high to low, an oscilloscope will be required to test the M Series modules located between B15D and C20U.

If a high-to-low signal is not detected, determine if the 6 kc time base at D20F is present. If it is not present, the K303 module may be improperly positioned in module slot or it may be defective. To check out the lower limit of the VI/VR, place test probe at B15K and verify the existence of a time base. If a time base exists, determine if the decoders are decoding proper numbers by placing the test probe on C13D. In the example given, the signal should be present every second. If there is no number being registered in the upper limit counter, place the test probe at D12D. A high-to-low transition signal should be observed every second. If this signal is not present, check logic schematic X602-0-7 at coordinates D4 and check the input pins to the AND/OR gate (K123 and K003).

NOTE

The second VI/VR Application P (logic schematic X602-0-8) is checked out in the same manner as Application M.

5.2.15 Independent Timing and Control Logic

The user should refer to logic schematic X602-0-2 at coordinates C,D: 4,5,6

Step	Procedure
1	To check out the independent one-shot: ( ) a. Connect the following wires to the plugboard: ( ) A6 to M1 ( ) Connect a plugwire to both K1 and L1. ( ) Place the test probe on the other end of the plugwire that is connected to L1. ( ) b. Depress the MASTER RESET toggle switch. ( ) c. Depress the SYSTEM ON toggle switch and observe a high-to-low pulse every 10 seconds. ( ) d. Place a test probe on the K1 patchcord lead and observe a low-to-high transition every 10 seconds. If this repetitive signal does not occur, the one-shot wiring is either incorrect or the module (K323) is defective. The potentiometer controlling this one-shot is shown in Chapter 4, Figure 4-1, pin V (Top Potentiometer).
2	To check out the Control Flip-Flop, the user should institute the following test procedure: ( ) a. Connect L10 to D5 (to enable the flip-flop). ( ) b. Place a jumper between A1R and C21U. ( ) c. Place one end of a plugwire H5 and another to I4. ( ) d. Place the test probe on the H5 plugwire lead. The set output should be sitting low (0 Vdc). If it is sitting high: ( ) e. Depress the MASTER RESET toggle switch. Signal should now be sitting low. ( ) f. Depress the SPARE toggle switch. The signal should now go high.

Repeat this procedure by placing the test probe on plugwire I4. The results should be exactly opposite of those obtained for plugwire H5. If this is not the case, check for defective wiring. If the wiring is not defective the modules are defective.

5.2.16 Application N – Session Timer

Install logic per X602-0-4 and X602-0-10.

Step	Procedure
1	To check out the Session Timer, the user should institute the following test procedure: ( ) a. Depress the MASTER RESET and START toggle switches.
2	If the "Nixie" read-out Option N1 or N2 has been ordered, a 1 minute time base will be observed on the "Nixie" read-out after the SYSTEM ON (START) toggle switch has been depressed. If, after one minute, the "Nixie" read-out does not show a count in the read-out, further testing is required.

Step	Procedure
3	If Option N1 or N2 have not been ordered, the following test procedure is indicated (see Chapter 4, Figure 4-1 for reference).

( ) a. Set the BCD Thumbwheel Switches for 00 hours and 02 minutes.

( ) b. Place the test probe in F29D. Plug in a plugwire to K5. Place the test probe on the other end of plugwire and verify a signal every two minutes. (See logic schematic X602-0-4). If the signal is not seen, refer to the general troubleshooting procedure at the end of this chapter.

5.3 SAMPLE IRT COMPONENTS

Component:

Determine the latency of X events using a 0.1-sec time base – duration 10 minutes.

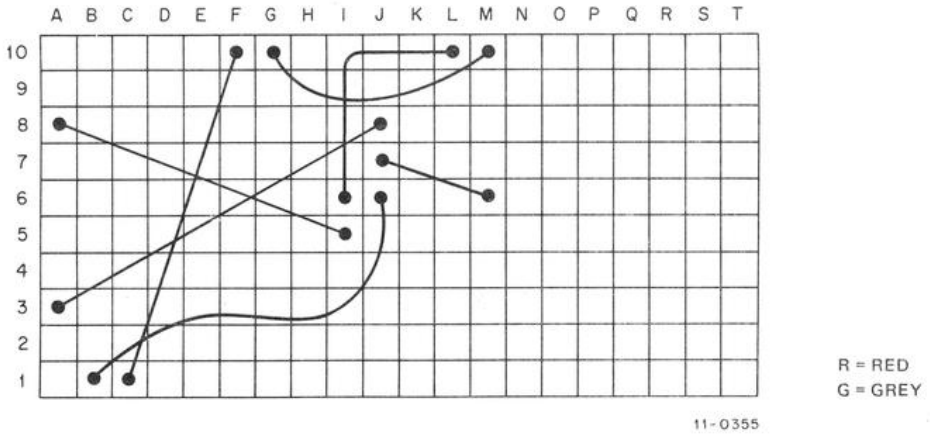
On the plugboard, make the following connections:

Sequence 0

Step	Procedure
1	L10 (sequencer step 0) to I6 (enable distributor) R
2	J6 to B1 (enable 60-sec down counter) G
3	C1 to F10 (enable down counter thumbwheel switch No. 1) G
4	G10 to M10 (down counter to zero steps sequencer) R
5	A8* (0.1-sec output) to I5 (time input to distributor) R
6	A3 ($\overline{\text{left}}$ event) or A1 ($\overline{\text{right}}$ event) to J8 (event input to IRT) G
7	J7 (disable) to M6 (ground)** R
8	Set down counter for run time (min.)
9	Latency of X events is determined using a 0.1-sec time base
10	Equipment List: LAB-K A, B, C, D, F, G, H, K, L, Q, R or J (needed for schedule) LAB-K B1, C2 (recommended for schedule)

*The time base and event outputs located in column A of the plugboard are used with the IRT.

**If this point is not being used, it is always connected to the ground. When connected to Bin 10, the sequencer cannot step pass position 10 to 0; therefore, the 10th position becomes the overflow bin.



The program outlined in component 1 is used in instances where the event latencies are going to be distributed over ten bins. The time base enabled into the IRT Distributor is the only variable from program to program.

Discussion:

A time base, which determines the bin width, is enabled into the BCD counter, and the counter output is decoded (K161) into a decimal number. The decimal numbers, 0 – 9, are represented by the ten decoder output lines; these lines are connected to one leg of the bin gate (K123). Thus, each bin gate represents one of the decimal numbers, 0 through 9. The other leg of the logic gates is connected to the event one-shot, which is triggered by a response. The outputs of the bin gates are connected to drivers, which are usually connected to an electromechanical decimal counter.

The output of a bin gate goes high (on state) when its decoder leg is high (the number that it represents has been decoded by the BCD counter) and when the one-shot line is high (response). The high output of the bin gate turns a driver on. At any given time, the output of only one bin gate is high.

The IRT BCD counter is reset and a new count initiated each time an event occurs. If an event does not occur and decimals 0 through 9 are decoded, the time base pulse resets the IRT BCD counter. This situation, however, could result in an inaccurate distribution, especially on the upper limits. This can be controlled by connecting the decoder leg of bin gate 10 (I7) to the IRT BCD counter count gate (J7, disable). If the decoder leg of bin 10 goes high, the high signal inhibits the count gate (K124) until an event occurs. When an event occurs, the IRT BCD counter is reset and the bin 10 decoder leg goes low, which subsequently enables the K124 count gate.

5.4 SKEWED DISTRIBUTION

The IRT is used for the purpose of recognizing the interval of time between responses. To count responses, it is common practice to distribute the responses over the ten bins. In some experiments, however, all the responses occur within a certain bin range and, in such instances, a lower limit can be established.

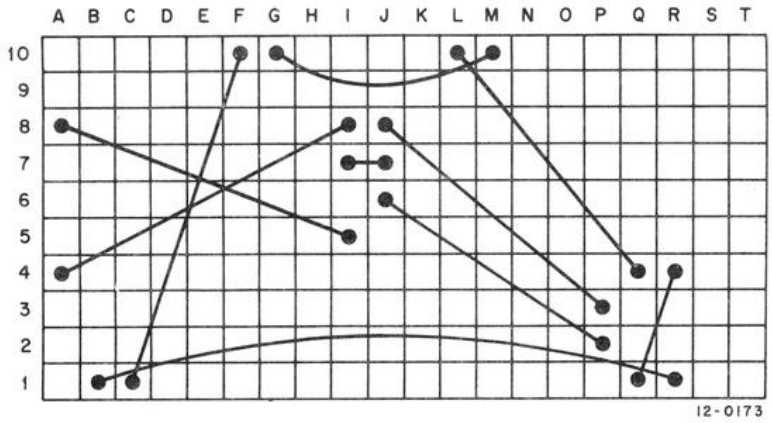
For example, if all the responses in a given experiment occur within bins 3, 4, and 5, then the time counted in bins 0, 1, and 2, say 0.3 seconds, would represent the lower limit figure. As a matter of accuracy, the researcher must be assured that the lower limit bins count up the amount of time in them. The Up Counter is used for this purpose.

The lower limit count is set into the Up Counter. The decoded Up count output is connected to the ENABLE DISTRIBUTOR point of the IRT counter count gate. Thus, a time base is enabled into the IRT counter after the lower limit is decoded in the Up Counter. This type of component is programmed on the plugboard as shown in the second programming sample.

Component:

Skewed distribution (bins 3, 4, and 5) – time base, 0.1 sec, duration – 10 minutes.

Step	Procedure
1	( ) L10 (Step 0) to Q4 (enable .1 sec to Up Counter)
2	( ) R4 to Q1 (enable Up Counter Thumbwheel Switch No. 2)
3	( ) P2 (SET MEMORY for Up Counter) to J6 (enable distributor)
4	( ) A8 (.1-sec output) to I5 (time input to distributor)
5	( ) A4 (left event) or A2 (right event) to I8 (event input to IRT)
6	( ) J8 to P3 (Reset Memory for Up Counter)
7	( ) J7 (disable) to I7 (bin 10)
8	( ) R1 to B1 (enable 60-sec Down Counter input)
9	( ) C1 to F10 (enable Down Counter Thumbwheel Switch No. 1)
10	( ) G10 to M10 (Down Counter to zero steps sequencer)



Discussion:

Since a 0.3 second lower limit is set into the Up Counter, bin 0 represents .3 to .4 seconds, bin 1, .4 to .5 sec, bin 2, .5 to .6 seconds, and so forth. The interval represented by bin 0 through bin 9 is from 3 to 12 seconds. If it is necessary to establish higher or lower limits, the time base is reduced or lowered accordingly.

NOTE

See Application F, Output Logic – K783.

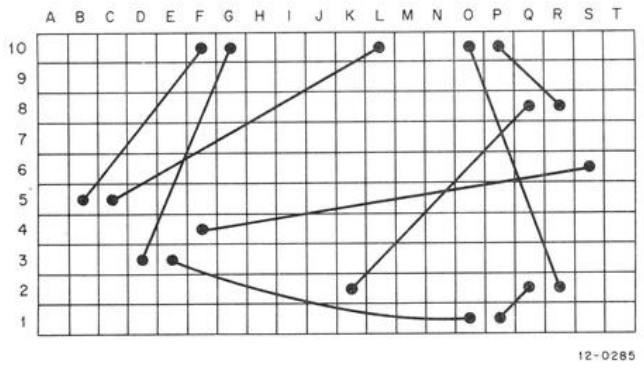
5.5 FIXED RATIO

Component:

Fixed Ratio, reinforcement provided after a predetermined number of events, for example twenty, are counted on the Down Counter, Recycle Down Counter on Zero. Duration of component is 1 hr.

On the plugboard, connect the following logic points to Sequence 0:

Step	Procedure
1	L10 (step 0 of sequencer) to C5 (enable right event to down counter) G
2	B5 to F10 (enable BCD thumbwheel switch No. 1) R
3	G10 to D3 (recycle down counter on zero) R
4	E3 to O1 (enable up counter BCD decode switch No. 1) G
5	P1 to Q2 (enable 60 sec to up counter) R
6	R2 to O10 (decoded up counter steps sequencer) R
7	P10 to R8 (input to driver No. 3) R
8	Q8 to K2 (enable heavy duty driver No. 4) R
9	F4 (zero detected on down counter) to S6 (one-shot input) G
10	Set the down counter thumbwheel switch No. 1 at desired number of events.
11	Set the up counter thumbwheel switch No. 1 at desired time (min.)
12	Set reinforcement time on the lower potentiometer
13	Equipment List: LAB-K A, B, C, D, E, F, G, H, K, R or J (needed for schedule) LAB-K B1, C2, E1 (recommended for schedule)



R = RED
G = GREY

Implementation:

Mount the plugboard into its mounting rack and depress the Master Reset and System On switches.

NOTE

Refer to Chapter 2, Section 2.10, Step 3 for information on setting the output drivers.

Discussion:

The sequencer step enables the logic points connected to it when the system is turned on. The Down Counter is stepped by 1 each time an event occurs. The DETECT ZERO pulse resets the counter and triggers the one-shot when the Down Counter has stepped from 20 to 0. The one-shot goes high and turns the drive on, which subsequently provides reinforcement. When the 1 hr. is detected the sequencer is stopped.

5.6 FIXED INTERVAL

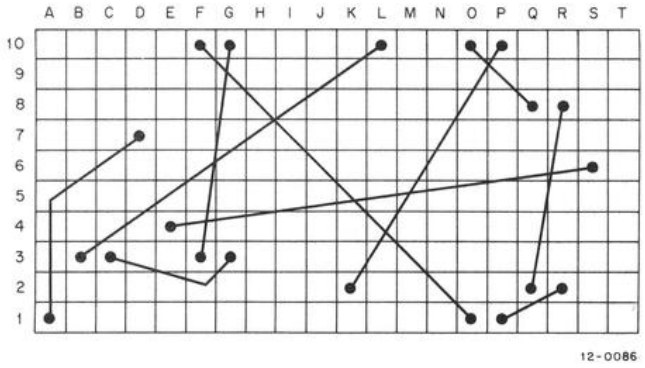
A Fixed Interval is run on the LAB-K by utilizing the Recycle Down Counter on Zero Plus Event gate located in the Down Counter kit.

Component:

Run a Fixed Interval of 30 sec, recycle Down Counter on zero plus event. Duration of component is 900 sec.

Sequence 0

Step	Procedure
1	L10 (step 0 of sequencer) to B3 (enable 1-sec to down counter) G
2	C3 to G3 (recycle down counter on zero, plus event – leg No. 1) R
3	F3 to G10 (enable down counter thumbwheel switch No. 1) R
4	F10 to O1 (enable up counter thumbwheel switch No. 1) G
5	P1 to R2 (enable 60 sec to up counter) R
6	Q2 to R8 (input to driver No. 3) R
7	Q8 to O10 (decoded up count steps sequencer) R
8	P10 to K2 (enable heavy duty driver No. 4) G
9	E4 (zero detected plus event) to S6 (one-shot input heavy duty driver No.4) G
10	T6 to D7 (reset 1 sec) G
11	Set the down counter thumbwheel switch No. 1 for desired time (sec)
12	Set the up counter thumbwheel switch No. 1 for desired run time (min.)
13	Set reinforcement time on the lower potentiometer
14	Equipment List: LAB-K A, B, C, D, E, F, G, H, K, R or J (needed for schedule) LAB-K B1, C2, E1 (recommended for schedule)



R = RED
G = GREY

NOTE

The sequencer thumbwheel switch (see Chapter 4, Figure 4-1) should be set at 9 (see Sequencer Application Note, Section 4.4).

Discussion:

The logic connected to Step 0 is enabled when the system is turned on. Any response that occurs before the Down Counter reaches zero is ignored by the logic. The first response that occurs after the Down Counter reaches zero triggers the one-shot, which turns the driver on – thus providing a reinforcement signal. The response signal also recycles the Down Counter which begins another 40-sec count down (Figure 5-1).

At the conclusion of 900 seconds, the Up Count is decoded and steps the sequencer. If a component is going to be implemented on Step 1, then its logic is enabled.

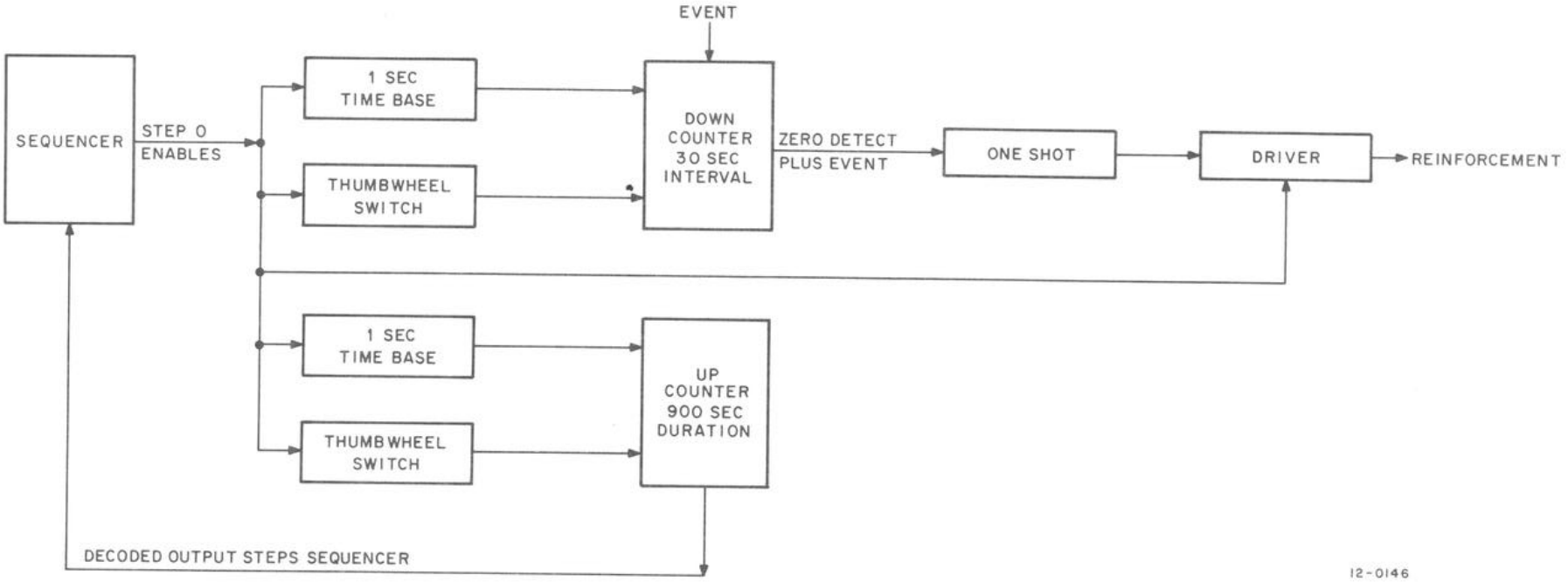


Figure 5-1 Fixed Interval

5.7 DRL SCHEDULE

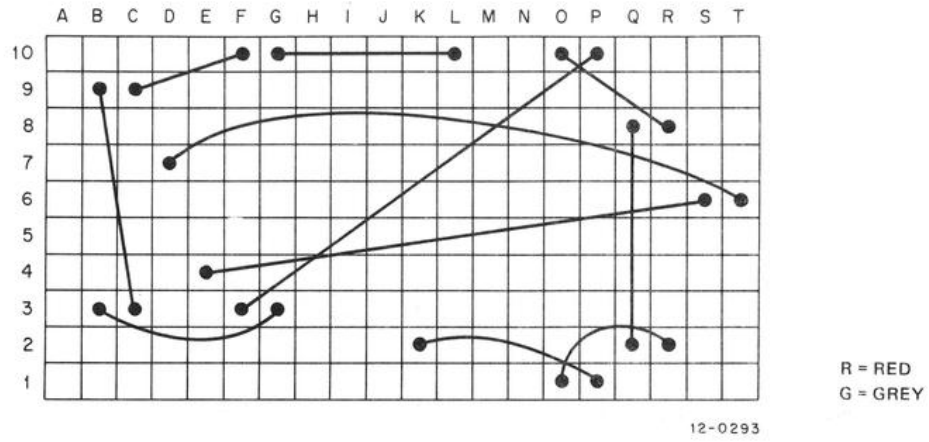
A DRL component is run by utilizing the Event Recycles Down Counter logic gate located in the Down Counter.

Component:

Run a DRL of 50 seconds, if event occurs during the count down – the Down Counter is recycled. If the Down Counter reaches zero, the organism is reinforced after first response. Duration of the component is 30 minutes.

Sequence 0

Step	Procedure
1	L10 (step 0 of sequencer) to G10 (enable downcounter thumbwheel switch #1) R
2	F10 to C9 (event recycles downcounter) R
3	B9 to C3 (enable 1 sec to downcounter) R
4	B3 to G3 (recycle downcounter on zero plus event) R
5	F3 to P10 (decoded upcounter steps sequencer) G
6	O10 to R8 (input to driver No. 3) R
7	Q8 to Q2 (enable 60 sec to upcounter) R
8	R2 to O1 (enable upcounter thumbwheel switch No. 1) R
9	P1 to K2 (enable heavy duty driver No. 4) R
10	A1 (right event) or A3 (left event) to D7 (reset 1 sec)
11	E4 (zero detected plus event output) to S6 (one shot input heavy duty driver No. 4)
12	Set the downcounter thumbwheel switch #1 for desired time (sec)
13	Set the upcounter thumbwheel switch #1 for desired run time (min)
14	Set reinforcement time on the lower potentiometer
15	Equipment List LAB-K A, B, C, D, E, F, G, H, K, R or J (needed for schedule) LAC-K B1, C2, E1 (recommended for schedule)



Discussion:

If an event occurs before the Down Counter reaches zero, the Down Counter is reset. Reinforcement is provided if a response occurs after a lapse of 50 seconds; i.e., at least 50 seconds between responses.

5.8 TITRATION AND THRESHOLD

The Down Counter can be programmed to count up or down, enabling the researcher to conduct threshold and titration experiments. The criteria for counting up or down is determined by the behavior of the organism. If the behavior is acceptable, the BCD counter counts down; conversely, if the behavior is unacceptable, the counter counts up (see Building Blocks – K220).

The plugboard is programmed for a normal Down Counter contingency (enable time base, thumbwheel, etc.); however, two new points are connected to the chain – FG6 (connect to ground for up/down counting – E30U) and DE6 (control line for counting on up/down counter – E32B).

Normally FG6 sits high, but it must be sitting at ground when the up/down count control gate (DE6) is being used. On the otherhand, it is necessary for the up/down line (pin L) to go high for at least 50 ms in order to read a number into the K220. To accomplish both the former and latter conditions, FG6 is connected to the normal output (low or GRN) of the Independent Timing One-Shot (Application F). The input of this one-shot is connected to a step on the sequencer. When the sequencer step goes true, the normal output of the Independent One-Shot goes high for a predetermined period of time (20 μs) which allows a number to be read into the Down Counter (the one-shot time period is set on the K432 adjustable potentiometer).

The SET MEMORY output (H5) of the memory flip-flop (Figure 5-2) located in Application F (X602-0-2) is connected to the Up/Down Control point (DE6). This flip-flop is connected in such a manner that acceptable behavior resets the flip-flop, and causes the Up/Down Control point (DE6) to go low, which causes the Down Counter to count down.

Conversely, unacceptable behavior sets the flip-flop and causes the Up/Down Control point to go high, which allows the Down Counter to count up.

NOTE

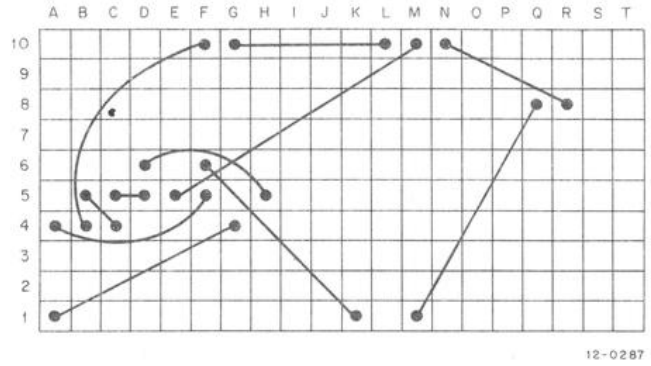
To use the memory flip-flop, the sequence enable input must be connected to the appropriate sequence step.

Sequence 0

Step	Procedure
1	L10 (step 0 of sequencer) to G10 (enable BCD thumbwheel switch No. 1) R
2	F10 to B4 (enable left event to down counter) R
3	C4 to B5 (enable right event to down counter) R

Sequence 0 (Cont)

Step	Procedure
4	C5 to D5 (sequence enable to set memory gate) R
5	E5 to M10 (down counter to zero steps sequencer) G
6	N10 to R8 (input to driver No. 3) R
7	Q8 to M1 (input to one-shot for independent timing) R
8	K1 (normal output of one-shot) to F6 (ground for up/down counting) R
9	H5 (set memory output) to D6 (control line for up/down counter) R
10	A4 (left event) to F5 (event enable to set memory gate) R
11	A1 (right event) to G4 (reset memory flip-flop) R
12	Set the down counter thumbwheel switch No. 1 for desired number.
13	Set the top potentiometer down in the central manual control hardware to the maximum (300 μsec).
14	Equipment List: LAB-K A, B, C, D, F, G, H, K, R or J (needed for schedule) LAB-K B1, C2 (recommended for schedule)



R = RED
G = GREY

5.9 SIDMAN AVOIDANCE

Component:

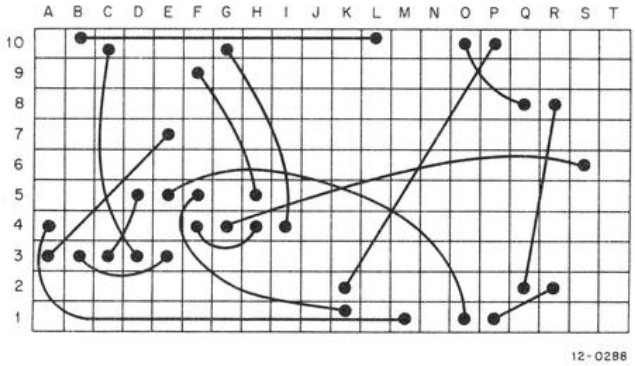
RS period of 30 sec and SS period of 15 sec. Duration is 80 minutes.

Sequence 0

Step	Procedure
1	L10 (Step 0 of sequencer) to B10 (event recycles down counter) G
2	C10 to D3 (recycle down counter on zero) R
3	E3 to B3 (enable 1 sec. to down counter) R
4	C3 to D5 (sequence enable to set memory gate) R
5	E5 to O1 (enable BCD decode) G
6	P1 to R2 (enable 60 sec. to up counter) R
7	Q2 to R8 (input to driver No. 3) R
8	Q8 to O10 (decoded up counter steps sequencer) R
9	P10 to K2 (enable heavy duty driver No. 4) G
10	A3 (left event) to E7 (reset 1 sec) R
11	A4 (left event) to M1 (input to independent one-shot) G
12	F4 (detect zero) to H4 (reset memory flip-flop) R
13	G4 to S6 (one-shot input to heavy duty driver No. 4) G
14	K1 (normal output of one-shot) to F5 (event enable to set memory gate) R
15	I4 (set memory output) to G10 (counter enable No. 1) R
16	H5 (set memory output) to F9 (enable BCD switch No. 2) R
17	Set the down counter thumbwheel switch No. 1 for RS period
18	Set the down counter thumbwheel switch No. 2 for SS period
19	Set the up counter thumbwheel switch No. 1 first run-time

Sequence 0 (Cont)

Step	Procedure
20	Set upper potentiometer for Max (downward)
21	Equipment List: LAB-K A, B, C, D, E, F, G, H, K, R or J (needed for schedule) LAB-K B1, C2, E1 (recommended for schedule)



R = RED
G = GREY

Discussion:

Initially, the SS period is enabled into the Down Counter. If the organism responds before the Down Counter reaches zero, the Down Counter is reset and the RS period is enabled into the Down Counter. If the organism does not respond before the RS period reaches zero, DETECT ZERO goes low and sets the memory flip-flop. The set output goes from high-to-low and triggers the driver one-shot, which turns the driver on. It also enables the SS period into the Down Counter. The next response during the avoidance period resets the memory flip-flop and re-enables the RS period.

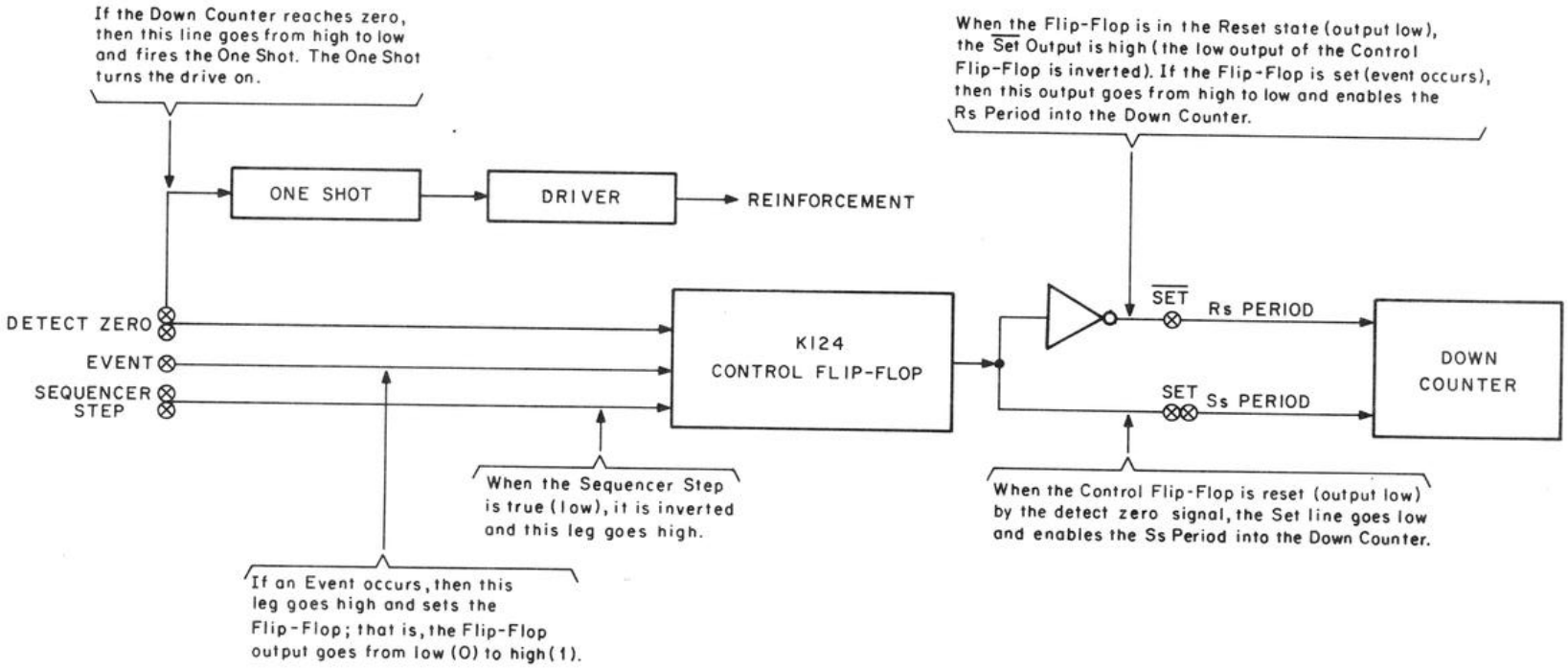


Figure 5-2 Sidman Avoidance

5.10 MULTIPLE SCHEDULE

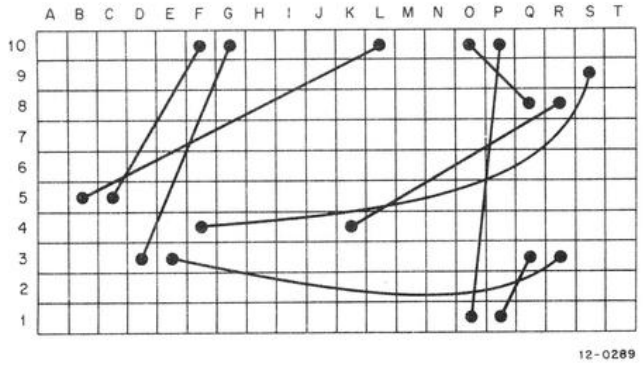
Sequences		Component		Duration	
0	FR	50		120	Red Lamp ON
1	Time Out	60			
2	Sidman Avoidance	SS 20	RS40	90	Tone
3	Time Out	60			

Sequence 0

Fixed Ratio of 50 for a duration of 120' – turn lamp on.

On the plugboard, make the following connections:

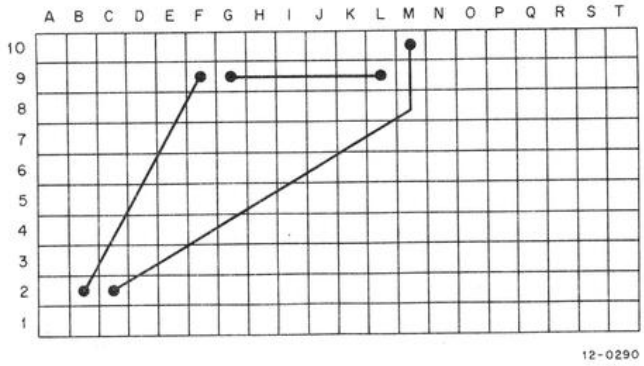
Step	Procedure
1	L10 (Step 0 of sequencer) to B5 (enable right event to down counter) G
2	C5 to F10 (enable down counter thumbwheel switch No. 1) R
3	G10 to D3 (enable down counter to recycle on zero) R
4	E3 to R3 (enable 10 sec to up counter) G
5	Q3 to P1 (enable up counter thumbwheel switch No. 1) R
6	O1 to P10 (decoded up counter steps sequencer) G
7	O10 to Q8 (input to driver No. 3) R
8	R8 to K4 (enable heavy duty driver No. 2) R
9	F4 (detect zero on down counter) to S9 (one-shot input heavy duty driver No. 2) G
10	Set the down counter thumbwheel No. 1 at desired number of events
11	Set the up counter thumbwheel switch No. 1 for run-time (10 sec)
12	Choose desired fixed (RC) pulse width from K990's and wirewrap to F28P (see Section 2.10 of handbook, Step no. 3 and Control Handbook – K323 description).



R = RED
G = GREY

Sequence 1

Step	Procedure
1	L9 (Step 1 of sequencer) to G9 (enable down counter thumbwheel switch No. 2) R
2	F9 to B2 (enable 10 sec to down counter input) R
3	C2 to M10 (down counter to zero steps sequencer) G
4	Set the down counter thumbwheel No. 2 for time out (10 sec)



R = RED
G = GREY

Sequence 2

Step	Procedure
1	L8 (Step 2 of sequencer) to D5 (sequencer step set memory gate) R
2	E5 to B6 (enable .1-sec to down counter) R
3	C6 to D2 (recycle down counter on zero) R
4	E2 to R1 (enable up counter thumbwheel switch No. 2) G
5	Q1 to P9 (decoded up counter steps sequencer) R
6	O9 to C10 event recycles down counter (input to driver No. 7) G

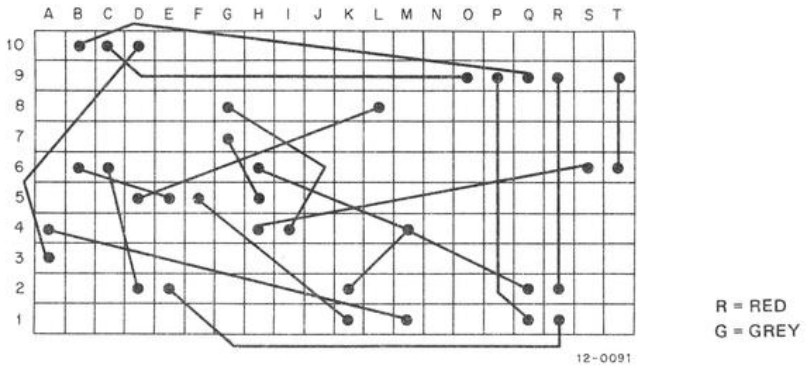
Sequence 2 (Cont)

Step	Procedure
7	B10 to Q9 (input to driver No. 7) G
8	R9 to R2 (enable 60 sec to up counter) R
9	Q2 to H6 (disable right event) to K2 (enable heavy duty driver No.4) *
10	** T9 (zero detected on down counter) to T6 (one-shot input HD driver No. 4) R
11	***S6 (zero detected on down counter) to H4 (reset memory flip-flop) G
12	A4 (left event) to M1 (input to one-shot for independent timing) G
13	K1 (*normal output* of one-shot) to F5 (event enable set memory gate) R
14	A3 (*left* event) to D10 (reset .1 sec) R
15	I4 (set memory output) to G8 (enable down counter thumbwheel No. 3) R
16	H5 (set memory output) to G7 (enable down counter thumbwheel switch No. 4) R
17	Set the up counter thumbwheel switch No. 2 at run-time (min.)
18	Set the down counter thumbwheel switch No. 3 at R. S. time (.1 sec)
19	Set the down counter thumbwheel switch No. 4 at S. S. time (.1 sec)
20	Set the upper potentiometer for max. (downward)
21	Set lower potentiometer for reinforcement time

* 3 leg "Y" patchcord

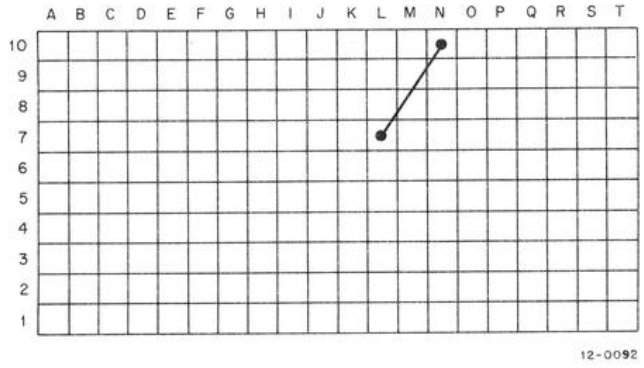
** Continued from step 9 sequence 0

*** Continued from step 10 sequence 2



Sequence 3

Step	Procedure
1	L7 (Step 3 of the sequencer) to N10 (Step 1 time out enabled) R
2	Set sequencer thumbwheel to no. 3
3	Equipment List: LAB-K A, B, C, D, E, F, G, H, K, L, R or J (needed for schedule) LAB-K B1, C2, E1 (recommended for schedule)



R = RED
G = GREY

5.11 GENERAL TROUBLESHOOTING PROCEDURE

NOTE

Review the basic logic functions as outlined in Chapter 3 before going on to General Troubleshooting. This information is essential to effective troubleshooting of the LAB-K. Further information on logic is available in the new K Series Logic Lab Workbook (DEC No. 042X-00270-AKP. This may be obtained by filling out the appropriate return reply card.

The Up Counter will be used as an example to establish a troubleshooting technique which LAB-K users can follow to track down a variety of problems. (The example to be used is shown in logic schematic X602-0-7.) Return to the checkout procedure of Application E (Section 5.2.8) and follow the explanation of this checkout procedure through Step 1, rewiring the Up Counter plugboard accordingly.

Malfunction: The Up Counter does not count.

Step	Procedure
1	( ) Check the clear lines to the three K210s – the Up Counter clear lines.
	( ) a. Place test probe on C10K (shown at coordinates 2D). This line should be sitting high. If it is sitting low (+0 Vdc), the counter cannot count (this is true for all K210, K211 and K220 counters).
	Assuming that the logic source of this signal is low, the source of the low position must be found. In this case, two possible sources exist: the Manual Reset Pulse; and the Automatic Reset Pulse.
	The Manual Reset Pulse comes from E4R, at coordinates C4, while the Automatic Reset line is found at E4K, at coordinates B3 of the logic schematic. Both of these points should be sitting high (+5 Vdc) and will follow the MASTER RESET toggle switch, bringing both clear lines high. The user will note that the source of those signals is referred to as MASTER RESET on the logic schematic (X602-0-5; coordinates B8).
2	If the MASTER RESET line is sitting high and the counter still does not count, the user should place the test probe on C12F. This is the input to the counter and, when functioning, should follow the train of pulses for its time base (previously determined on the plugboard to be a 1-second increment while on Step 0).

Step	Procedure
3	If the time base is not found on this point, place the test probe on D12D. If the time base is still not found, place the test probe on D10J. If the signal is not present at D10J, the user should review the logic of the Timing Kit to facilitate further troubleshooting (refer to logic schematic X602-0-5).
4	If timing pulse is present at D10J, check D10K (the enabling level controlled by the programming plugboard) which should be sitting high. If it is not, make certain the plugwire is connected to the proper position on the plugboard (coordinates Q4 or R4).

The path which the time base should take in order to count up on the Counter has been traced. The source having been traced, the potential problem should have been found.

Malfunction: The number set in BCD Thumbwheel Switches (Group No. 1) not detected.

Step	Procedure
1	If the number had been detected, it would have set the memory flip-flop located at coordinates B3 (on logic schematic X602-0-7). The memory flip-flop consists of a K124 module; its output pin is F18R. This memory flip-flop, after detecting the number, normally sits high. If it is not high (i.e., the number has not been detected), check the OR gate output located at F18K.
2	This point should go from high to low when the Up Counter reaches the number set on the Thumbwheel Switches. If this does not occur, the next checkpoint is D9U where the same signal as at F18K should be present.
3	At this point, check C13R which should go from high to low. If it does not, check D13P and verify that it is sitting high. If it is not high, check the programming plugboard to determine if F9 or G9 is connected directly or indirectly to Step 0 on the Sequencer and therefore sitting low.
4	The only other possible sources of this malfunction would be the counter is not counting up properly because of defective modules or defective wiring between modules. This can be readily determined by inspecting the input/output pins of the K210s (according to the description of these modules found in Chapter 3).
5	If the counter is counting, the wiring before and after the BCD Thumbwheel Switches must be either miswired or defective.
6	Outputs of the K424 BCD Thumbwheel Decoder can only be recognized by an oscilloscope; therefore, all signals between expander gates and other respective amplifying gates (K113, K123) require an oscilloscope to detect such short signal pulses.

The above troubleshooting procedure describes the method used to check out all other logic kits and functions in LAB-K. Always check back from the signal desired (but missing) on the plugboard to the source of the problem.

CHAPTER 6
ENGINEERING DRAWINGS

The following is a list of the Engineering Drawings used in the LAB-K.

Drawing Number	Title
D-BS-X602-0-6	LAB-K Patchboard Functional Location
D-BS-X602-0-5	LAB-K Application Option A + D, L
D-BS-X602-0-9	LAB-K Application B
D-BS-X602-0-3	LAB-K Application C
D-BS-X602-0-7	LAB-K Application E, M
D-BS-X602-0-2	LAB-K Application F
D-BS-X602-0-4	LAB-K Application N, Q
D-BS-X602-0-8	LAB-K Application P
D-MU-X602-0-10 (2 Sheets)	Module Utilization
D-UA-LAB-K-0 (5 Sheets)	LAB-K Unit Assembly

APPENDIX A
NUMBER SYSTEMS

A.1 INTRODUCTION

With the arabic or decimal number system in use today, common arithmetic operations can be defined and easily used.

The decimal number system uses ten symbols representing quantities zero through nine. Other numbers are constructed by assigning different values (or weights) to the position of the symbol relative to the decimal point. For example, the number 008 (commonly written 8) represents eight units, while the number 080 (commonly written 80) represents a quantity of eighty units, and the number 800 represents a quantity of eight hundred units.

Examining the decimal number system, it is apparent that each position in a number has a value that is ten times the value of the next position on the right. In other words, the value of every position is a multiple of ten and can be expressed by ten raised to some power. The tens position is 10^1, the hundreds position is 10^2, the thousands position is 10^3, etc.

Simple exponential arithmetic shows that the ones position is $10^0 = 1$ (any number raised to the zero power is equal to 1). This progression of increasing exponents can be continued indefinitely to the left of the decimal point.

The same progression can be extended to the right of the decimal point, but here the exponents are negative. For example, the first position to the right of the decimal point is the tenths position; it has a value of 10^{-1} or $1/10^1$. Figure A-1 represents a general skeleton for any decimal number. A particular symbol placed in a particular position indicates the number of multiples of the power of ten in the total quantity represented by the number.

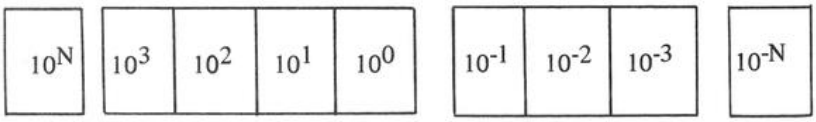


Figure A-1 Skeleton of Decimal Number System

Ten is not a magic number; there is no reason for the number of symbols to be extended to ten (or limited to ten). It would be just as simple to have twelve symbols or eight symbols or two symbols, or any number of symbols. One feature of the decimal system is that there is only one way that any given number can be written; and there is only one value represented by a particular written number. To keep this feature, in a number system with a different number of symbols, it is necessary to change the positional values of the different positions. The values that must be assigned are, in fact, multiples of the number of symbols available. (Experimenting with different number systems demonstrates this.)

Figure A-2 represents the skeleton of a general number system with a radix R.

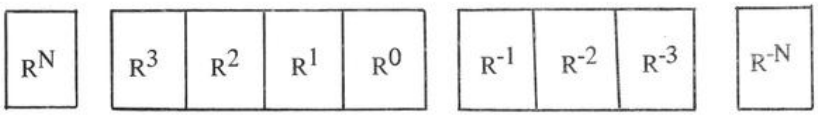


Figure A-2 Skeleton of General Number System

Table A-1 illustrates methods of counting in different number systems. The duodecimal number system has a radix of twelve; the symbols A and B are used here to represent the quantities eleven and twelve respectively. The octal number system has a radix of eight and the binary number system has a radix of two. The positional values are given in decimal at the top of each column.

Table A-1
Counting in Different Number Systems

Decimal	Duodecimal	Octal	Binary
Tens	Dozens	Eights	Sixteens Eights Twos Ones
0	0	0	0
1	1	1	1
2	2	2	10
3	3	3	11
4	4	4	100
5	5	5	101
6	6	6	110
7	7	7	111
8	8	10	1000
9	9	11	1001
10	A	12	1010
11	B	13	1011
12	10	14	1100
13	11	15	1101
14	12	16	1110
15	13	17	1111
16	14	20	10000
17	15	21	10001
18	16	22	10010
19	17	23	10011
20	18	24	10100
21	19	25	10101
22	1A	26	10110
23	1B	27	10111
24	20	30	11000

A.2 BINARY NUMBERS

When there are only two unique states to work with, a counting system can be evolved: this is the binary or two-state counting sequence. Table A-2 shows the binary count sequence and decimal numbers of corresponding value. Digital computers are composed of two-state logic elements which can use the binary system. Just as the decimal system is based on powers of 10, the binary system is based on powers of 2. Each binary digit carries a weight or multiplier which is a power of 2, as shown in Table A-2. The least significant, or right-most digit, carries a weight or multiplier of 2^0 or 1; the next most significant binary digit carries a weight or multiplier of 2^1; the next most significant binary digit carries a weight or multiplier of 2^2 and so on. A decimal number is weighted with the right-most column having a multiplier or weight of 10^0; the next most significant column has a multiplier of 10^1 or 10; the next most significant column has a weight of 10^2 or 100, and so on.

Table A-2
Binary Counting Sequence

Binary							Decimal		
2^6	2^5	2^4	2^3	2^2	2^1	2^0	10^2	10^1	10^0
0	0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	1	0	0	1
0	0	0	0	0	1	0	0	0	2
0	0	0	0	0	1	1	0	0	3
0	0	0	0	1	0	0	0	0	4
0	0	0	0	1	0	1	0	0	5
0	0	0	0	1	1	0	0	0	6
0	0	0	0	1	1	1	0	0	7
0	0	0	1	0	0	0	0	0	8
0	0	0	1	0	0	1	0	0	9
0	0	0	1	0	1	0	0	1	0
0	0	0	1	0	1	1	0	1	1
0	0	0	1	1	0	0	0	1	2
0	0	0	1	1	0	1	0	1	3
0	0	0	1	1	1	0	0	1	4
0	0	0	1	1	1	1	0	1	5
0	0	1	0	0	0	0	0	1	6
0	0	1	0	0	0	1	0	1	7
0	0	1	0	0	1	0	0	1	8
–	–	–	–	–	–	–	–	–	–
–	–	–	–	–	–	–	–	–	–
–	–	–	–	–	–	–	–	–	–
1	1	0	0	1	0	0	1	0	0
1	1	0	0	1	0	1	1	0	1
1	1	0	0	1	1	0	1	0	2

A.3 DECIMAL-TO-BINARY CONVERSION

To convert a binary number into decimal, add the decimal weights of each binary bit which is a 1. Thus the binary number 1001100 is equivalent in value to the decimal number $2^6 + 2^3 + 2^2 = 76$. This binary-to-decimal conversion suggests a method for converting decimal numbers into binary numbers.

That method is to subtract the largest power of 2 which is less than or equal to the decimal number being converted. The second step is the same as the first and it is performed on the remainder from the first step. The process continues until the remainder of successive subtractions equals 0. Example, convert 76 into binary.

$$76 - 2^6 = 12$$
$$12 - 2^3 = 4$$
$$4 - 2^2 = 0$$

Thus 76 equals $2^6 + 2^3 + 2^2$. As shown in Table A-2, the 2^2 is the third position from the right of a binary number; 2^3 is the fourth position from the right of a binary number; 2^6 is the seventh position from the right in a binary number. The binary equivalent of a decimal number 76 is, therefore, 1001100.

Table A-3
Decimal Equivalents of Binary Numbers to 2^8

Decimal	Binary	Decimal	Binary	Decimal	Binary	Decimal	Binary
180	10110100	199	11000111	218	11011010	237	11101101
181	10110101	200	11001000	219	11011011	238	11101110
182	10110110	201	11001001	220	11011100	239	11101111
183	10110111	202	11001010	221	11011101	240	11110000
184	10111000	203	11001011	222	11011110	241	11110001
185	10111001	204	11001100	223	11011111	242	11110010
186	10111010	205	11001101	224	11100000	243	11110011
187	10111011	206	11001110	225	11100001	244	11110100
188	10111100	207	11001111	226	11100010	245	11110101
189	10111101	208	11010000	227	11100011	246	11110110
190	10111110	209	11010001	228	11100100	247	11110111
191	10111111	210	11010010	229	11100101	248	11111000
192	11000000	211	11010011	230	11100110	249	11111001
193	11000001	212	11010100	231	11100111	250	11111010
194	11000010	213	11010101	232	11101000	251	11111011
195	11000011	214	11010110	233	11101001	252	11111100
196	11000100	215	11010111	234	11101010	253	11111101
197	11000101	216	11011000	235	11101011	254	11111110
198	11000110	217	11011001	236	11101100	255	11111111

A.4 BINARY-TO-DECIMAL CONVERSION

Binary-to-decimal conversion can be accomplished by hand using the methods outlined in Figure A-3.

A binary number can be converted to decimal by adding the positional values of all those positions where a 1 appears.

Decimal-to-binary conversion is a process of trial and error (see Figure A-4). First, subtract the largest power of 2 which will factor into the number that is being converted. This process is repeated on the remainder until the remainder is equal to zero.

```
32  16  8 4 2 1
 1   0  1 1 0 1 = 32 + 8 + 4 + 1 = 45
        1 0 1 0 = 8 + 1 = 10
 1   1  0 1 1 1 = 32 + 16 + 4 + 2 + 1 = 55
```

Figure A-3 Binary-to-Decimal Conversion

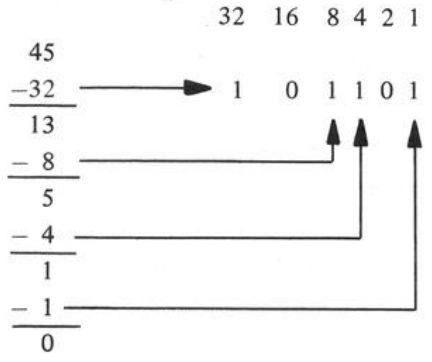


Figure A-4 Decimal-to-Binary Conversion

A.5 BINARY-CODED-DECIMAL NUMBERS

Because computer inputs and outputs often must be in decimal notation, a variety of special codes are used. These hybrid number systems are referred to as binary-coded-decimal or BCD.

An example of BCD is the 8421 code. This code is referred to as BCD because the values of the positions are the same as in the binary number system, as illustrated below.

Decimal	8421 Code
0	0000
1	0001
2	0010
3	0011
4	0100
5	0101
6	0110
7	0111
8	1000
9	1001

The 8421 code employs four bits to represent each decimal digit. For instance, the number 987 can be represented by the 12-bit number 1001 1000 0111. Although this number contains only ones and zeros, it is not a true binary number because it does not follow the rules previously established. Arithmetic operations with BCD are quite involved. However, it is relatively easy for the computer to convert to true binary, perform the necessary calculations, and reconvert to BCD.

A.6 THE OCTAL NUMBER SYSTEM

The octal number system has a radix of eight, i.e., it uses eight discreet symbols: 0, 1, 2, 3, 4, 5, 6, 7. The positional values in the octal number system are powers of eight.

The octal number system is widely used by digital engineers and computer programmers, because it is easily converted to binary. It is also considerably easier to work with, or to record octal numbers than to use a long string of binary zeros and ones.

The binary-to-octal conversion can be performed quite simply due to the fact that eight is the third power of two. This fact produces a direct correlation between the successive three-bit groups in a binary number and the octal digits. In other words, an octal number can be converted to binary digit by digit, while with a decimal number the entire number must be converted to binary. The table for octal-to-binary conversion is shown in Figure A-4.

Octal	Binary
0	000
1	001
2	010
3	011
4	100
5	101
6	110
7	111

Figure A-5 Octal-to-Binary Conversion

Using this table, the octal number 777, for example, can be easily and directly converted to the binary number 111111111; conversely the binary number 110101110 can be converted directly to 656. (As in other number systems, zeros are always assumed in the most significant bits. For example, the number 1110110 converts to 166 in octal.)

APPENDIX B

DECIMAL EQUIVALENTS OF BINARY NUMBERS TO 2^8

Table B-1

Decimal Equivalents of Binary Numbers to 2^8

Decimal	Binary	Decimal	Binary	Decimal	Binary	Decimal	Binary
0	00000000	45	00101101	90	01011010	135	10000111
1	00000001	46	00101110	91	01011011	136	10001000
2	00000010	47	00101111	92	01011100	137	10001001
3	00000011	48	00110000	93	01011101	138	10001010
4	00000100	49	00110001	94	01011110	139	10001011
5	00000101	50	00110010	95	01011111	140	10001100
6	00000110	51	00110011	96	01100000	141	10001101
7	00000111	52	00110100	97	01100001	142	10001110
8	00001000	53	00110101	98	01100010	143	10001111
9	00001001	54	00110110	99	01100011	144	10010000
10	00001010	55	00110111	100	01100100	145	10010001
11	00001011	56	00111000	101	01100101	146	10010010
12	00001100	57	00111001	102	01100110	147	10010011
13	00001101	58	00111010	103	01100111	148	10010100
14	00001110	59	00111011	104	01101000	149	10010101
15	00001111	60	00111100	105	01101001	150	10010110
16	00010000	61	00111101	106	01101010	151	10010111
17	00010001	62	00111110	107	01101011	152	10011000
18	00010010	63	00111111	108	01101100	153	10011001
19	00010011	64	01000000	109	01101101	154	10011010
20	00010100	65	01000001	110	01101110	155	10011011
21	00010101	66	01000010	111	01101111	156	10011100
22	00010110	67	01000011	112	01110000	157	10011101
23	00010111	68	01000100	113	01110001	158	10011110
24	00011000	69	01000101	114	01110010	159	10011111
25	00011001	70	01000110	115	01110011	160	10100000
26	00011010	71	01000111	116	01110100	161	10100001
27	00011011	72	01001000	117	01110101	162	10100010
28	00011100	73	01001001	118	01110110	163	10100011
29	00011101	74	01001010	119	01110111	164	10100100
30	00011110	75	01001011	120	01111000	165	10100101
31	00011111	76	01001100	121	01111001	166	10100110
32	00100000	77	01001101	122	01111010	167	10100111
33	00100001	78	01001110	123	01111011	168	10101000
34	00100010	79	01001111	124	01111100	169	10101001
35	00100011	80	01010000	125	01111101	170	10101010
36	00100100	81	01010001	126	01111110	171	10101011
37	00100101	82	01010010	127	01111111	172	10101100
38	00100110	83	01010011	128	10000000	173	10101101
39	00100111	84	01010100	129	10000001	174	10101110
40	00101000	85	01010101	130	10000010	175	10101111
41	00101001	86	01010110	131	10000011	176	10110000
42	00101010	87	01010111	132	10000100	177	10110001
43	00101011	88	01011000	133	10000101	178	10110010
44	00101100	89	01011001	134	10000110	179	10110011

C.1 WIRE INSULATION STRIPPING

Correct stripping of insulation is one of the most important steps in making an acceptable connection. The insulation must be completely removed, yet the conductor or conductors must not be nicked or cut.

Using the proper tools makes stripping insulation relatively easy. Diagonal cutters or knives are not the proper tools. The use of either of these tools usually results in a damaged conductor.

The correct tool to use is a wire stripper. There are two preferred types available. One type has a fixed adjustment with a different size opening for each wire size. It is virtually impossible to nick the conductor if the proper size opening is used.

The second and more common type of wire stripper has one opening and an adjustable set screw. This type of cutter is easy to use but requires constant checking to ensure undamaged conductors. With either type of tool, it is essential to regularly check the conductor for nicks. This can be done by stripping the wire twice and checking the conductor for damage at the first point of stripping.

A properly stripped piece of wire has no nicks, cuts or frayed insulation.

CAUTION

Under no circumstances can nicks reduce the area of a conductor by more than 10%.

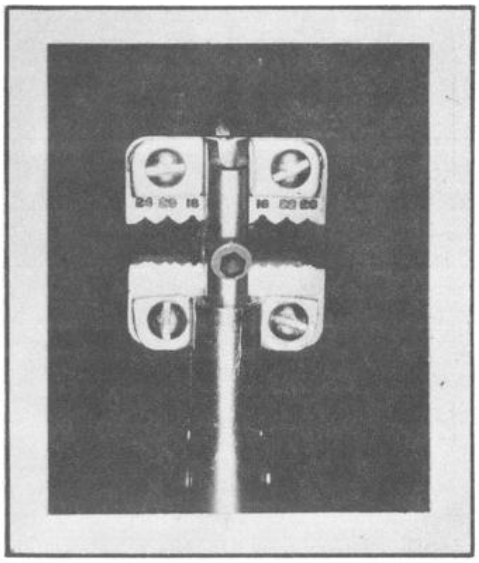


Figure C-1 Non Adjustable Wire Stripper

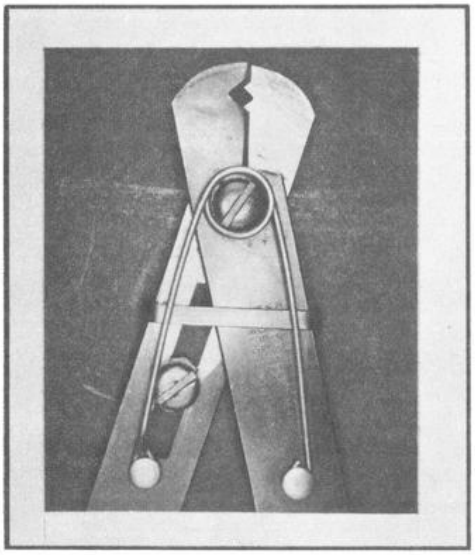


Figure C-2 Adjustable Wire Stripper (Use with Caution)

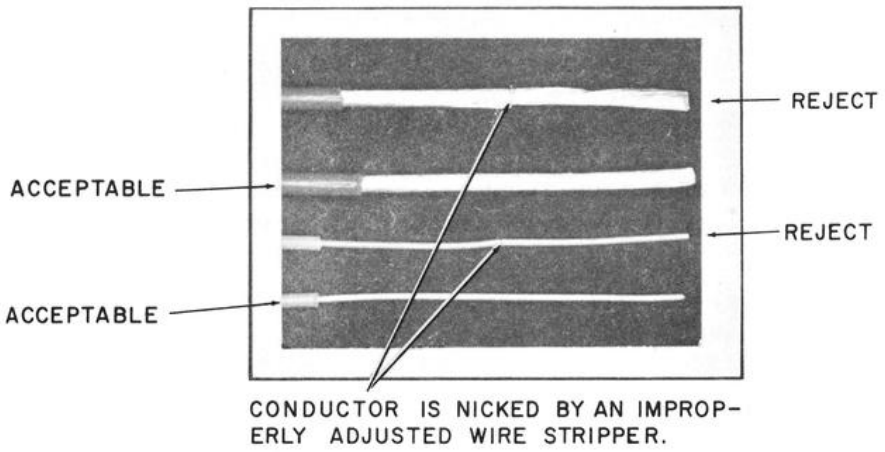


Figure C-3 Stripping Damage

C.2 SOLDERLESS CONNECTIONS

A solderless connection is a mechanical technique for fastening a wire to a post or a lug. Two basic types of solderless connections are used; 'crimped' and wire-wrap. Acceptable connections can only be obtained by the correct use of the proper tools.

C.2.1 Crimped Connections

Typical crimped connectors and proper crimping techniques are shown below. In all these connectors, a metal body is compressed around the conductor. To guarantee a reliable joint it is absolutely essential that the proper size wire, connector, and tool always be used.

The major cause of unreliable crimped connections is too loose a crimp; this occurs when hand tools are used which can be released by the operator before the joint is fully made.

CAUTION

For this reason, only ratchet type or air driven hand tools are recommended.

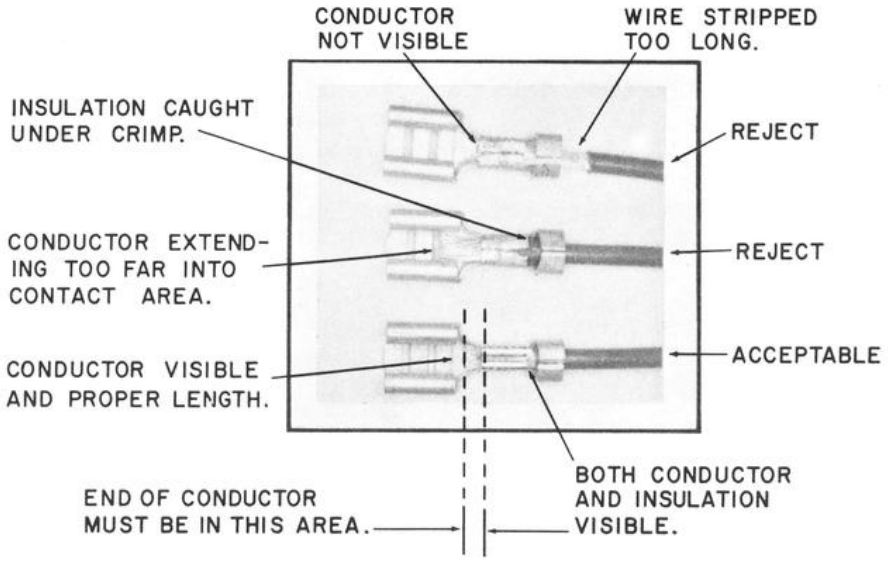


Figure C-4 Crimped Connectors

The characteristics of acceptable and unacceptable crimped connections are shown below.

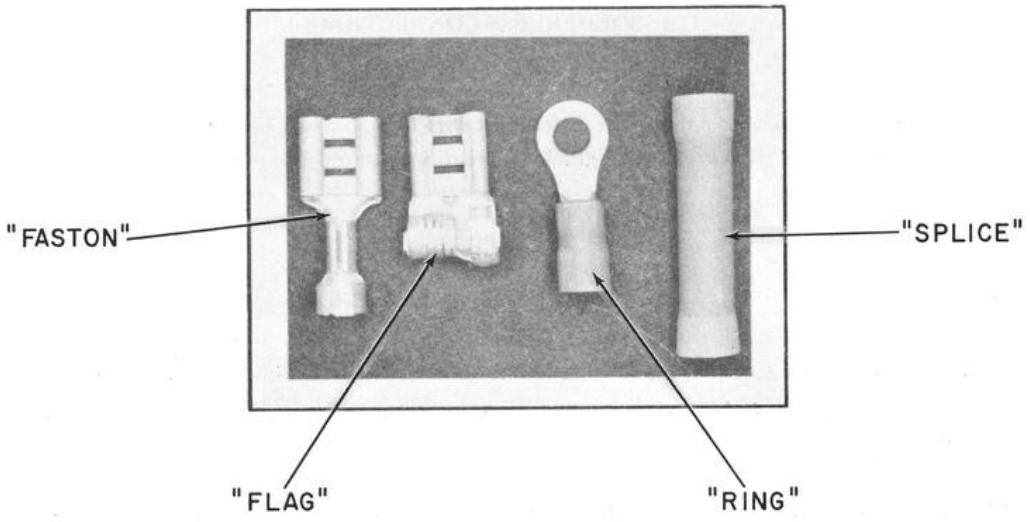


Figure C-5 Crimped Connections

C.2.1.1 **Insulating Crimped Connections** - In many applications it is necessary to place insulation around the end of the crimped connection. The most commonly used insulation is heat-shrinkable spaghetti ('shrinky'). Before putting a 'shrinky' over a crimped connection, carefully inspect the joint. Never cover a defective connection! Heat must be applied carefully or the 'shrinky' will discolor and crack. The correct tool to use is a heat gun made by Master Appliance Corp., Model HG 501 lg. The heat gun should be held four to six inches from the work. The spaghetti shrinks completely in about 4 seconds, with the cover on the side of the heat gun completely open. When shrinking spaghetti in an assembly, make certain that you do not damage some painted surface or plastic part beyond the joint.

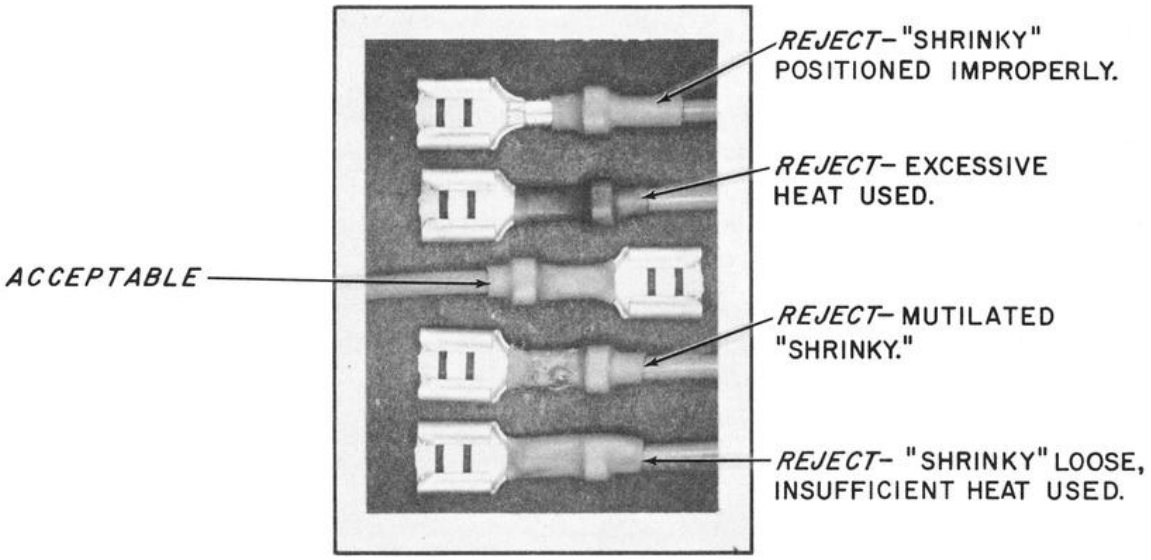


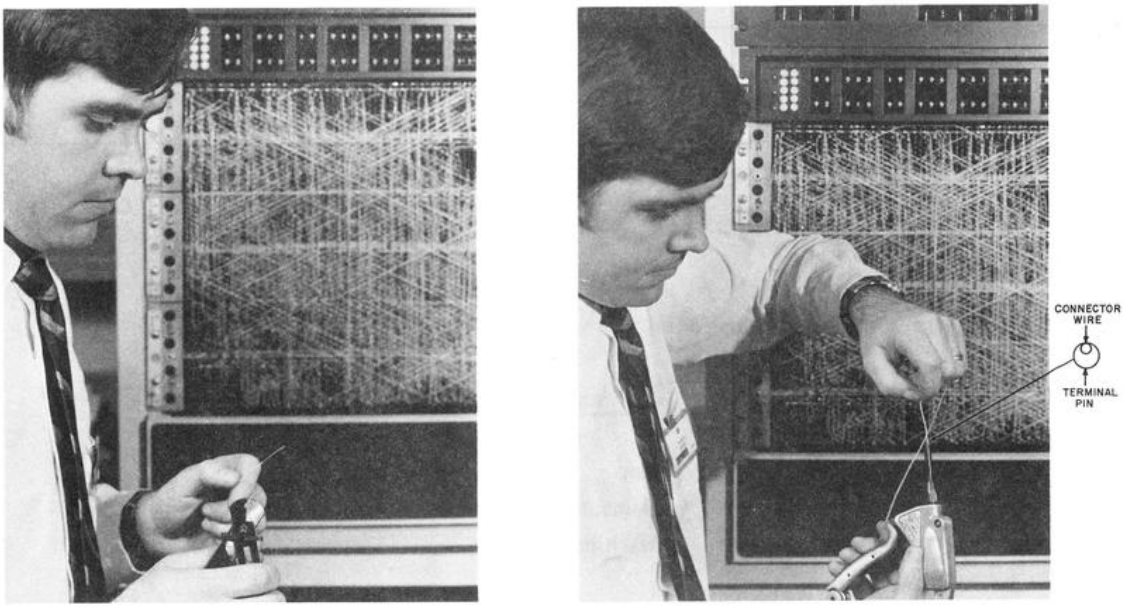
Figure C-6 Properly and Improperly Shrunk Spaghetti

C.3 WIRE WRAP

Wire wrapping is used for fairly small (#24-0) solid wire in repetitive applications. It evolved as the only economical way to easily make a large number of connections.

A wire-wrapped joint is made by tightly wrapping a bare conductor around a rectangular post. The post has sharp edges which cut into the wire as it is wrapped. In a properly made joint, the pressures at the edges of the post, are high enough to cause a cold weld to take place. For every complete turn around the post, four welds are made, one at each corner. In a typical joint the wire makes six full turns and therefore it is fastened to the post at twenty-four places.

The most efficient way to make a wire-wrapped joint is to use a H810 Pistol Grip Hand Wrapping tool. The gun is shown in the sequence below. Wire-wrapped connections can be removed with a H812 Hand Unwrapping Tool. This tool can be purchased from Gardner-Denver Co. (Part 500130).



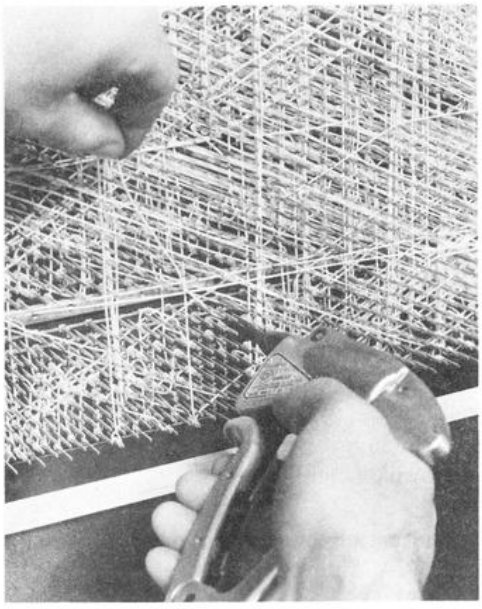


Figure C-7 Wire-Wrap Procedure

Chart of Tools, Wire Size, and Wrapping Requirements for Connectors

Wire Gauge	Connector Type	Stripping Length (Inches)	Gardner Denver Bit #	Gardner Denver Sleeve #	Turns of Wire		Turns of Insulation		Pull Test Requirements (lbs)		Gardner Denver Unwrapping Bit
					Min	Max	Min	Max	Min	Max	
#24	1144 Pin (H8000W) Part #12-02244	1-1/2	26263	18840	4-1/2	6	1/2	2	7	35	5000-30-L-E

C.3.1 **Wire Color Codes**

The following is a description of wire color codes.

Wire	Description	Color
AC Power Cord	Hot	Black
	Neutral	White
	Machine Ground	Green
Logic Wiring		Red (+28 Volts)
		Orange (+5 Volts)
		Black (0 Volts) Ground

C.3.2 **Wire-Wrap Terminology Requirements (See Figure C-9)**

The most important factor in making reliable-wire-wrap joints is the use of the correct tools. Always use the bits and sleeves outlined in the tool chart. Check the condition of the wire-wrap post making the connection. It must meet the following requirements (Figure C-9).

a. No more than a 15° twist.

b. No more than 10° from the vertical.

c. No solder build-up over .003 inches.

d. Post not damaged.

The routing of the wire must meet the following requirements:

a. The wire must be positioned such that subsequent routing of the wire does not tend to unwrap the joint.

b. Wires should be routed for the shortest practical length.

c. Wires must start and end on the same level. 'LEVEL JUMPING' is not allowed.

d. Allow enough slack when routing a wire around an unused post to allow a wire wrap tool to be placed over the post without damaging the wire passing by.

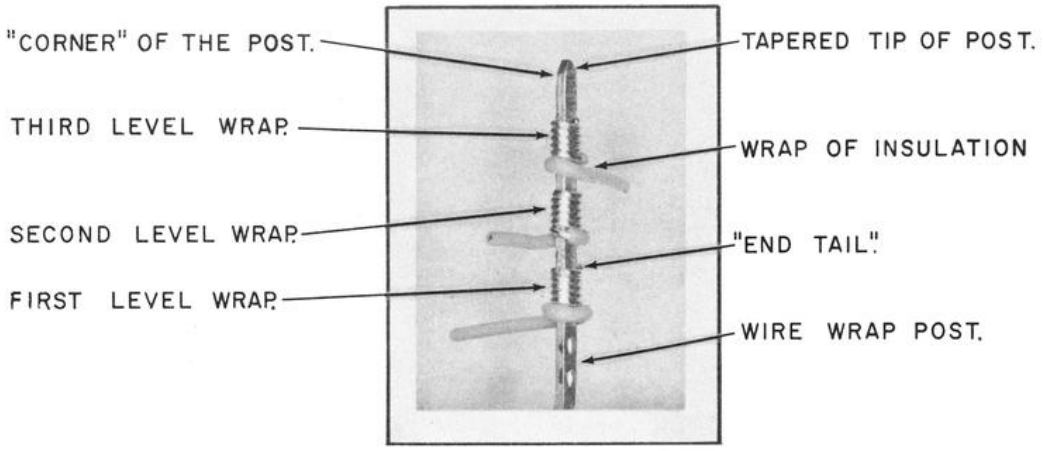


Figure C-8 Wire-Wrap Terminology

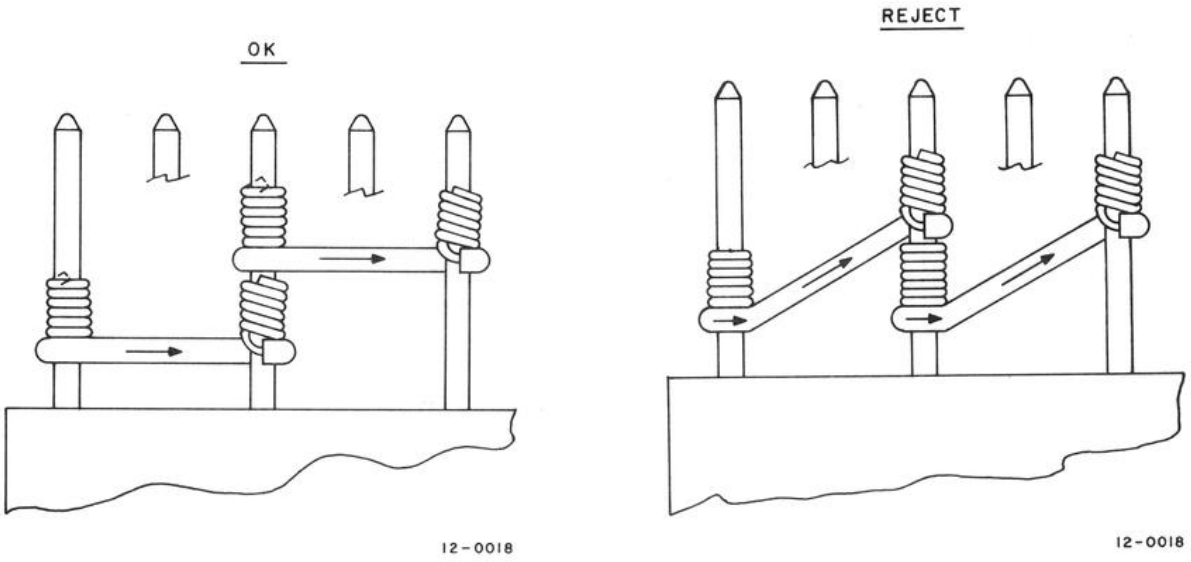


Figure C-9 Level Jumping

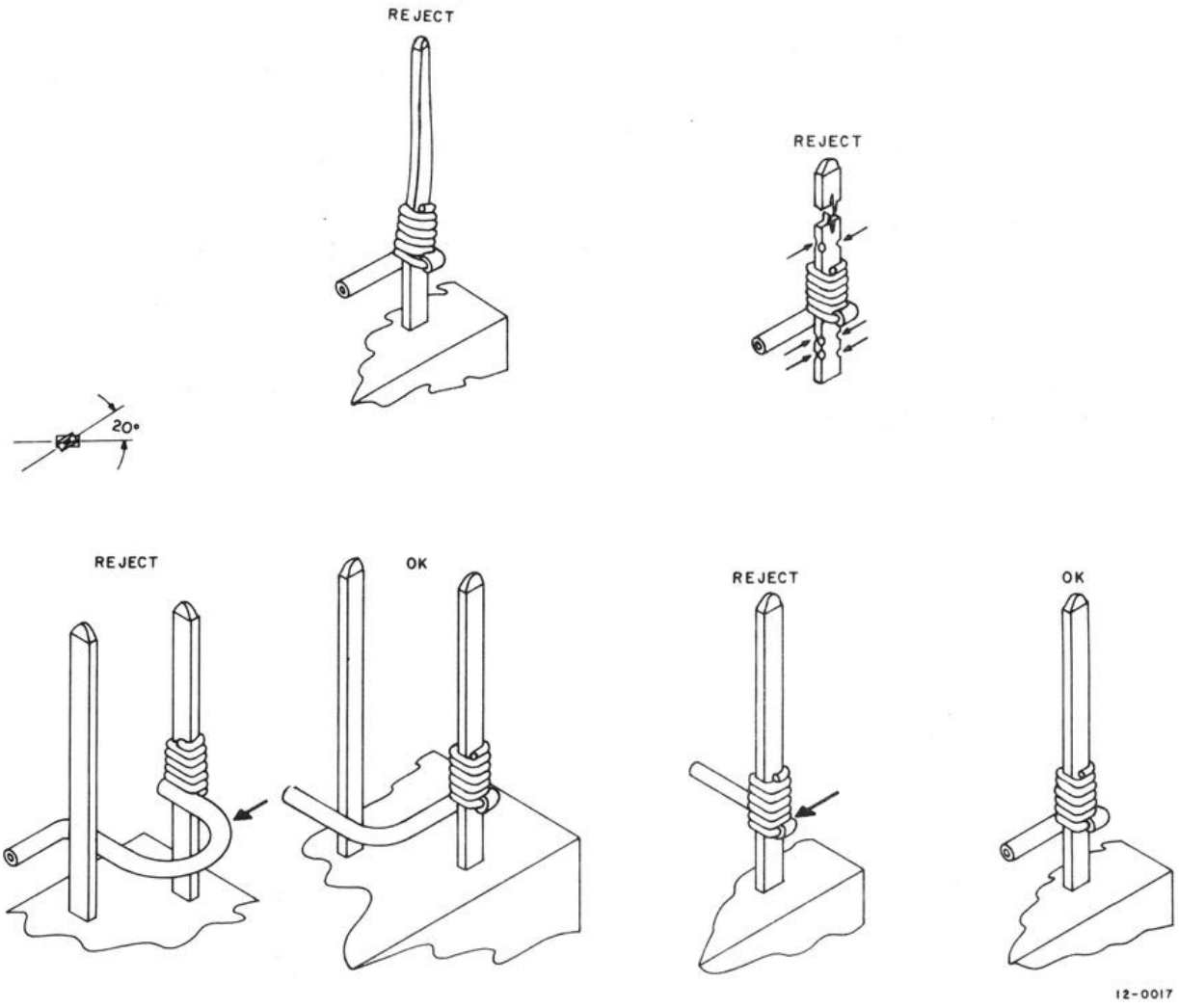


Figure C-10 Proper and Improper Wire Wrapping

C.3.3 Wire-Wrap Post Location

It is necessary to be able to locate the 'from' and 'to' end of any wire-wrap 'run'. The 'from' and 'to' is indicated by a series of four letters and numbers such as A24F. The first letter identifies the horizontal row (A24F). The rows are lettered starting with 'A' from the top of the bay. The second and third digits identify the vertical column or 'slot' in a particular row (A24F). There are 32 'slots' in a row. The second letter identifies the pin (wire-wrap post) in a given row and column (A24F). There are 18 letters used; A through V. The letters G, I, O, and Q are not used. There are twice as many 30 gauge pins as 24 gauge pins in a slot.

NOTE

If every fifth slot, starting at slot 5, is identified by a piece of red spaghetti pushed over a pin A1, then it is easy to locate a particular slot by counting from the nearest red marker.

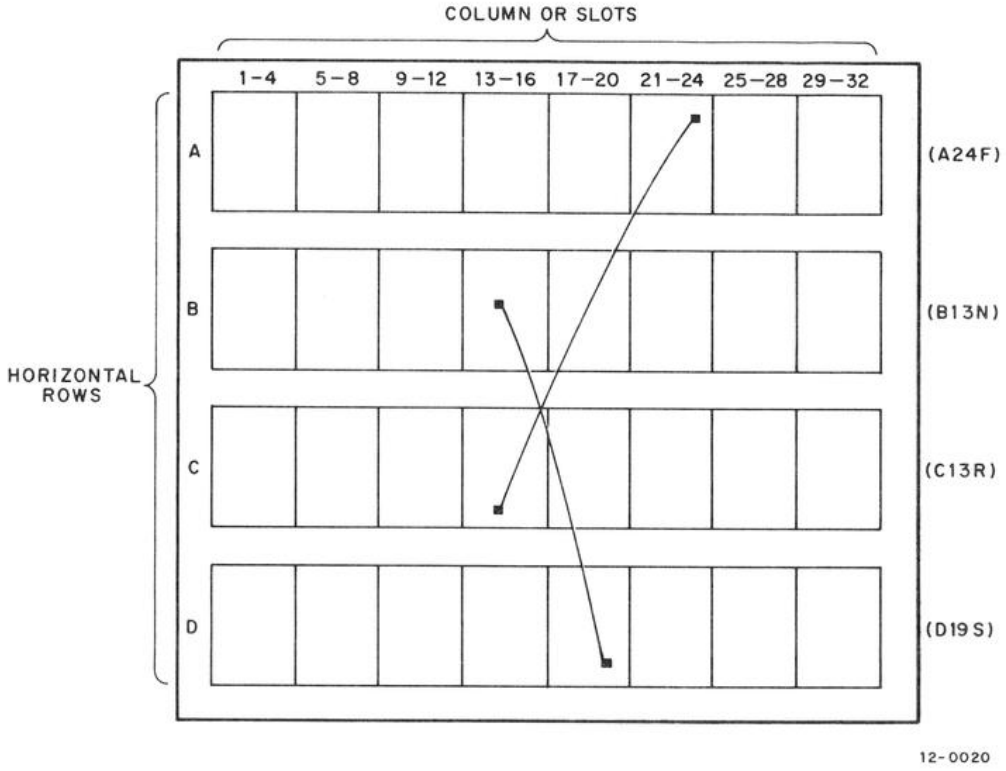


Figure C-11 Wire-Wrap Post Location Standard

A typical 'run' of 24 gauge wire would be:

From A24F to C13R (thus, a 24 gauge wire would run from row A, slot 24, pin F, to row C, slot 13, pin R.)

APPENDIX D
SOLDERING

D.1 SOLDERED CONNECTIONS

In a soldered connection, a metal alloy is melted, flows around, and bonds all parts of the joint.

The most commonly used alloy or solder is a 60% lead, 40% tin mixture. This type of solder is simply called 'sixty-forty'. Solder melts at a relatively low temperature about 375°F.

In a properly made joint, the solder actually forms a chemical bond to all the metal surfaces it contacts. A clean surface is essential to ensure a good chemical bond. Because all surfaces become contaminated by exposure to air, a cleaning agent is necessary. These cleaning agents are called fluxes.

Most solder contains the flux. The flux is released from the core of the solder as heat is applied. Since the flux melts at a lower temperature than solder, it cleans the surfaces of the joint just before the solder flows. Rosin flux is the only acceptable type of flux used in hand soldering.

D.1.1 Soldering Irons

The heat required to melt the solder is usually generated by an electrical soldering iron. Many soldering irons have a built in thermostat which automatically regulates the temperature of the tip.

The temperature required to solder a joint is the same, regardless of its size. A larger connection does, however, require a larger soldering iron. The 'size' of a soldering iron is measured by its wattage rating. A higher wattage soldering iron is required for a larger connection.

CAUTION

When soldering is done on a mounting panel containing modules, a 6V (transformer) soldering iron should be used. A 110V soldering iron may damage the modules.

The tips are replaceable on most soldering irons. It is recommended that you purchase this type of iron. Tips, which are subject to oxidation and corrosion, must be replaced periodically. Also, various types of soldering work require different types of tips.

For soldering requirements on the Lab-K, use either the chisel or conical tips with a 48-watt rating and a 1/8 in. or 3-1/16 in. diameter shank.

D.1.1 Soldering Iron Care

If corrosion is allowed to buildup on the tip, it acts as an insulation and prevents the right amount of heat from being transferred from the iron to the connection. To inhibit corrosion and ensure the rapid transfer of heat, the iron tip should be tinned.

When the tip is cool, remove it from the iron and place it in a vise. If the tip is copper, file the soldering area until the corrosion is removed. Remove burrs with a fine grain sandpaper or emory cloth. Iron-clad tips must never be filed, corrosion can be removed with a piece of emory cloth.

Reassemble the iron, and plug it into a power line. Wait about two minutes, and then apply a flux-core solder to the cleaned surface. When this surface is covered with melted solder, wipe off the excess solder on a wet sponge. Tinning should be done at the lowest temperature possible. The higher the temperature, the faster corrosion sets in.

A soldering iron must be routinely maintained.

a. Always clean the tip prior to use. Clean it on a wet sponge.

b. Never file the tip of a soldering iron.

c. Never clean the tip of a hot iron in any solvent; the fumes can be poisonous or the iron damaged.

d. Periodically disassemble the barrel and tip, and clean off any residue. This ensures that the tip can be replaced and will not be 'frozen' to the barrel.

D.1.2 Solder

It is essential that only the proper type of solder be used. It is recommended that 63/37 ('60/40') rosin-core wire solder be used. The wire solder is the same diameter as #20 wire.

This solder contains a fairly mild flux, which is adequate for soldering all reasonably clean joints. Solder containing stronger flux must never be used. Flux is actually a mild corrosive and must always be cleaned from the joint. Always check the label on the roll of solder.

CAUTION

Never use any solder which is marked acid core.

D.1.3 **Soldered Connection Requirements**

Wrap Requirements

a. The solder in a joint is necessary for electric continuity, not mechanical strength. Prior to soldering, a joint must be wrapped tightly and all wires must contact at least three corners of the lug or post. The joint must be tight enough to keep the wire from moving while the solder is cooling.

b. The wire must be dressed in such a manner as to minimize strain on the solder joint.

c. All wires on a joint must contact the post or lug. Do not wrap layers of wire over other wires. The lower layer may not solder and will be impossible to inspect.

Use of Stranded Wire

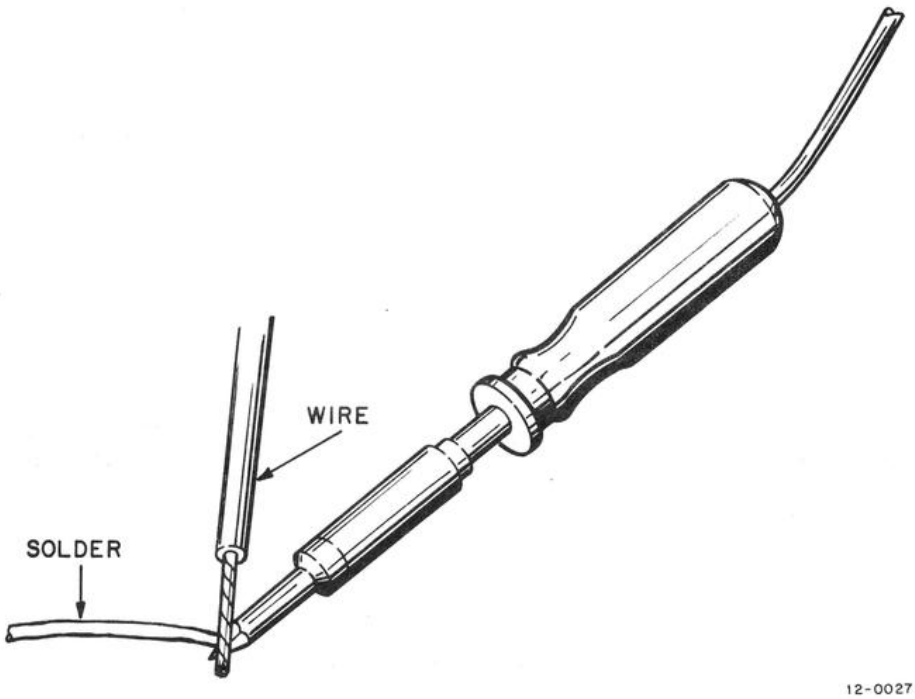
a. Stranded wire must be 'tinned' before use. Tinning involves coating and impregnating the wire with solder.

b. To tin stranded wire proceed as follows:

(1) Place the solder on a work bench.

(2) Place the stranded wire against the iron tip for a few seconds.

(3) Apply solder to the wire. If the wire is hot enough, then the solder will melt into the strands of wire, right up to the insulation.



12-0027

c. When tinning, do not allow the solder to run up under the insulation. This tends to trap flux under the insulation which may eventually cause corrosion.

d. Tin only that portion of the wire which is going to be in the joint. Tinning too much of the wire makes it stiff and decreases its flexibility.

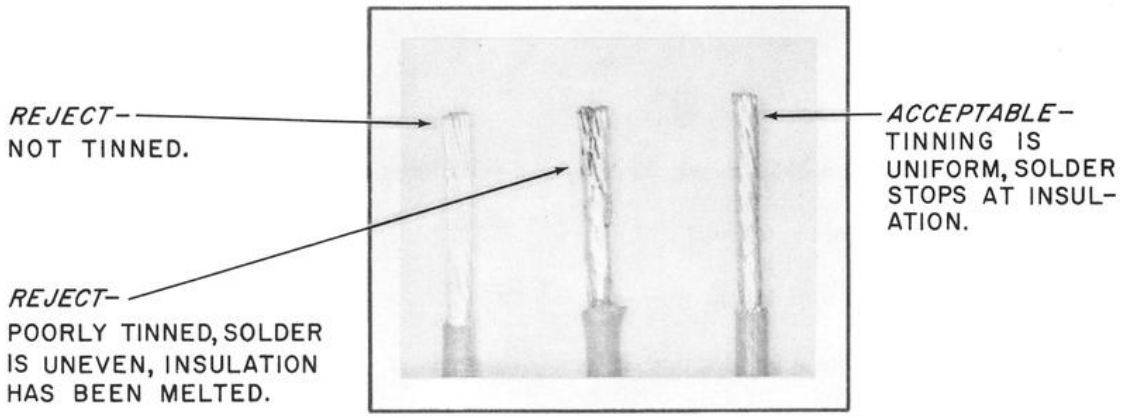


Figure D-1 Tinning Stranded Wire

D.1.4 Acceptable Joint Characteristics

The quality of a solder can be easily determined by a simple visual inspection. Characteristics of acceptable and defective solder joints are shown in the following examples.

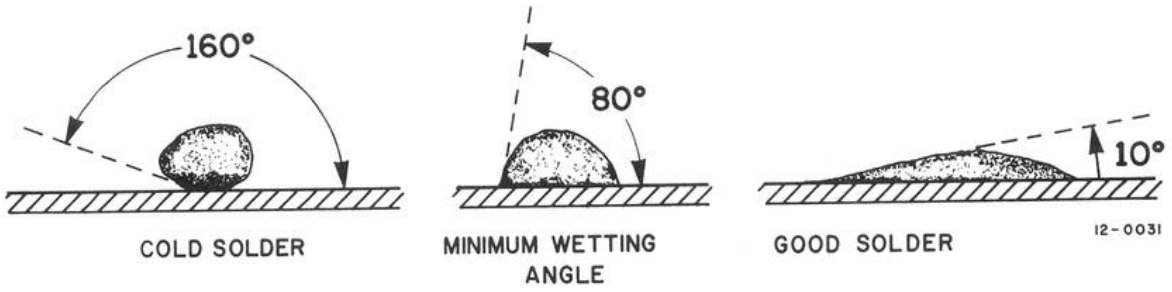


Figure D-2 Acceptable Joint Characteristics

D.2 HOW TO SOLDER

Many electronic malfunctions are the result of a poorly made solder joint. A poor solder joint, in most cases, results from not applying enough heat.

The object of soldering is to wet the base metal with solder. When solder is applied to a heated copper surface, it's flux removes the oxide coating of the parent metal. At the same instant, the melted solder flows along the copper and mixes with the surface layer of copper. This results in an alloy of tin, lead, and copper, which provides electrical continuity.

Flux reacts with a thin layer of metallic oxide, but it does not remove oil or dirt - so metal surfaces must be clean. Also, it takes a proper amount of heat to achieve good flux action and good solder wetting. Excessive heat burns the flux, which inhibits its ability to remove oxide. Insufficient heat results in poor wetting - and as a result, poor electronic continuity.

A low angle between the edge of the solder and the parent metal is characteristic of good wetting. A rounded edge is characteristic of poor wetting. Never touch the solder to the hot tip of the iron while soldering. This causes the solder to run over the surface of the joint, which results in a cold-solder. Heating the parts to be welded, and then applying the solder to the heated parts is the current soldering technique. The best results are achieved when the solder flows into all the crevices of the connection. The joint should have a shiny-ribbed appearance when it cools.

To make a solder connection proceed as follows:

Step	Procedure
1	Make a firm mechanical connection.
2	Coat the iron tip with solder, and then place the flat side of the tip firmly against the parts to be soldered. Hold the iron in place for about three seconds (count to four).
3	Place the solder between the parts to be soldered and the iron tip. Wait three seconds then remove the soldering iron. Use only enough solder to cover the metal parts. Do not move the parts until the solder is hard.
4	Check the connection and ensure the wetting is satisfactory. Compare your connection with those shown below.

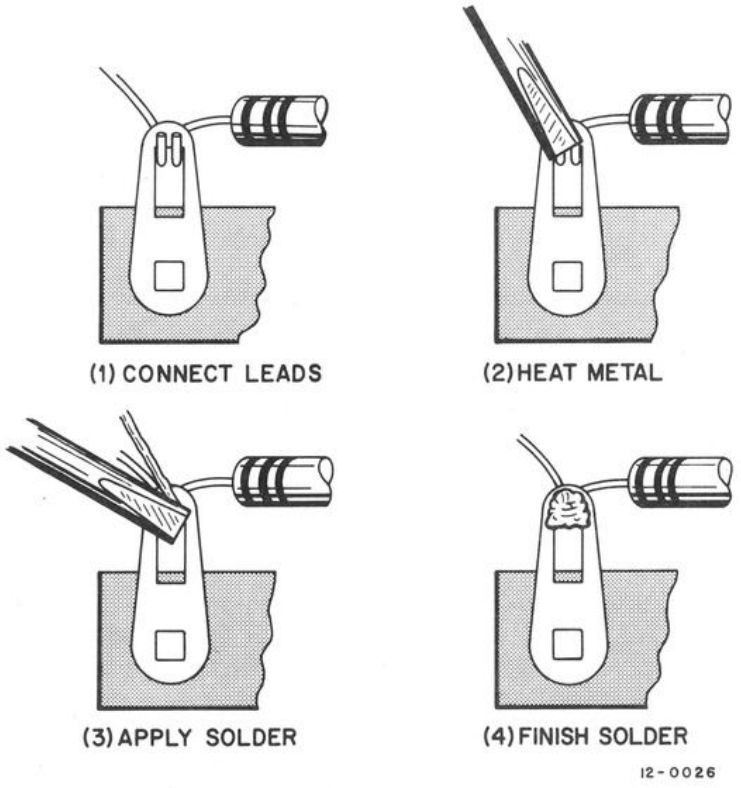


Figure D-3 Soldering Connections

To remove a soldered component proceed as shown in the following figure.

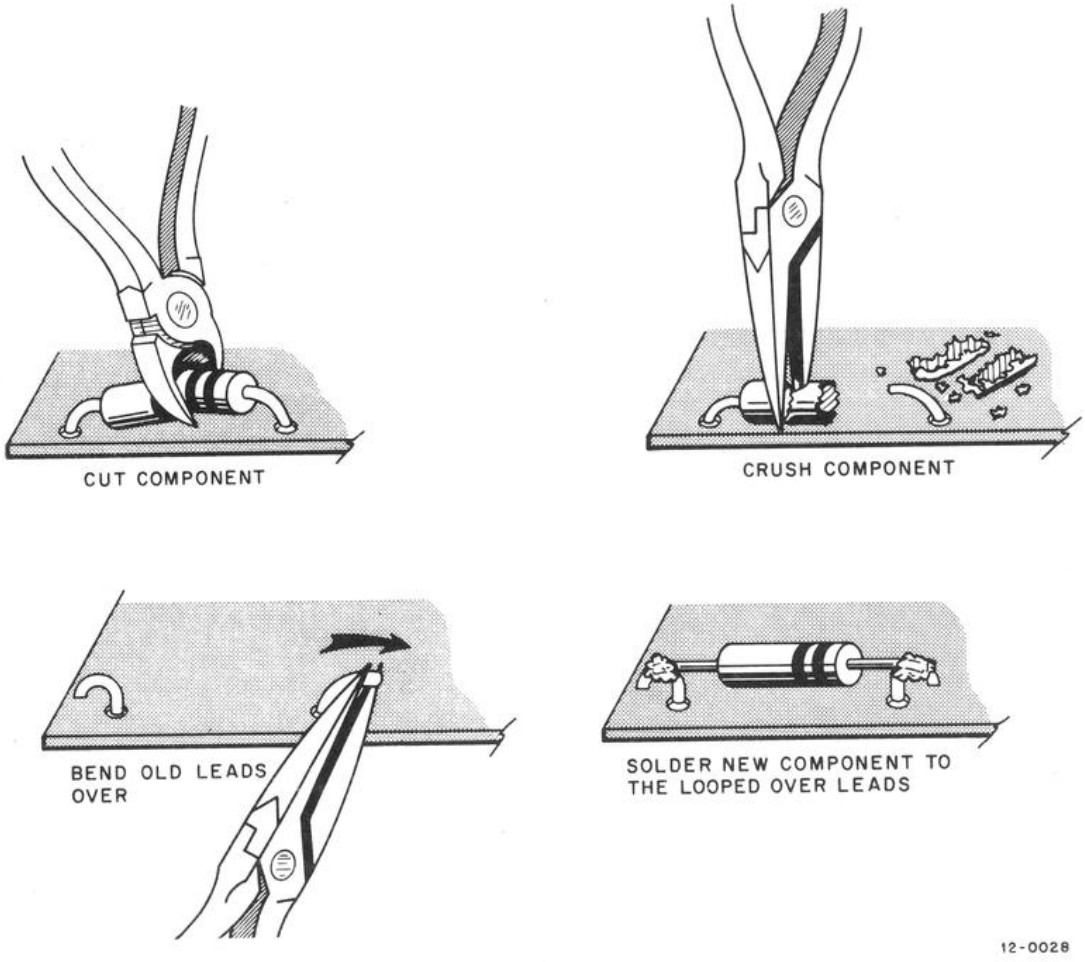


Figure D-4 Removal of Soldered Component

APPENDIX E
GLOSSARY OF TERMS

ASYNCHRONOUS–An asynchronous device is one which does not have all elements of that device operating at the same time. For example, an asynchronous counter does not have all bits of the counter operating simultaneously. The information which causes a bit to complement in an asynchronous counter must ripple through all less significant bits.

BINARY–The binary number system is one which has only two states. "0" and "1" are the two binary digits.

BINARY CODED DECIMAL–Four or more bits of binary information can be used to encode one decimal digit. When a decimal digit is encoded in this way it is called a Binary Coded Decimal (BCD).

BIT–The words "binary digit" are often abbreviated to BIT.

CARRY–In performing binary additions one bit of information often has to be carried from one section of the addition to the next most significant section. This bit of information is called a "carry bit." The carry flip-flop in a serial adder stores the carry information of one addition and presents it to the next most significant addition.

CLOCK–The clock in a digital system is used to provide a continuous train of pulses.

CLOCKED R-S FLIP-FLOP–The clocked R-S flip-flop has two conditioning inputs which control the state to which the flip-flop will go at the arrival of the clock pulse. If the S (Set) input is enabled, the flip-flop goes to the "1" condition when clocked. If the R (Reset) input is enabled, the flip-flop goes to the "0" condition when clocked. The clock pulse is required to change the state of the flip-flop.

COUNTER–The counter is a device that maintains a continuous record of the number of pulses which it has received at its input. The output of the counter indicates the sum of the number of input pulses.

D-TYPE FLIP-FLOP–A D-type flip-flop propagates whatever information is at its D (data) conditioning input prior to the clock pulse, to the 1 output on the leading edge of a clock pulse.

DECODER–A decoder is a device used to convert information from a coded form into a more usable form (i.e., binary-to-decimal decoder).

DIGIT–A digit is one character in a number. There are 10 digits in the decimal number system. There are two digits in the binary number system.

ENABLE–A gate is enabled if its input conditions result in a specified output. The specified output varies for different gating functions. For instance, an AND gate is enabled when its output is High and the NAND gate is enabled when its output is Low. Sub-systems described in later experiments have function enabling inputs which allow operations to be executed on a clock pulse after the function enabling input is enabled with the correct logic level.

ENCODER–An encoder is a device which takes information in one code and encodes it into another (e.g., the decimal-to-binary encoder).

EXCLUSIVE OR–The Exclusive OR function is valid, or its value is 1, if one and only one of the input variables is present. The Exclusive OR applied to two variables is present or 1, if the 2 binary input variables are different. The Exclusive OR applied to 2 input variables is often also called half-add.

FAN-OUT–The fan-out of an output is a number which indicates the number of the unit loads an output can drive.

FLIP-FLOP–A flip-flop is a storage device which can be used to retain one bit of information. A flip-flop can be in the "1" state or the "0" state. In the "1" state, its 1 output presents a High level and its 0 output presents a Low level. In the "0" state, its 1 output presents a Low level and its 0 output presents a High level.

FUNCTION–A relationship is a function if, and only if, for every combination of input conditions there is one unique output (e.g., the AND function will be valid or present if all the input variables examined are valid).

GATE–A gate is a device whose operation can be defined by a binary logic function.

GROUND–Ground is the reference or base level from which all voltages are measured on the Lab-K.

INVERT–To invert a function or variable is to change the value of that function or variable to a 0 if it is 1, or to a 1 if it is 0.

INVERTER–An Inverter is a device which performs the invert operation. It presents at its output the inverse or complement of the information at its input.

J-K FLIP-FLOP–A J-K flip-flop has two conditioning inputs and one clock input. If both conditioning inputs are disabled prior to a clock pulse, the flip-flop will remain in its present condition when a clock pulse occurs. If the J input is enabled (High) and the K input is disabled (Low), the flip-flop will go to the 1 condition on a clock pulse. If the K input is enabled, and the J input is disabled, the flip-flop will go to the 0 condition on a clock pulse. If both the J and K inputs are enabled prior to a clock pulse, the flip-flop will complement or go to the opposite state on a clock pulse.

LEADING EDGE–The leading edge of a pulse is defined as that edge or transition which occurs first. (i.e., the leading edge of a High pulse is the Low to High transition.)

LEVEL–A level is a voltage which remains constant for a long time. There are two possible levels in the LAB-K: High or Low.

LOGIC–Logic is a form of mathematics based upon two-state truth tables. Electronic logic uses two-state gates and flip-flops to perform decision making functions.

MASTER-SLAVE–A master-slave flip-flop is one which contains two flip-flops, a master flip-flop and a slave flip-flop. A master flip-flop receives its information on the leading edge of a clock pulse and the slave or output flip-flop receives its information on the trailing edge of the pulse.

MODULUS–The modulus of a counter describes the number of distinct states which that counter has. (e.g., the modulo 10 counter has a modulus of 10 and therefore has 10 distinct states).

MODULO N COUNTER–A modulo N counter has N unique states.

NAND GATE–A NAND gate is enabled when both its inputs are present or High. When a NAND gate is enabled, its output is Low. The term NAND is a contraction of the two words NOT AND.

NEGATE–To negate a binary function or variable is to change the value of that function or variable to 1 if it is 0, or to 0 if it is 1. The symbol for negation is superscript bar ($\bar{}$).

NEGATED INPUT OR GATE–A negated input OR gate is enabled if one input or the other or both are Low. When enabled, the output of the gate is High. A NAND gate is identical to a negated input OR gate in function. The difference between a NAND gate and a negated input OR gate is merely in the way that the operation of that gate is interpreted.

NOR GATE–A NOR gate is enabled when one or more of its inputs are enabled or High. When enabled, the output of a NOR gate is Low. The word NOR is a contraction of the two words NOT OR.

OCTAL–The octal number system is one which has 8 distinct digits–namely, 0, 1, 2, 3, 4, 5, 6, 7.

PROPAGATION DELAY–The propagation delay of an electronic digital device is the time which is required to transfer information from its input to its output.

PULSE–A pulse is a voltage which goes from one level to another, remains there for a short time and then returns to the original level. A High pulse is one which goes from Low to High for a short time and then returns to Low. A Low pulse is one which goes from High to Low for a short time and then returns to High.

PULSE WIDTH–The width of a pulse is defined as the length of time for which the pulse voltage is at the second, or transient, level.

RECYCLING MODULO N COUNTER–A recycling modulo N counter is one which has N distinct states and which counts to a maximum number and recycles, on the next input pulse, to its minimum number.

RESET–If a Reset input to a flip-flop is enabled, the flip-flop will go to the "0" condition.

RING COUNTER—A ring counter is a device capable of storing several bits of information. A ring counter will accept shift instructions which will shift all the information one position at a time. If information is shifting left in a register, the value of the left-most bit will shift into the right-most bit of the register. Similarly, if the ring counter is shifting right, the value of the right-most bit will shift into the left-most bit in the register. The information will recycle in a ring counter every N shift pulses where N is the number of bits in the ring counter. A SWITCH TAIL RING COUNTER will contain the complement of the information it initially contained after N clock pulses and it will contain the same information as it started with initially after 2N clock pulses.

R-S FLIP-FLOP—The R-S flip-flop has two inputs, a Set input and a Reset input. If the Set input is enabled (High), the flip-flop goes to the "1" condition. If the Reset input is enabled (High), the flip-flop goes to the "0" condition.

SELF-STOPPING MODULO N COUNTER—A self-stopping modulo N counter has N distinct states and stops when it reaches a predetermined maximum number. It does not accept further count pulses until it is reset to a number less than the maximum number.

SET INPUT—When the Set input to a flip-flop is enabled, the flip-flop goes to the "1"condition.

SIGN BIT—When using complementary arithmetic, the left-most bit in a number is called the sign bit. If the sign bit is a 1, the number is negative. If the sign bit is a 0, the number is positive.

SYNCHRONIZE—To synchronize a level or a pulse is to make sure that the level or pulse is presented to a system or subsystem at the correct time.

SYNCHRONOUS—A synchronous device or subsystem is one which has all changes occurring simultaneously. For instance, a synchronous counter is one which has all required bit changes taking place at the same time.

TRAILING EDGE—The trailing edge of a pulse is that edge or transition which occurs last. The trailing edge of a High clock pulse is the High to Low transition.