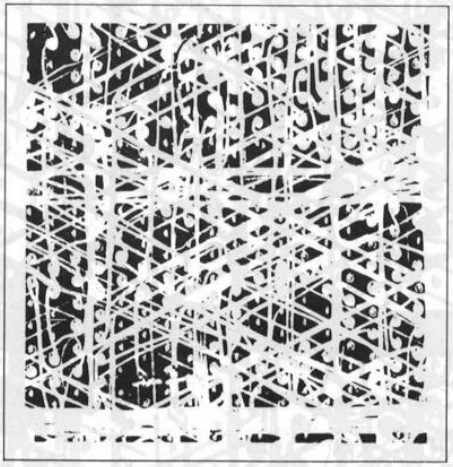
digital

FPP12 FLOATING-POINT PROCESSOR



HIGH SPEED
25 microseconds per floating-point multiply. Decreases computation time by 100 times from using software alone.

HIGH ACCURACY
Automatically maintains accuracy of 1 part per 16 million (6-7 significant figures)

LARGE DYNAMIC RANGE
Handles numbers between 10^{+620} and 10^{-620}, which includes most numbers encountered by physical problems, without losing significant figures.

PARALLEL PROCESSING
Operates independently of, but asynchronously and in parallel with, Central Processor, which provides the equivalent power of two computers.

LARGE ADDRESSABILITY
Directly addresses 32K of memory, eliminates page and field boundary constraints, thereby simplifying program development and reducing program size.

LARGE INSTRUCTION SET
34 defined instructions. Effectively requires fewer of these more powerful instructions to perform specific operations than on a less capable processor.

"RE-ENTRANT" HARDWARE
To facilitate RE-ENTRANT Programming which allows multiple tasks to utilize common programs and routines. Saves memory space and simplifies multi-user/task programming. *Base Register*—Used to simplify control of data addressing. Allows a single program to operate with multiple data files. Allows the equivalent of a moveable "PDP-8 page zero" for FPP-12 programs. *Exit and External Halt Commands*—Auto. saves and restores FPP control registers (Active Parameter Table). Allows FPP or CPU to interrupt the current task and resume its execution using only two instructions.

EXTERNAL SYNCHRONIZATION
FPP can wait for external event before proceeding with processing. Simplifies real-time processing.

MULTIPLE REGISTER INDEXING
Utilizes any 8 core locations for index registers. Simplifies list processing by performing automatic address modifications and automatic incrementing for both double-precision and floating-point data.

FORMAT FLEXIBILITY
Operates with both floating-point data (3 word) and double-precision fixed-point data (2 word).

SOFTWARE COMPATIBLE
Utilizes DEC PDP-8 standard floating-point format. (Compatible with software package DEC-08-YOYB-D).

FIELD INSTALLABLE
Can be added to any PDP-12 or PDP-8 Family Computer installation, on-site, allowing upgrading of existing systems.

SPECIFICATIONS

Typical Execution Times

Floating Point ADD	19 μsec
Floating Point SUBTRACT	19 μsec
Floating Point MULTIPLY	25 μsec
Floating Point DIVIDE	26 μsec
Floating Point NORMALIZE	6 μsec

Mechanical/Electrical

Size	21" of rack space
Power	150 watts

Ordering Information

FPP12/P	Positive Bus
FPP12/N	Negative Bus

50/60 Hz
110/220 Volts

FPP12 FLOATING-POINT PROCESSOR

FOR DIGITAL'S 12-BIT COMPUTERS

Floating Point Processor (FPP-12)

The floating-point processor (FPP-12) is a parallel processor that fetches instructions and accesses data from core memory directly. It interfaces to the standard I/O bus of DEC's widely used 12-bit machines– the PDP-8 and PDP-12. Adding the FPP-12 to the PDP-12 laboratory computer system reduces the time required to perform complex calculations by as much as two orders of magnitude.

Normalized floating-point calculations are employed to maximize precision with minimum core space. Each floating-point number is the form A*2B where A is the mantissa or binary fraction and B is an exponent. A normalized floating-point number is characterized by the fact that A doesn't contain any leading zeros. The exponent B is used to keep track of decimal point position while A is the unique or significant part of the number. Compilers, such as FORTRAN and BASIC, as well as many machines level programs use floating-point calculations. In the past, small computer systems under $100,000 had limited arithmetic capabilities. For instance, a floating-point multiply performed as a software routine typically required the execution of 400 to 1000 machines cycles in a time period of 400 to 1700 microseconds. With the FPP-12 in parallel mode, a floating point multiply requires 4 machine cycles and approximately 28 microseconds, the PDP-12 can execute, simultaneously, approximately 21 microseconds of PDP-8 or LINC code. In "straight-line" mode a floating-point multiply requires only 25 microseconds.

The FPP-12 uses the DEC standard floating-point format which includes a 12-bit signed 2's complement exponent and a 24-bit signed 2's complement mantissa. All calculations are carried to 28 bits of precision and rounded to 24 bits after normalization.

Fixed-point 24-bit fraction arithmetic is provided in the event that full 24-bit precision is less important than speed and core space. Since normalization is nor performed in fixed-point mode, leading zeros can occur to reduce precision. The decimal point position is known, therefore speed may be increased and core memory saved.

The CRT display, LINCtape, Teletype, disk and analog data acquisition proceed while the FPP-12 is performing calculations. This occurs in programs written for the Analytical Instrument Package Operating System on the PDP-12 computer.

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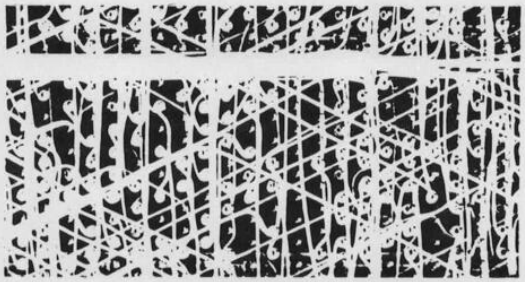

CIRCUITRY DESIGNED FOR DEPENDABILITY AND EASY MAINTENANCE

The circuitry of the FPP-12 uses the latest TTL-MSI technology. The use of MSI reduces the physical size of the arithmetic section of the hardware by a factor of 5 over standard logic elements. This permits the use of an overall architecture which is extremely flexible and inherently immune to problems caused by noise and component variation. Maintenance circuitry is included which permits diagnostic software written in PDP-12 or PDP-8 code to thoroughly check out and, when necessary, isolate malfunctions in the FPP-12. This operation significantly reduces downtime.

Along with the use of the very latest integrated circuit technology, proven production techniques are used which have helped DEC successfully deliver over 9,000 computer systems.

APPLICATIONS

The Floating Point Processor, when used on a DEC 12-bit computer, provides capabilities normally found on larger word length and more expensive computers. These include the ability to directly address 32K of memory and to perform high precision arithmetic at high speed. The two processors together—the DEC 12-bit computer and the FPP-12—allow the programmer to have the advantages of either a 24-bit or 36-bit computer.

Signal Processing

Signal Processing tasks for DEC 12-bit computers include work in the biomedical research laboratory, analytical chemistry laboratory, the physics laboratory and the industrial research laboratory.

The FPP-12 provides the capability of performing sophisticated multi-task jobs with fast signals being handled by the compact processor. The initialization is simplified by requiring only two instructions to start service an interrupt, or restart the processor. The job status is automatically saved and restored using an active parameter table. Therefore, the signal processing unit can abort a current job and restart where it left off again. The old job can be resumed with minimum of programming overhead. This allows the system, for instance, to be doing on-line smoothing of fast signals and be interrupted in order to service another instrument. This small dual processor system can easily handle both functions. This effectively increases the sampling rate that can be handled.

The FPP's most important forte for the signal processing field is the speed and ease with which it handles the Floating-Point Format. The Floating-Point Format provides maximum accuracy for all calculations and real data. This format, added to the increase in program speed, allows complicated arithmetic to be done on real signals in real time without sacrificing either data rate or accuracy.

Education

The high speed capabilities of the FPP-12 allows the student more tries at a problem in what may be a limited period of time at a given computer installation. In the educational environment, the FPP has many advantages over using the small computer alone. It allows students to operate on and experiment with a multi-processor system for a minimum investment. Also, it allows the possibility of very sophisticated time sharing on small machines. This is accomplished by the FPP re-entrant type architecture. In addition, Fortran programming can be readily adapted to this compact dual-processor system. Direct addressing of all of core memory and moveable temporary storage areas allows many different types of jobs to be done simultaneously with the minimum amount of programming. The fact that the FPP can do index register arithmetic provides for the creation of push-down stacks and pop-up lists. This is extremely useful for evaluating complex equations and programming priority structures. Any core location can be an index register. This allows manipulation of large arrays with very simple programming.

FPP SOFTWARE

Assembler

Translates FPP-12 mnemonics into binary code. Includes literals and logical expressions. Operates in two passes, including program listing. Utilizes the DIAL system on a PDP-12 and operates the PS/8 system on a PDP-8 family computer.

AIPOS

Analytical Instrumentation Operating System—A real-time monitor system that handles the functions of job control, program loading, parameter interchange between programs, and interrupt handling. Provides routines to support the system real-time clock, CRT display, and standard I/O devices. Utilizes a special filing system for storing and retrieving programs and data. Requires 8K PDP-12.

DORA

Display-oriented math package. Displays multiple data files in conjunction with operator-controllable cursors that allow X-Y coordinate readout of the displayed waveforms. Simple user-oriented commands are available to perform integration, differentiation, scaling, baseline correction, peak stripping, X and Y axis offset, X axis calibration (linear and nonlinear), normalization, smoothing, addition and subtraction. DORA combines the processing power of the FPP-12 with the interactive display features of the PDP-12, and utilizes both LINCtapes and disks for data storage. Requires 8K PDP-12 with FPP-12.

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