EK-AN1/2-TM-001

AN10/AN20 ARPANET INTERFACE TECHNICAL MANUAL

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CHAPTER 1
INTRODUCTION

1.1 GENERAL DESCRIPTION

The AN10/AN20 Interface Option is a standard hardware interface option designed for users of the Advanced Research Projects Agency Network (ARPANET). The AN10 provides the means to integrate a DECsystem-10 packet switching system (T-series host) into the ARPANET by electrically and logically interfacing the KL10 external I/O bus (IBus), or KA10 or KI10 I/O bus, to the ARPANET Interface Message Processor (IMP). The AN20 differs from the AN10 in mechanical packaging. It also requires a DIB20 interface adapter to provide an electrical and logical interface to the internal EBus for purposes of integrating a DECSYSTEM-20 packet switching system (T-series host) to the ARPANET. See Figures 1-1, 1-2, and 1-3. The AN10 and AN20 each support either local (less than 9 meters [30 feet]) or distant (less than 610 meters [2000 feet]) connections to the IMP.

The AN10/AN20 is fully compatible with the 316, 316 TIP, 516, or Pluribus IMP buses without modification. It may be connected to only one T-series host CPU and one IMP at a time. The AN10/AN20 is made up of two functional device sections (input and output) which share a common I/O interface to the host. Each section is independently programmable for controlling message transfers.

The AN10/AN20 is specifically designed to use the KI10/KL10 vector and DATAO/DATAI interrupt capability (API functions 2, 4, and 5). KA10 I/O bus interrupt mode may, however, be selected by the program. It will handle I/O instruction executions in either "fast" bus or "slow" bus mode.

The AN10 logic circuitry is mounted in an H956 type cabinet 53 cm W × 76 cm D × 183 cm H (21 in W × 30 in D × 72 in H) equipped with the necessary power supplies and cooling fan assemblies. The AN20 logic circuitry is mounted in a type H9502 single high-boy cabinet frame 66 cm W × 76 cm D × 152 cm H (26 in W × 30 in D × 60 in H) equipped with the necessary power supplies and cooling fan assemblies. The required DECSYSTEM-20 EBus interface adapter (DIB20) is mounted within the CPU cabinetry.

1.2 OPERATION

The AN10/AN20 Interface Option is designed to handle full-duplex bit-serial message data streams at a minimum rate of 100,000 bits per second. The bit-serial data transmission protocol between the Host and IMP is supported by the AN10/AN20 with a program which selects either two-way or four-way handshake per bit.

Input is given priority over output; i.e., the IMP may cease handshaking data on AN10/AN20 output to favor message input to the Host thus freeing IMP buffer space. Four-way handshaking is recommended for all configurations except distant connections of several hundred meters.

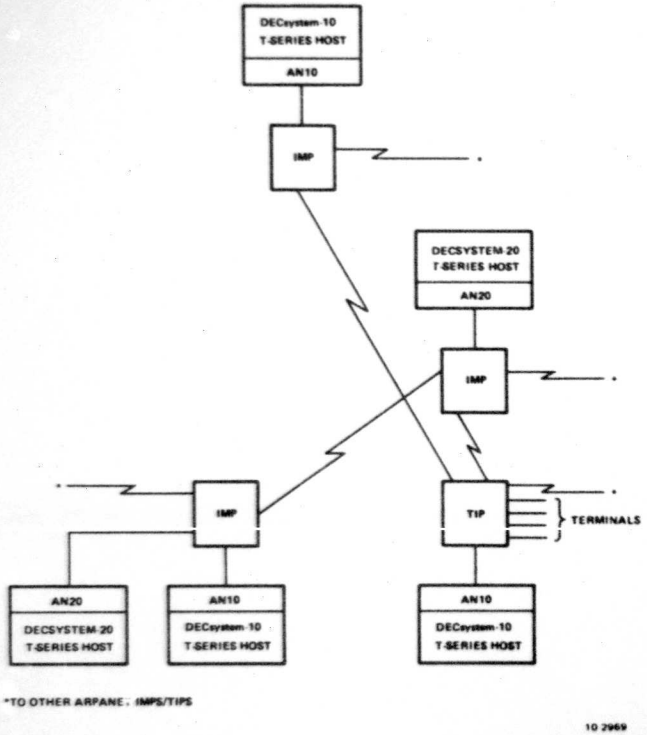


Figure 1-1 Typical Section of ARPANET

The AN10/AN20 supports two program selectable data modes: 32-bit mode and 36-bit mode. In 32-bit mode, message data is packed left-justified within the DECsystem-10/20 word. A message may be broken into multiple blocks of variable lengths. The data mode may be changed at any block boundary.

The AN10/AN20 supports two interrupt modes: KA10 style and KI10/KL10 vector style. A data-interrupt is generated for each word transfer. In addition, each AN10/AN20 transfer direction provides separate priority-interrupt channel assignments for status and data interrupts and these interrupts cannot occur simultaneously. In KI10/KL10 vector interrupt mode, status interrupts assert API function 2 (program vector interrupt), data out interrupts assert API function 4 (hardware executed DATAO), and data in interrupts assert API function 5 (hardware executed DATAI).

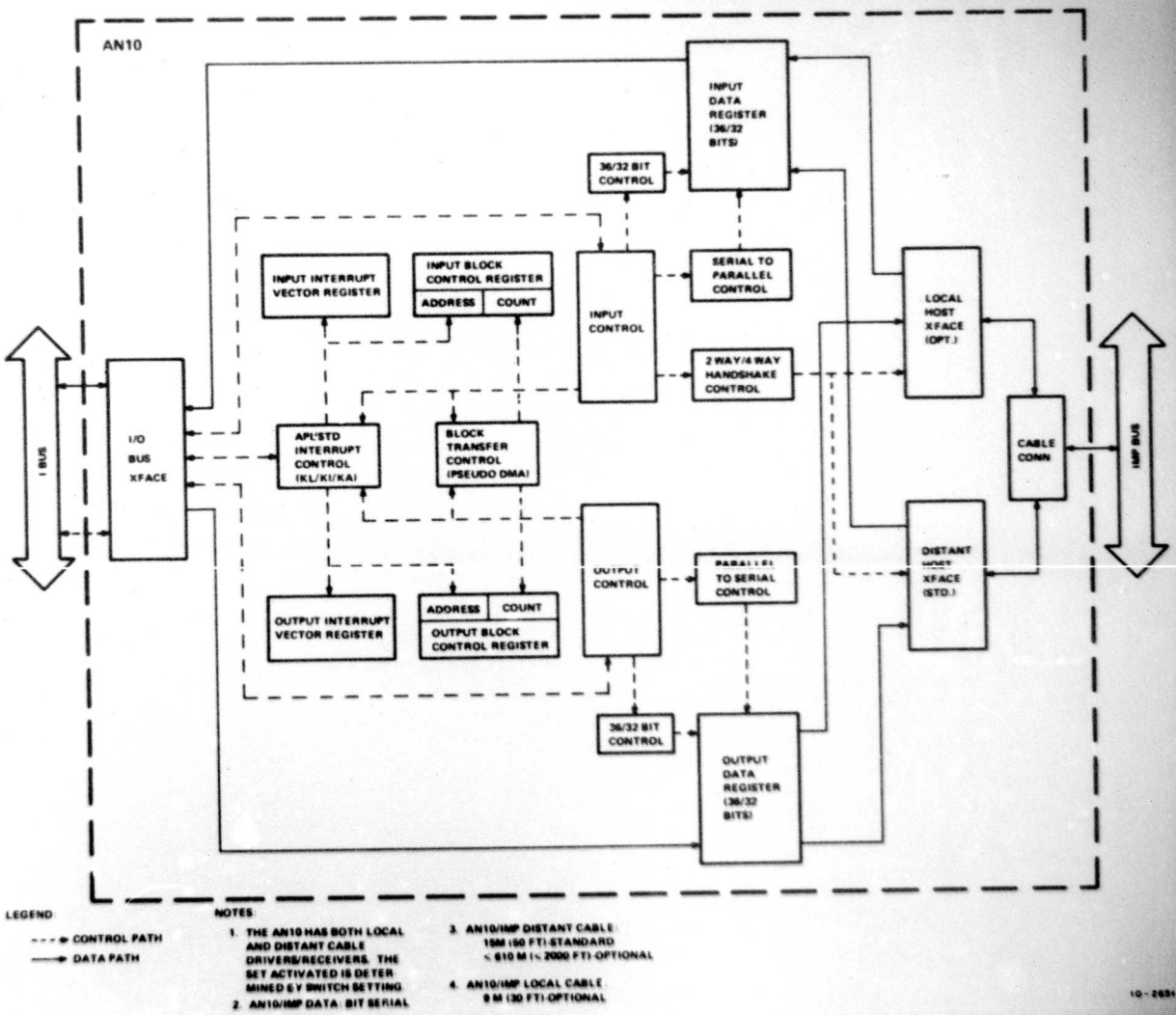


Figure 1-2 AN10 Interface Option Simplified Block Diagram

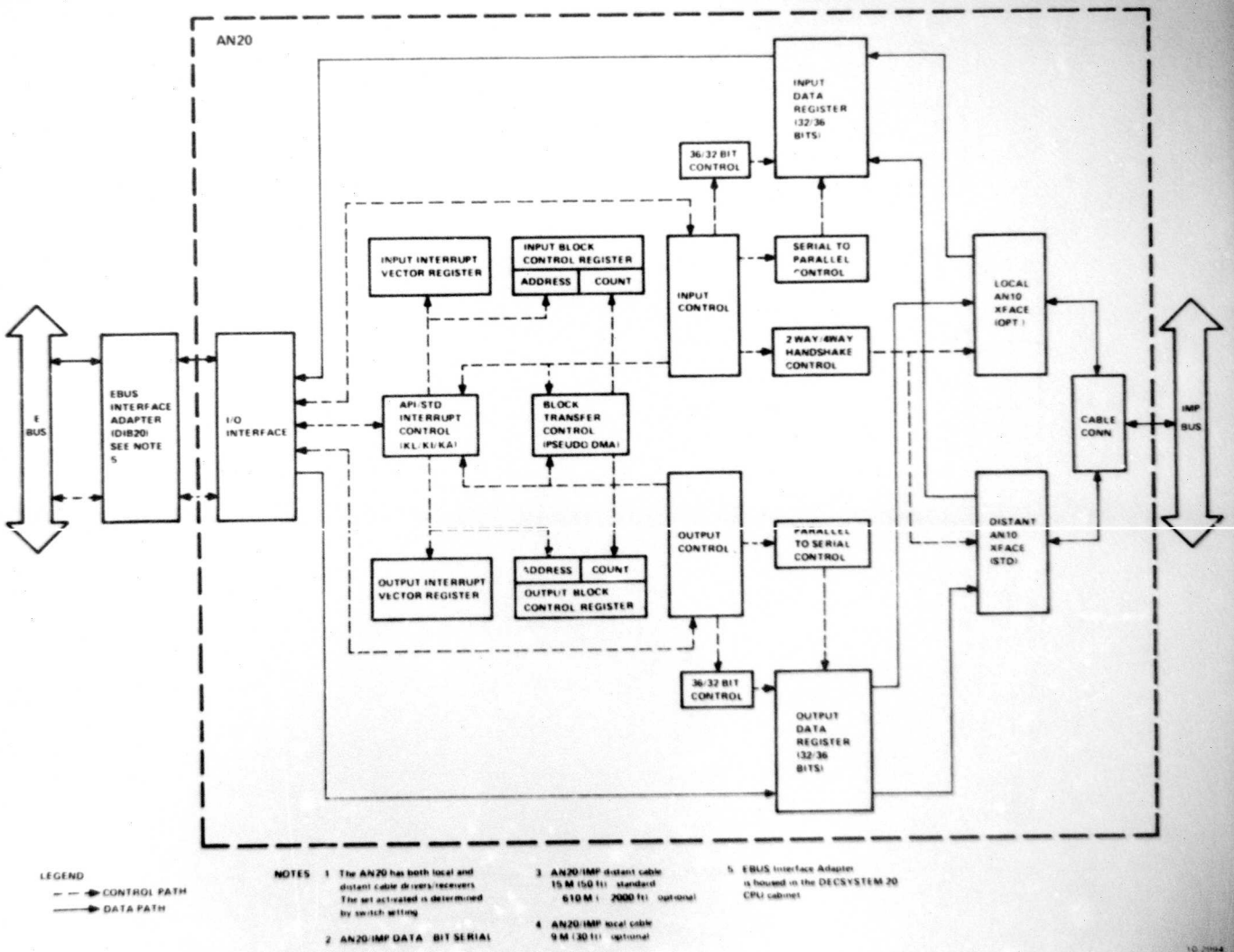


Figure 1-3 AN20 Interface Option Simplified Block Diagram

1.3 RELATED DOCUMENTATION

The following documents contain information that supplements the information in this document.

Title	Document Number
DECsystem-10/20 Hardware Reference Manual, Volume 1	EK-10/20-HR-001
DECsystem-10/20 Packet Switching System Site Preparation Guide	EK-PACSS-SP
DECsystem-10 Interface Manual	DEC-10-HIFC
Interface Message Processor, Specifications for the Interconnections of a Host and an IMP; Bolt Beranek and Newman, Inc.: Cambridge, MA	Report No. 1822, May 1978 Rev.

1.4 SPECIFICATIONS

AN10 and AN20 specifications are provided in Appendix A.

1.5 MODELS

AN10-AA/AN20-AA	KL10 to IMP Interface for ARPANET. Includes logical and electrical interface for either local or distant connection plus cable connector for terminating a 9 m (30 ft) local IMP cable (customer supplied); 120 Vac, 60 Hz service.
AN10-AB/AN20-AB	Same as AN10-AA/AN20-AA, except for 240 Vac, 50 Hz service.
AN10-BA/AN20-BA	AN10-AA/AN20-AA with the local cable connector replaced with a 15 m (50 ft) distant host cable assembly.
AN10-BB/AN20-BB	Same as AN10-BA/AN20-BA, except for 240 Vac, 50 Hz service.

CHAPTER 2
INSTALLATION AND CHECKOUT

2.1 SITE CONSIDERATIONS

All general requirements specified for the DECsystem-10 and the DECSYSTEM-20 in the DECsystem-10/20 Packet Switching System Site Preparation Guide are applicable to the AN10 and AN20.

The AN10/AN20 should be located so as to provide sufficient service clearance areas at the front and rear of the H956/H9502 Cabinet in which it is mounted. Figures 2-1 and 2-2 illustrate the suggested space clearance.

2.1.1 Local Connection to the IMP

When the AN10/AN20 is supporting a local connection to the IMP, the cable-run distance must be no more than 9 meters (30 feet) from the IMP.

2.1.2 Distant Connection to the IMP

When the AN10/AN20 is supporting a distant connection to the IMP, the cable-run distance must be no more than 610 meters (2000 feet) from the IMP; a 15 meter (50 foot) BC10T cable comes standard.

2.2 INSPECTION

Upon receipt of the AN10/AN20, inspect the exterior and interior of the equipment for any visible signs of damage from shipping. Verify that all logic modules are secure in the correct slots. Any damage observed should be reported immediately to both the carrier and the Branch Field Service manager. Check the contents of the shipment with the shipping list (A-PL-AN10-0-SL or A-PL-AN20-0-SL) and immediately report any omissions to the manufacturer. Installation is not recommended until all materials are present and the insurance company has had an opportunity to inspect the equipment in cases where damage claims are filed.

2.3 EQUIPMENT REQUIRED FOR INSTALLATION AND CHECKOUT

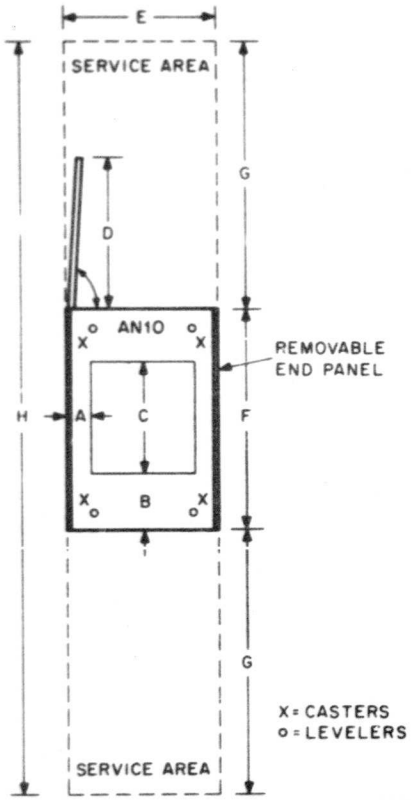
The following equipment is needed for proper installation of the AN10/AN20 Interface Option. The accessories included with the AN10/AN20 are listed in the shipping lists A-PL-AN10-0-SL and A-PL-AN20-0-SL.

Host Processor (DECsystem-10 or -20 with at least 64K words of memory)
BC10T IMP Cable or equivalent
Oscilloscope – Tektronix 454 or equivalent
DVM – Triplett Model 630 or equivalent
ARPA Interface Message Processor (IMP) with appropriate port
Diagnostics

MAINDEC-10-DDANA	ARPANET INTERFACE DIAGNOSTIC (EXEC MODE)
MAINDEC-10-DDANB	ARPANET USER MODE "IMPTST"
SUBRTN.A10	DIAGNOSTIC SUBROUTINE PACKAGE

AN10 (AN20) Print Set — MP00326 (MP00399)

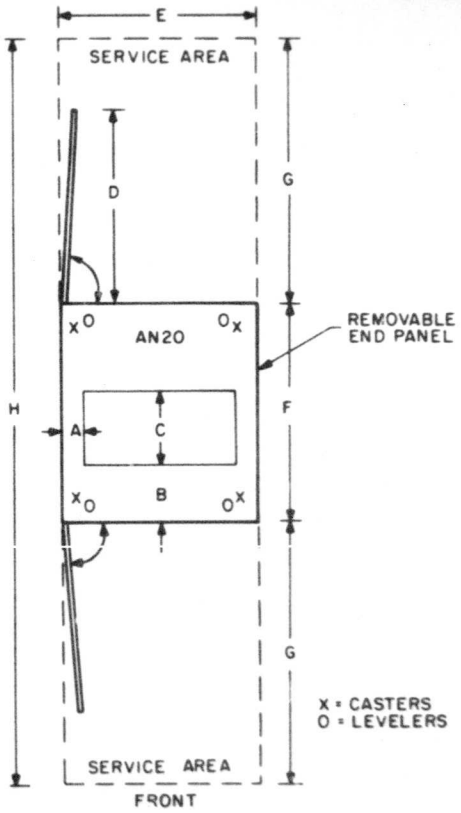
AN10/AN20 Technical Manual EK-AN1/2-TM



DIMENSIONS	A	B	C	D	E	F	G	H
METERS	0.08	0.19	0.38	0.5	0.52	0.76	0.91	2.58
INCHES	3.2	7.5	15	20	20.5	30	36	102

10-2500

Figure 2-1 AN10 Space Requirements



DIMENSIONS	A	B	C	D	E	F	G	H
METERS	0.08	0.20	0.25	0.69	0.69	0.76	0.91	2.59
INCHES	3	8	10	27	27	30	36	102

10-2992

Figure 2-2 AN20 Space Requirements

2.4 INSTALLATION AND CABLING

The AN10/AN20 Interface Option logic and associated H7420A Power Supply and 861-C/B Power Controller are mounted in an H956/H9502 Cabinet. To install the AN10/AN20 Interface Option, perform the following installation and cabling procedures.

1. If the interface is an AN10, remove the cabinet from the shipping skid and position it according to the applicable site installation floor plan.

   If the interface is an AN20, remove the cabinet caster shipping brackets and position the AN20 cabinet according to the applicable site installation floor plan. Then extend, adjust, and secure the rear cabinet stabilizer feet *before* opening the rear equipment mounting door.

CAUTION

Do not open the rear equipment mounting door without first extending and securing the stabilizer feet. Also, do not remove the machine screws serving as a doorstop. Failure to comply with the above will permit the cabinet to tip over risking serious injury to service personnel.

2. Set the H7420A Power Supply circuit breaker to OFF. Set the 861 Power Controller circuit breaker to OFF.

3. Ensure that logic modules are securely installed according to drawing D-MU-AN10-0-MU.

4. Connect the AN10/AN20 cabinet ground stud to the adjacent cabinet (if any) with a 90-08887 or equivalent ground braid or else to an appropriate earth ground by No. 4 AWG copper wire (7010789 or equivalent). Refer to E-UA-AN10-0-0 or E-UA-AN20-0-0.

5. For an AN20 installation, ensure that a DIB20 I/O bus adapter is installed in accordance with the DIB20 Installation Procedure, A-SP-DIB20-0-2.

6. If the unit being installed is an AN10, connect the BC10B margin check cable between the AN10's 70-05868 Margin Check Power Distribution Bar and the Margin Check Control Panel of the DECsystem-10. When the AN10 is the last device on the margin check bus, ensure that margin check terminating plug 70-05486 is also installed in the 70-5868 Margin Check Power Distribution Bar. Proper installation of the margin check bus is necessary because the bus supplies -15 V power for terminating the H867 I/O bus terminator. Also perform this step for an AN20 being installed on a DECSYSTEM-20 containing a DIB20 I/O bus adapter.

7. Connect the AN10/AN20 861 Power Controller to the power control bus in the DECsystem-10/20, with the 70-08288 Remote Turn-On Cable.

8. Ensure that the H867 I/O bus terminator is securely installed in Quick-Latch connector QL2 labeled I/O OUT (on rear of AN10 Wired Logic Mounting Assembly). Refer to drawing D-AD-7013480-0-0.

9. Install the I/O bus cable (BC10J or K) to the AN10/AN20 cable connector QL1 labeled I/O IN (on rear of AN10 Wired Logic Mounting Assembly) according to the applicable site installation floor plan. Refer to drawing D-AD-701384-0-0. Ensure that the BC10J or K cable is properly connected to the external I/O bus of the Host computer.

CAUTION

When an AN20 is installed, the cabinet must be carefully tipped a few degrees to allow insertion of the quick-latch connector of the cable under the cabinet and up through the bottom opening. Note that the rear equipment mounting door precludes routing the cable out the rear of the cabinet. The cabinet drip screen must then be secured. For the AN20, the drip screen (PN 7415394) and its supports (PN 7415268) are shipped loose. Install them as illustrated in the unit assembly print E-UA-AN20-0-0.

10. Install the AN10/AN20 IMP cable connector into the mating ZIF connector labeled IMP IN (on rear of AN10/AN20 Wired Logic Assembly). See Figure 2-3. This cable is a BC10T-XX for an AN10-B/AN20-B and is customer supplied for an AN10-A/AN20-A. In the latter case, the DIGITAL supplied ZIF connector may need to be installed on the customer supplied cable. This assembly is illustrated in prints E-UA-AN10-0-0 or E-UA-AN20-0-0, and D-BS-AN10-0-LCC. Install the IMP end of the AN10/AN20 IMP cable at the IMP interface according to the appropriate site installation plan supplied with the IMP.

11. Verify that a BC06R-4 flat 40-conductor cable is connected into the leftmost (facing front of AN10/AN20 cabinet) IMP IN connector. See Figure 2-3. The other end of this cable feeds through the wired assembly cable service opening and installs into connector J1 (top connector) on the M8612 module in slots AF13. See print E-UA-AN10-0-0 or E-UA-AN20-0-0.

12. Verify that a BC06R-4 flat 40-conductor cable is connected into the rightmost (facing front of AN10/AN20 cabinet) IMP IN connector. The other end of this cable feeds through the wired assembly cable service opening and installs into connector J2 (bottom connector) on the M8612 module in slots AF13. See print E-UA-AN10-0-0 or E-UA-AN20-0-0.

13. Verify that a BC06R-1 40-conductor flat cable is connected from the rightmost IMP LOOP connector (facing front of AN10/AN20 cabinet) to the leftmost IMP LOOP connector. The cable loop should be dressed through the wired logic assembly cable service opening. Refer to Figure 2-3 and print E-UA-AN10-0-0 or E-UA-AN20-0-0.

14. Install the AN10/AN20 Loop Back Test connector assembly 70-13963 on the mating ZIF connector labeled "IMP LOOP" (on back of AN10 Wired Logic Mounting Assembly). See Figure 2-3.

15. Verify that no shorts between +5 V, -5V, -15 V, and ground exist on the backplane assembly.

16. Connect the 861 Power Controller input power cable to the appropriate ac facility power. Refer to EK-PACSS-SP and to Appendix A for details.

17. Set the 861 Power Controller REMOTE ON/OFF/LOCAL ON toggle switch to REMOTE ON. Set the circuit breaker to ON.

18. Set the H7420A Power Supply circuit breaker to ON.

19. Power up the DECsystem host and check the AN10/AN20 for proper fan rotation and for absence of smoke.

D3

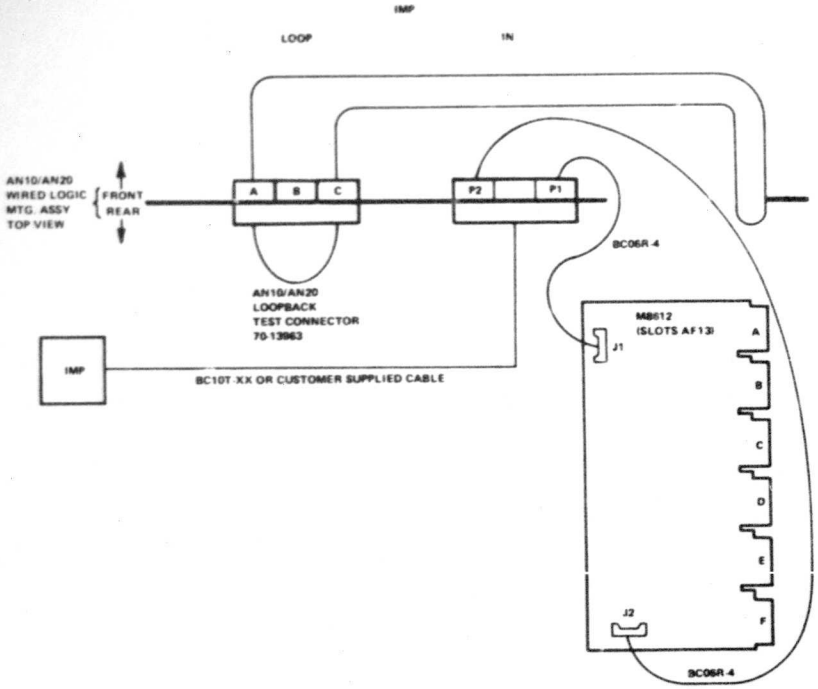


Figure 2-3 AN10/AN20 Partial Cabling Diagram

10 2970

20. Adjust the H744, H745, and H754 power supply regulators for their respective voltage ±0.1 V, measured at the backplane.

21. Verify that -15 V power is properly applied to the I/O bus terminator at pin 30T2 of the quick-latch connector QL2 labeled I/O OUT. Refer to print D-AD-7013480-0-0, sheet 5 of 5, for the positioning of this pin.

22. With the AN10/AN20 powered up, verify that the G891 power fail-crobar has properly released. That is, A15M2 should no longer be at ground potential and A15V2 should be at +3 V.

2.5 LOCAL/DISTANT CONNECTION SWITCH SETTING

Set switch E15-1 on the M8612 module to correspond to the type IMP-interface connection available; i.e., ON for a distant interface connection and OFF for a local interface connection. Refer to D-CS-M8612-0-A21 drawing. The AN10/AN20 is factory shipped with switch E15-1 OFF for an AN10-A/AN20-A and ON for an AN10-B/AN20-B.

2.6 DEVICE CODE SWITCH SETTINGS

Set switches E15-3 through E15-8 on the M8612 module to correspond to the six most significant bits of the IOS device code; i.e., 101 010($52X_8$). Refer to D-CS-M8612-0-P1 drawing. The AN10/AN20 is factory shipped with device codes 520_8 and 524_8 selected.

NOTE

Switches E15-3 through E15-8 are set to ON for a binary ONE and OFF for a binary ZERO.

2.7 ACCEPTANCE TEST PROCEDURES

Perform the procedures specified in print A-SP-AN10-0-AP to check out and accept the AN10/AN20 Interface Option. The procedures specified are summarized below for convenience.

2.7.1 AN10 Acceptance Test

1. If the AN10 is to be configured for a distant IMP interface, position switch E15-1 on the M8612 module OFF to enable the local cable drivers and receivers. Otherwise, switch B15-1 ON to enable the distant receivers and drivers.

2. Load MD-10-DDANA, consulting the listing for switch settings and operating instructions.

3. Start execution of MD-10-DDANA. Type a carriage return (CR) to the TTY prompt message to specify execution of all basic tests. In response to the TTY prompt regarding the type of loopback to be tested, type I to specify internal loopback. Execute 10 minutes, no errors allowed. Typical TTY typeout follows:

```
DIAMON CMD - DDANA
DDANA.A10 VER 0.1 15-MAR-77

DDANA - AN10/AN20 ARPA NETWORK INTERFACE DIAGNOSTIC LOADED.
VERSION 0.1, SV=0.12, CPU#G592, 60 HZ

SWITCHES = 000000 000000
DDANA: OPTIONS (ANY OF H,L,<CR>,T,C,I)=><CR>

LOOPBACK;)TYPE I FOR INTERNAL, E FOR EXTERNAL): I
```

4. Disconnect the AN10 to IMP cable (BC10T or equivalent) from the AN10 logic assembly ZIF connector labeled IMP IN. Move the AN10/AN20 loopback test connector 70-13963 from the ZIF connector labeled IMP LOOP to the IMP IN position. Repeat step 3 except type E to the appropriate TTY prompt to select external loopback. Typical TTY typeout follows:

```
DIAMON CMD - DDANA
DDANA.A10 VER 0.1 15-MAR-77

DDANA - AN10/AN20 ARPA NETWORK INTERFACE DIAGNOSTIC LOADED.
VERSION 0.1, SV=0.12, CPU#G592, 60 HZ

SWITCHES = 000000 000000
DDANA: OPTIONS (ANY OF H,L,<CR>,T,C,I)=><CR>

LOOPBACK;)TYPE I FOR INTERNAL, E FOR EXTERNAL): E
```


E3

5. If the IMP interface is configured for a local connection, plug the AN10 end of the local cable into the ZIF connector labeled IMP LOOP. Call the Network Control Center and arrange with them to run a cable continuity test from the IMP. This test is optional unless cable continuity problems are suspected.

6. If the AN10 is to be configured for a distant IMP interface, position switch E15-1 on the M8612 module ON to enable the distant cable drivers and receivers. Otherwise, switch E15-1 OFF to enable the local receivers and drivers.

7. Repeat step 3, typing I to the appropriate TTY prompt to select internal loopback.

8. Repeat step 3, typing E to the loopback TTY prompt to select external loopback.

9. Restore the AN10/AN20 loopback test connector 70-13963 to its storage position on the ZIF connector labeled IMP LOOP. Connect the AN10 end of the BC10T or equivalent cable to its operational position on the ZIF connector labeled IMP IN.

10. If the unit under test is an AN10-B (supplied with a BC10T distant Cable), disconnect the BC10T from the IMP and attach the BC10T cable loopback test connector 70-13995 to the BC10T cable. Repeat step 3, typing E to the loopback TTY prompt to select external loopback. After successful completion of this test, disconnect the 70-13995 test connector from the BC10T cable and reattach the BC10T cable in its normal operating position within the IMP.

11. Start execution of MD-10-DDANA. Type I to the first TTY prompt to select the IMPTST (or reliabillity) portion of the diagnostic. Type ESC (escape or altmode) to the parameter select prompt to specify all pattern combinations and random message lengths. Execute this test for 1 hour. No data or length mismatches are acceptable. Other typeouts relate to the performance of the network at the time and are not necessarily errors. Consult the listing for operational procedures. Note that while IMPTST is running, the AN10/AN20 is on the ARPANET. This means that other connections may send messages to this AN10. These messages will be printed on the TTY log and are not errors. A typical acceptable TTY typeout follows:

```
SWITCHES = 000000 000000

DDANA* OPTIONS (ANY OF H,L,<CR>,T,C,I)=> I
IMPTST: OPTIONS(ANY OF L,T,P,S,<ESC>,?) <ESC>
RUNNING...
OLD FORMAT, TYPE: 4 MSG.
TYPE: 12, MSG-ID: 0, BITS: 0, FROM HOST 0 ON IMP 0
TYPE: 1, MSG-ID: 0, BITS: 0, FROM HOST 2 ON IMP 0
TYPE: 0, MSG-ID: 0, BITS: 72, FROM HOST 1 ON IMP 52
TYPE: 0, MSG-ID: 0, BITS: 76, FROM HOST 3 ON IMP 52

MESSAGES SENT: 500
MESSAGES RECEIVED: 500
RFNM's RECEIVED: 500
DATA MISMATCHES: 0
LENGTH MISMATCHES: 0
MESSAGE TIMEOUTS: 0
RFNM TIMEOUTS: 0
```



```
TYPE: 0, MSG-ID: 0, BITS: 72, FROM HOST 3 ON IMP 5
TYPE: 0, MSG-ID: 0, BITS: 76, FROM HOST 2 ON IMP 22

MESSAGES SENT: 1000
MESSAGES RECEIVED: 1000
RFNM's RECEIVED: 1000
DATA MISMATCHES: 0
LENGTH MISMATCHES: 0
MESSAGE TIMEOUTS: 0
RFNM TIMEOUTS: 0
```

12. Bring up the TOPS20-AN Operating System on the system under test. Load MD-10-DDANB, consulting the listing for switch settings and operating instructions. Execute for one hour with no data mismatches or length errors. Other typeouts relate to the performance of the network and are not necessarily errors. The note for step 11 also applies in this test. This test is for customer acceptance only and is not performed as part of factory acceptance. This test is not valid on systems not supporting TOPS20-AN release 3.0 or higher. A typical acceptable TTY typeout follows.

NOTE

Successful running of MD-10-DDANB requires:

- **DIAMON.SAV DIAGNOSTIC MONITOR**
- **SUBRTN.A10 NON-RESIDENT SUBROUTINE PACKAGE**
- **ARPANET-WIZARD PRIVILEGES**

```
DIAMON CMD - DDANB
DDANB.A10 VER 100.1     18-JUL-77

DDANB:IMPTST-USER MODE LOADED.
VERSION 100.1, SV=0.13

TTY SWITCH CONTROL ? - 0,S,Y, OR N <CR> - 0

SWITCHES = 000000 000000
STARTING...
IMPTST>START
MESSAGES SENT: 500
MESSAGES RECEIVED: 476
RFNM's RECEIVED: 476
MESSAGE TIMEOUTS: 17
RFNM TIMEOUTS: 16
LATE MESSAGES: 0
LATE RFNMS: 0
IGNORED MESSAGES: 0
DATA MISMATCHES: 0
LENGTH ERRORS: 0
IMPTST>STOP
IMPTST>↑C
```


F3

For a list of the available operating commands recognized by DDANB, type "?" in response to the "IMPTST>" prompt. An example follows. These commands may be given after the program is running.

IMPTST>? one of the following:

DAYTIME	DDT	EXIT	HELP
PRINT	REINITIALIZE	SET	START
STOP	TAKE		

13. Successful completion of the above tests constitutes acceptance of the AN10 ARPANET Interface Option.

2.7.2 AN20 Acceptance Test

1. Repeat steps 1 through 13 of the AN10 acceptance test procedure (Paragraph 2.7.1), replacing AN10 with AN20.

2. Completion of step 1 above constitutes acceptance of the DIB20 EBus interface adapter, if not previously installed and accepted.

CHAPTER 3
OPERATION AND PROGRAMMING

3.1 GENERAL OVERVIEW

The AN10/AN20 is a freestanding interface-option for interfacing the external IBus of a T-series DECsystem-10/20 host to the ARPANET IMP. It is manually selectable via a switch on the M8612 I/O Control Board for the following operations.

- Local interface connection for interfacing to the IMP over a single-endedly driven cable up to 9 m (30 ft) long.

- Distant interface connection for interfacing to the IMP over a balanced, differentially driven cable of up to 610 m (2000 ft). The standard cable length is 15 m (50 ft).

The AN10/AN20 minimizes host CPU overhead by making extensive use of the advanced KL10/KI10 API interrupt functions. Data is moved to/from the AN10/AN20 addressed host memory buffer by the DATAI/DATAO API function; in this manner a cycle is "stolen" from the host CPU to move a 32- or 36-bit data word without software intervention. A vectored software interrupt is generated only when the complete message is transferred. This API interrupt mode has the capability, however, to be deselected by the program to support the conventional, higher overhead, KA10 I/O bus interrupt structure.

The AN10/AN20 maintains separate data and control registers for each direction to facilitate full-duplex data transfers. It provides several programmable maintenance functions for diagnosing failures. These functions provide three different modes of internal control and data signal loopback as well as a mechanism for single stepping the handshake control signals to/from the IMP. Alternatively, data may be looped back externally with installation of a cable loopback connector.

The AN10/AN20 features programmable selection of either 2-way or 4-way handshaking of the control signals transporting bit serial data between the AN10/AN20 and the IMP.

3.2 OPERATION

3.2.1 Data Modes

Two program selectable data modes are supported: 32-bit mode and 36-bit mode. In 32-bit mode, message data is packed left-justified within the DECsystem-10/20 word with the remaining bits zero filled as illustrated in Sections 3.4.1.2 and 3.4.1.6. The data format may be changed whenever the word count register for the desired direction decrements to zero.

3.2.2 Interrupt Modes

Two programmable interrupt modes are supported by the AN10/AN20 hardware: KA10 style and KI10/KL10 vector style. In addition, each transfer direction provides separate priority interrupt channel assignments for status and data interrupts. The hardware architecture is such that for a given transfer direction, a data and a status interrupt cannot occur simultaneously: a data interrupt is serviced before a status interrupt of the same level, and an input interrupt has priority over an output interrupt of the same type. A data interrupt is generated for each word transferred.

3.2.2.1 KA10 Interrupt Mode – When the CPU grants an interrupt request, the AN10/AN20 transfers an API function word type 1 to the host CPU in response to the function word transfer signals on the I/O bus. This occurs when the AN10/AN20 is programmed for KA10 interrupt mode and when it is connected to the I/O bus of the KI10 or to the IBus output of a DIA20 or DIB20 KL10 I/O bus Adapter. The API function word type 1 specifies that the interrupt is to be KA10 style; i.e., to location 40 + 2n. The device interrupt service routine must then determine the cause of the interrupt and issue to the AN10/AN20 the appropriate I/O command to clear the interrupt condition. A DATAO/DATAI is required to clear a data interrupt request and a CONO is required to clear a status interrupt request.

CAUTION

Once the API function word is transferred, the AN10/AN20 removes its interrupt request from the I/O bus. The interrupt status flag is not cleared, however, until the appropriate I/O instruction is executed. Hence, no more interrupts of that type will be issued to the CPU until the state initiating the interrupt request is cleared by the desired I/O command response.

The AN10/AN20 has a separate, programmable word count register for each transfer direction. Once a transmission is initiated, a data-interrupt per word continues until the word count for that direction expires.

The I/O bus structure of the KA10 does not support API function words. Hence, when the AN10/AN20 is connected to the I/O bus of the KA10, no I/O bus API function word transfer control signals will be asserted to the AN10/AN20. Therefore, no API function word will be generated and the AN10/AN20 will, by default, be compatible with the KA10 mode of interrupt handling. In this case, both the I/O bus interrupt request flip-flops and the interrupt status flip-flops will remain asserted until cleared by execution of the appropriate I/O instruction. This difference, however, is not distinguishable from a user standpoint.

3.2.2.2 KI/KL Interrupt Mode – Two variations of KI/KL Interrupt mode are defined in the AN10/AN20.

- KL10 Interrupt mode
- KI10 Interrupt mode

KL10 Interrupt mode is the default state for the AN10/AN20. When programmed for KI/KL interrupt mode the AN10/AN20 handles status and data interrupts differently.

For status interrupts, the AN10/AN20 generates an API function word type 2 (vectored) interrupt to the address pointed to by the contents of the selected vector address register. A separate vector address register is maintained for each transfer direction.

For data interrupts the AN10/AN20 generates an API function word type 4 (or 5) interrupt to specify hardware execution of a DATAO from (or DATAI to) the memory location specified by the contents of the address portion of the selected word count/address register. Hardware execution of this DATAO (DATAI) clears the interrupt request flag, decrements the word count, and increments the data address. The AN10/AN20 has a separate word count/address register for each transfer direction. Data interrupts continue until the word count for that direction is zero. Using this mechanism, which steals CPU cycles to move data to/from memory, a pseudo DMA transfer capability is implemented to reduce software overhead.

The difference between KI10 interrupt mode and KL10 interrupt mode is that in KI10 interrupt mode vector and data word address pointers for automatic priority interrupts are restricted to 18 bits, whereas the pointers are 23 bits long for KL10 interrupt mode. Additionally, for the KL10 interrupt mode, a qualifier bit in the API function word allows programmable specification of whether or not protection and relocation should be applied to the pointer addresses.

API function word bits 0–2 are not asserted by the AN10/AN20. These bits correspond to the address space in the KL10 API format. The DIA20 and DIB20 unconditionally assert bit 02 to specify EXEC VIRTUAL addressing.

3.3 INTERFACING

The AN20 utilizes the AN10 logic assembly, module set, and cables. For simplicity and to avoid redundancy in documentation, the AN20 lists components of the AN10 with its attendant documentation as a subassembly. Therefore, in the following sections where this manual refers to a signal or bit definition documented in the AN10 print set, and which includes AN10 as part of the documented name, AN20 will not be substituted for AN10. Rather, the correctly documented name will be utilized. The reader must keep this in mind when reading this manual for an understanding of the AN20 interface option and mentally associate that signal or name with the AN20.

3.3.1 IMP Cable Interface and Indicator Panel (See Figure 3-1.)

The 12 signals composing the interconnecting cable between the AN10/AN20 Interface Option and the IMP are summarized below. The signal name, the mnemonic, and the functional description, in summary, are given for each of the 12 signals. I2A is the prefix given for signals from the IMP to the AN10/AN20. Conversely, A2I is the prefix for signals from the AN10/AN20 to the IMP.

1. **IMP MASTER READY (IMP RDY)** signal (I2A IMP MASTER RDY) – The return for the IMP READY TEST signal through the IMP's relay contact. (See 5, Figure 3-1.)

2. **IMP READY TEST** signal (I2A IMP RDY TEST) – The test signal sent to the IMP to interrogate its ready status through the IMP's relay contacts.

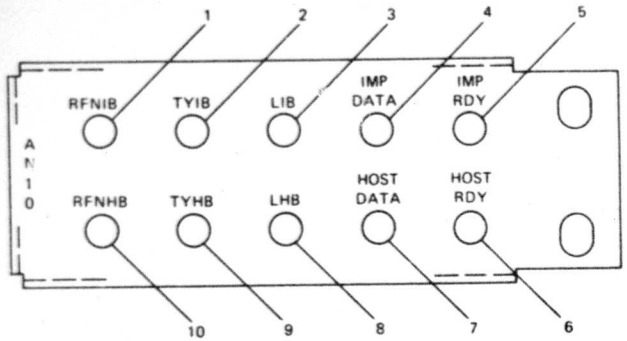
3. **AN10* MASTER READY (HOST RDY)** signal (A2I AN10 MASTER RDY) – The return for the AN10 READY TEST signal (refer to 4, below) through the AN10's/AN20's relay contacts. (See 6, Figure 3-1.)

4. **AN10 READY TEST** signal (A2I AN10 RDY TEST) – The ground signal sent to the AN10/AN20 to interrogate its ready status through the AN10's/AN20's relay contacts.

5. **AN10* TO IMP DATA (HOST DATA)** signal (A2I AN10 TO IMP DATA) – This signal carries the data bit for transmission from the AN10/AN20 to the IMP. A 350 ns deskew delay plus approximately 235 ns additional logic delay provides approximately 585 ns deskew between assertion of the AN10 TO IMP DATA signal and the YOUR AN10 BIT handshake control signal. Data from the AN10/AN20 is changed for successive bits only after the IMP's READY FOR AN10 BIT signal (refer to 7, below) goes off. (See 7, Figure 3-1.)

6. **YOUR AN10* BIT (TYHB)** signal (A2I YOUR AN10 BIT) – This signal is presented to the IMP by the AN10/AN20 when it has a bit available to transmit, a 350 ns data-deskew delay has elapsed, and the IMP has asserted the READY FOR AN10 BIT signal (refer to 7, below). When the READY FOR AN10 BIT signal turns off, the YOUR AN10 BIT signal is removed, following a minimum assertion of 500 ns for a local connection and 1.1 μs for a distant connection. (See 9, Figure 3-1.)

*AN10 is the host.



REF NO	NAME	MEANING	REFERENCE
1	RFNIB	READY FOR NEXT IMP BIT	SECTION 3.3.1, SIGNAL 11
2	TYIB	THERE'S YOUR IMP BIT	SECTION 3.3.1, SIGNAL 10
3	LIB	LAST IMP BIT	SECTION 3.3.1, SIGNAL 12
4	IMP DATA	IMP DATA	SECTION 3.3.1, SIGNAL 9
5	IMP RDY	IMP READY	SECTION 3.3.1, SIGNAL 1
6	HOST RDY	HOST* READY	SECTION 3.3.1, SIGNAL 3
7	HOST DATA	HOST* DATA	SECTION 3.3.1, SIGNAL 5
8	LHB	LAST HOST* BIT	SECTION 3.3.1, SIGNAL 8
9	TYHB	THERE'S YOUR HOST* BIT	SECTION 3.3.1, SIGNAL 6
10	RFNHB	READY FOR NEXT HOST* BIT	SECTION 3.3.1, SIGNAL 7

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Figure 3-1 Interface Indicator Panel

7. READY FOR AN10* BIT (RFNHB) signal (I2A RDY FOR AN10 BIT) - This signal is presented to the AN10/AN20 whenever the IMP is ready for transmission of a bit from the AN10/AN20. Each time the AN10/AN20 gives the IMP a bit (via YOUR AN10 BIT signal), the READY FOR AN10 BIT signal will go off after the bit has been taken in. It will go back on again when the IMP is ready for another bit. (See 10, Figure 3-1.)

8. LAST AN10* BIT (LHB) signal (A2I LAST AN10 BIT) - When the AN10/AN20 transmits the last bit of a message, the LAST AN10 BIT signal is sent to the IMP in conjunction with the YOUR AN10 BIT signal. A 350 ns deskew delay pulse plus approximately 65 ns additional circuit delay provides about 415 ns deskew from the assertion of the LAST AN10 BIT signal to assertion of the YOUR AN10 BIT signal. The IMP will pad the message with a one followed by enough zeros (perhaps none) to fill the current IMP word. (See 8, Figure 3-1.)

*AN10 is the host.

9. IMP TO AN10 DATA (IMP DATA) signal (I2A IMP TO AN10 DATA) - This signal carries the data bit for transmission from the IMP to the AN10/AN20. A 50 ns deskew delay for the YOUR IMP BIT signal plus approximately 55 ns additional circuit delay provides about 105 ns deskew of data received from the IMP. Data for the AN10/AN20 is changed for successive bits only after the READY FOR IMP BIT signal (refer to 11, below) goes off. (See 4, Figure 3-1.)

10. YOUR IMP BIT (TYIB) signal (I2A YOUR IMP BIT) - This signal is presented to the AN10/AN20 by the IMP as soon as the IMP has a bit available to transmit and the AN10/AN20 presents the READY FOR IMP BIT signal (refer to 11, below). When the READY FOR IMP BIT signal goes off, the YOUR IMP BIT signal will be removed. It will not be renewed until the READY FOR IMP BIT signal is again asserted. (See 2, Figure 3-1.)

11. READY FOR IMP BIT (RFNIB) signal (A2I RDY FOR IMP BIT) - This signal is presented to the IMP whenever the AN10/AN20 is ready to receive information. Each time that the IMP gives the AN10/AN20 a bit (via the YOUR IMP BIT signal), the READY FOR IMP BIT signal goes off after the bit has been taken in. This notifies the IMP that the bit has been taken and that a new bit can be moved into position and made available. The READY FOR IMP BIT signal is off for at least 100 ns (1.1 μs for a distant connection) as seen at the IMP before it goes back on again. It may, of course, be off for as long as it takes the AN10/AN20 to ready itself to receive the next bit. (See 1, Figure 3-1.)

12. LAST IMP BIT (LIB) signal (I2A LAST IMP BIT) - When the IMP transmits the last bit of the source IMP's message or padding, the LAST IMP BIT signal is sent to the AN10/AN20 in conjunction with the YOUR IMP BIT signal. Specifically, the LAST IMP BIT signal comes on no later than the YOUR IMP BIT signal. The AN10/AN20 provides approximately 105 ns additional deskew. The AN10/AN20 will round out (pad) the last message word with zeros, as required. (See 3, Figure 3-1.)

3.3.2 Master Ready Line Usage

The AN10/AN20 Interface gates all incoming signals from the IMP with the IMP MASTER READY signal. Status bits within the AN10/AN20 provide the user with information regarding the current polarity of the IMP MASTER READY signal as well as whether or not the signal changed during a message transfer. Before a message is started (in either direction), the user should check to see that the IMP MASTER READY line is asserted (ICSR CONI bit 19=0) and that IMP WAS DOWN is not asserted (ICSR CONI bit 18=0). If the latter bit is set, it should be cleared. The message transfer should then be initiated.

If IMP MASTER READY is lost during a message transfer, the AN10/AN20 will wait until it is again asserted before continuing data transmission to/from the IMP. However, loss of IMP MASTER READY does not cause an AN10/AN20 interrupt. This means that a message transfer, once started, will eventually continue to completion. Therefore, at the conclusion of a transmission, the IMP NOT READY status bits discussed above must be examined to ensure correct transmission of the message. If either ICSR CONI bit 18 or 19 is set, error recovery and IMP resynchronization procedures must be invoked.

The reader should note that the IMP interface will change the signal on the IMP MASTER READY line whenever the IMP (1) detects an error during a message transmission, or (2) several seconds of inactivity elapse with no message transferred between the AN10/AN20 and IMP.

3.3.3 Signaling Protocol

The AN10/AN20 program can select either two-way or four-way handshaking of the asynchronous demand/response signals used to transport data across the interconnecting cable from the IMP. The

mode of handshaking is a function of the receiving device and is, therefore, selectable by the AN10/AN20 for input only. Four-way handshaking is recommended for all configurations except distant connections of several hundred meters, and is therefore the default mode of signal handshaking.

Four-way handshaking (Figure 3-2) requires four cable transactions of the READY FOR BIT/YOUR BIT control signals per data bit transfer.

Two-way handshaking (Figure 3-3) monitors only two cable transitions of the READY FOR BIT/YOUR BIT control signals. For a local connection, READY FOR BIT must be unasserted for at least 100 ns before being asserted again; for a distant connection, it must be unasserted for at least 1.1 μs.

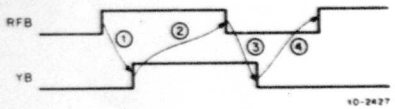

Figure 3-2 Four-Way Handshake

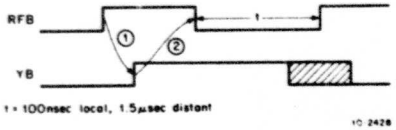

Figure 3-3 Two-Way Handshake

Except for time delays necessary to preserve the signaling protocol specification, the AN10/AN20 operates at the signaling speeds determined by the IMP up to a maximum limit of 850K bits/second. Speeds above 100K bits/second, however, are not supported by T-series host systems.

3.3.4 I/O Bus Interface

The AN10/AN20 Interface Option interfaces to the DECsystem-10 external I/O bus. For a KL10 based host, a DIA20 or DIB20 EBus to IBus adapter is required. The AN10/AN20 IBus interface is common to both the input and output device sections of the AN10/AN20 and uses DIGITAL's standard M-series I/O bus receivers and drivers.

3.3.5 IOB Reset

I/O Bus Reset initializes the entire AN10/AN20 logic.

3.3.6 Device Codes

Two device codes are customarily assigned to the AN10/AN20. Device select code 520_8 is assigned to the input device and 524_8 is assigned to the output device. The logic design requires that the input device be $XY0_8$ and the output device be $XY4_8$. The device code assignment is controlled by switches on the M8612 I/O bus control module.

3.3.7 Signal Deskew

The AN10/AN20 Interface Option deskews the data signal for IMP to Host data transmission by approximately 100 ns; data for Host to IMP transmission is deskewed approximately 500 ns.

3.4 PROGRAMMING

In the following programming section, the names AN10 and AN20 will be referenced together where the interface is referred to by name and where the text applies to both the AN10 and AN20. However, since the AN20 uses AN10 components, references to signal names and logic states documented under an AN10 assembly, and which incorporate the name AN10, will not have the name AN20 optionally substituted in the text so that the reference will be exactly as found in the print set and attendant documentation. The AN20 reader should, nevertheless, note that the text applies to the AN20 as well. See also Paragraph 3.3.

3.4.1 Programmable Registers

Each device section (input and output) of the AN10/AN20 has four major registers: control/status, data, word count/address, and vector. All but the control/status register are loaded by DATAO and read by DATAI. The register referenced is controlled by register select bits in the control/status register.

3.4.1.1 Output Control/Status Register (OCSR) – Each bit position of the Output Control/Status Register (OCSR) is defined in Table 3-1 and illustrated in Figure 3-4.

Table 3-1 Output Control/Status Register (OCSR) Bit Definitions

I/O	Bit	Definition
CONI	00	READY FOR AN10 BIT signal. The READY FOR AN10 BIT signal is the received 12A RDY FOR AN10 BIT signal on the AN10/AN20-IMP cable during normal operation and is internally simulated as an AN10/AN20-IMP signal in diagnostic loop modes. The READY FOR AN10 BIT signal is the output of a multiplexer which selects one of several source signals as defined in Table 3-2 (the multiplexer is enabled by 12A IMP READY). This signal is described in Section 3.3.1.
CONI	01	YOUR AN10 BIT signal. The OCON YOUR AN10 BIT flip-flop is the source of the A2I YOUR AN10 BIT signal on the AN10/AN20-IMP cable during normal operations and is internally simulated as an AN10/AN20-IMP signal during diagnostic loop modes. This signal is described in Section 3.3.1.
CONI	02	AN10 TO IMP DATA signal. The OCON AN10 TO IMP DATA flip-flop is the source for the A2I AN10 TO IMP DATA signal on the AN10/AN20-IMP cable during normal operation and is internally simulated as an AN10/AN20-IMP signal during diagnostic loop modes. This flip-flop holds the data bit shifted out of the Output Data Register (ODR) for transmitting to the IMP. This buffering permits fetching the next data word concurrent with transmission of the last bit of the current word. The AN10 TO IMP DATA signal is described in Section 3.3.1.

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Table 3-1 Output Control/Status Register (OCSR) Bit Definitions (Cont)

I/O	Bit	Definition
CONI	03	LAST AN10 BIT signal. The OCON LAST AN10 BIT flip-flop is the source for the A2I LAST AN10 BIT signal on the AN10/AN20-IMP cable during normal operation and is internally simulated as an AN10/AN20-IMP signal during diagnostic loop modes. This flip-flop is set upon detection that the bit to be transmitted is the last bit of the message. The A2I LAST AN10 BIT signal is described in Section 3.3.1.
CONI	04	Currently undefined.
CONI	05	Currently undefined.
CONI	06–11	The Output Data Register shift counter. It is cleared by DATAO to the Output Data Register (ODR) and by RESET.
CONI	12	OUT 32 BITS. Asserted whenever 32 or more bits have been shifted out of the Output Data Register (ODR) and into the OCON AN10 TO IMP DATA flip-flop for transmitting to the IMP. Cleared by the DATAO that loads a new word in the ODR and by RESET.
CONI	13	OUT 36 BITS. Asserted whenever 36 bits have been shifted out of the Output Data Register (ODR) and into the OCON AN10 TO IMP DATA flip-flop for transmitting to the IMP. Cleared by the DATAO that loads a new word into the ODR and by RESET.
CONI	14	Currently undefined.
CONI	15	Currently undefined.
CONI	16	OUT MSG BUSY. OUT MSG BUSY is set upon start of a message transfer and remains set until the last bit of the last block of the message is transmitted to the IMP. It facilitates segmenting the message into multiple data blocks since it is not affected by the setting of OUT WCOF and the attendant clearing of OUT BUSY. It is cleared only at the end of the total message when OUT DONE is set, or by RESET. OUT MSG BUSY also enables output transfers to the IMP and thereby provides the mechanism for the last bit of a word or message block segment to be transmitted to the

Table 3-1 Output Control/Status Register (OCSR) Bit Definitions (Cont)

I/O	Bit	Definition
CONI (Cont)	16	IMP concurrent with the interrupt request for more data (either OUT WCOF or OUT DATA REQ). The message termination interrupt, OUT DONE, will not, however, be issued to the host until the last message bit has been received by the IMP.
CONI	17	ODR RDY (Output Data Register Ready), when asserted, indicates that there is data in the Output Data Register (ODR). This status flag is used to synchronize the data bit transfer logic with requests for additional host words to be loaded in the ODR for transmission. It is set by the DATAO transfer of a Host word to the ODR if OUT BUSY is set. It is cleared by the AN10/AN20 concurrent with transmission of the last bit of a word and by RESET.
CONO/CONI	18	Currently undefined.
CONO/CONI	19	IMP PORT DISABLED. When asserted, this bit disables the IMP cable drivers and receivers for diagnostic purposes. When not asserted, it directly clears OUT LOOP, LOOPBACK, IN LOOP, IVAR IMP TO AN10 DATA, and IVAR LAST IMP BIT. It is directly cleared with MAINT MODE unasserted. It may be set by CONO concurrent with the setting of MAINT MODE.
CONO/CONI	20	MAINT MODE. MAINT MODE is set and cleared by CONO. When set, it places the AN10/AN20 in maintenance mode and in conjunction with IMP PORT DISABLED enables setting of all maintenance functions in the Input Vector Address Register (IVAR) and the Output Vector Address Register (OVAR). (Refer to definition of OCSR bit 19 for a listing of the OVAR and IVAR maintenance bits that require IMP PORT DISABLED to be set in conjunction with MAINT MODE.) Bits in the OCSR set/cleared in conjunction with MAINT MODE may be operated on by the same CONO. MAINT MODE is cleared by RESET. The clearing of MAINT MODE also clears the diagnostic functions defined in the OVAR and IVAR as well as IMP PORT DISABLED.
CONO/CONI	21	Currently undefined.

Table 3-1 Output Control/Status Register (OCSR) Bit Definitions (Cont)

I/O	Bit	Definition
CONO/CONI	22	OUT DATA REQ. When asserted, this bit indicates that the AN10/AN20 is ready for a new data word to transmit. It is set by the AN10/AN20 when it is ready for a new data word; it is cleared by the DATAO to the ODR of a new word, by RESET, and by CONO with writing a zero to bit 22. It generates an interrupt on the DATA PI channel. For diagnostic purposes, OUT DATA REQ may be set by CONO of bit 22 if MAINT MODE (bit 20) is set. The register select bits (bits 28 and 29) are initialized to 00 when OUT DATA REQ is set.
CONO/CONI	23	OUT DONE. OUT DONE is cleared by CONO when writing a zero to bit 23 and by RESET. It is setable by CONO with bit 23 asserted only when MAINT MODE is set. It is also set upon transmission of the last bit of the message to the IMP, as specified by END MSG (bit 27). It clears OUT BUSY (bit 26), and generates a status interrupt. This definition applies to both standard and vector modes of interrupt service.
CONO/CONI	24	OUT WCOF (Output Word Count Overflow). OUT WCOF is cleared by CONO when writing a zero to bit 24 and by RESET. It is setable by CONO with bit 24 asserted only when MAINT MODE (bit 20) is set. OUT WCOF works in conjunction with END MSG (bit 27). It is set upon transmission of the last bit of the word which results in the word count register decrementing to zero; i.e., upon transmission of the last bit of the message block. The setting of OUT WCOF thus signifies the AN10 has transferred to the IMP the last bit of the message block and is waiting for the next block of the message. This feature provides message segmenting across page boundaries, data mode switching within a message, and gather-read capability. Upon transmission of the last bit of the message block in the case where END MSG is set, OUT DONE (bit 23) is set in addition to OUT WCOF. OUT WCOF causes a status interrupt. Setting OUT WCOF clears OUT BUSY (bit 26) which in turn clears OUT MODE 36 (bit 25). This definition applies to both standard and vector modes of interrupt service.

Table 3-1 Output Control/Status Register (OCSR) Bit Definitions (Cont)

I/O	Bit	Definition
CONO/CONI	25	OUT MODE 36. OUT MODE 36 is set and cleared by CONO of bit 25. It controls the data format mode. When set, OUT MODE 36 specifies 36 bits of message data per Host word. When cleared, OUT MODE 36 is interpreted to mean OUT MODE 32. That is, each Host word contains 32 bits of left-justified data. OUT MODE 36 is cleared when OUT BUSY (bit 26) is cleared (i.e., when OUT WCOF or OUT DONE sets) and by RESET. The data mode should be selected concurrently with setting OUT BUSY.
CONO/CONI	26	OUT BUSY. OUT BUSY is set by CONO of bit 26 (binary one) at CONO SET pulse time to initiate an output transfer. Setting OUT BUSY sets OUT DATA REQ (bit 22) to prime the first data interrupt request. OUT BUSY is cleared by assertion of either OUT DONE (bit 23) or OUT WCOF (bit 24) which in turn clears OUT MODE 36 (bit 25). As OUT BUSY is cleared in this manner, the REGISTER SELECT BITS (bits 28 and 29) are set to 01 to select the Output Word Count/Address Register (OWAR) preparatory to loading a new word count and current address by DATAO. OUT BUSY can also be cleared by CONO if bit 26 is a binary zero.
CONO/CONI	27	END MSG. END MSG is set and cleared by CONO of bit 27. END MSG must be set along with OUT BUSY (bit 26) in order to specify that a given message block is the last block of the message and that upon transmission of the last bit of the last word of that block to the IMP, OUT DONE (bit 23), in addition to OUT WCOF (bit 24), should be set. Note that the A21 LAST AN10 BIT signal is issued to the IMP concurrent with transmission of the last message bit.
CONO/CONI	28–29	REGISTER SELECT. The REGISTER SELECT bits are programmable in both standard and vector interrupt mode of operation. They are set and cleared by CONO of bits 28–29 and determine the destination (or source) register for subsequent DATAOs (or DATAIs) according to the following code. 00 Output Data Register (ODR) 01 Output Word Count/Address Register (OWAR) 10 Output Vector Address Register (OVAR)

Table 3-1 Output Control/Status Register (OCSR) Bit Definitions (Cont)

I/O	Bit	Definition
		The setting of OUT DATA REQ (bit 22) initializes the register selection to 00, addressing the output data register for subsequent DATAO(I) execution. Only when OUT BUSY (bit 26) and OUT DATA REQ (bit 22) are cleared may the register selection be changed by CONO for diagnostic and maintenance purposes. The termination of a message, or message block, clears OUT BUSY which in turn sets the register selection to 01 to address the Output Word Count/Address Register in anticipation of loading a new message block count and address pointer.
CONO/CONI	30–32	STATUS PI CHANNEL. The status PI assignment is set and cleared by CONO of bits 30–32. These bits specify the PI channel over which AN10/AN20 status interrupts are generated. Defined status interrupts are OUT DONE and OUT WCOF.
CONO/CONI	33–35	DATA PI CHANNEL. The data PI assignment is set and cleared by CONO of bits 33–35. These bits specify the PI channel over which OUTput DATA REQuest interrupts are generated.

Table 3-2 Multiplexer Selection of READY FOR AN10 BIT Source Signal Decode Chart

OVAR MAINTENANCE SIGNALS			"READY FOR AN10 BIT" Source Signal
LOOP BACK	OUT LOOP	OUT S CYC	
0	0	0	12A RDY FOR AN10 BIT (IMP Cable)
0	0	1	OVAR RDY FOR AN10 BIT
0	1	0	-OCON YOUR AN10 BIT
0	1	1	OVAR RDY FOR AN10 BIT
1	0	0	ICON RDY FOR IMP BIT
1	0	1	OVAR RDY FOR AN10 BIT

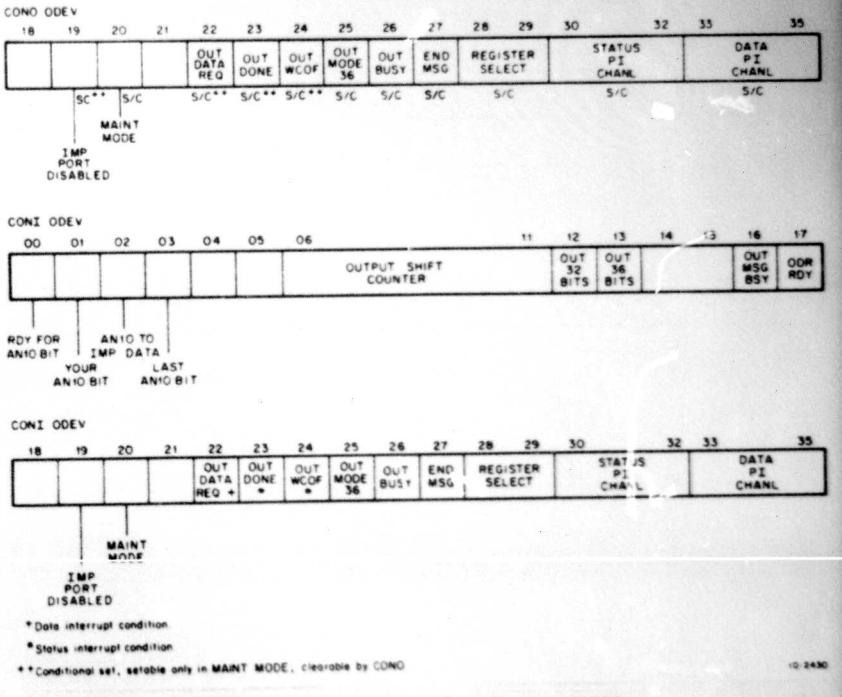


Figure 3-4 Output Control/Status Register (OCSR)

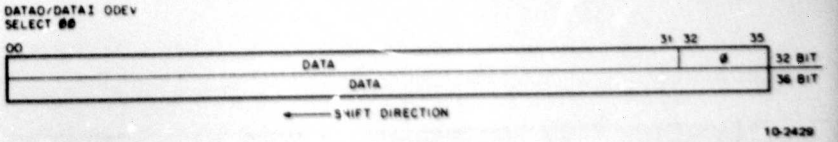


Figure 3-5 Output Data Register (ODR)

3.4.1.2 Output Data Register (ODR) – The Output Data Register (ODR) (Figure 3-5) is a 36-bit shift register that is loadable and readable by DATAO and DATAI, respectively. The ODR is selected by a Register Select bit code of 00 (OCSR bits 28 and 29), and is unconditionally selected (Register Select bits initialized by 00) by the setting of OUT DATA REQ (OCSR bit 22). In 32-bit mode, only the leftmost 32 bits are loaded and read. For data transfers to the IMP, the most significant bit is shifted out first. The ODR is cleared by RESET.

3.4.1.3 Output Word Count/Address Register (OWAR) - The Output Word Count/Address Register (OWAR) is a 36-bit register loadable and readable by DATAO and DATAI, respectively. It is selectable and *must be used* in both standard interrupt and DATAO interrupt modes of operation. It is selected by a REGISTER SELECT bit code of 01 (OCSR bits 28 and 29). The REGISTER SELECT bits are automatically switched to code 01 upon the clearing of OUT BUSY (OCSR bit 26) in anticipation of loading a new word count/current address.

This register supplies the address parameter information for the API function word of the DATAO (function 4) interrupt request. In addition, it contains the 12-bit WORD COUNT parameter necessary for termination control of the block transfer. An 18-bit DATA ADDRESS is supplied for the KI10 and a 23-bit DATA ADDRESS plus QUALIFIER is supplied for the KL10. The QUALIFIER specifies relocation and protection in accordance with the KL10 API function word format. The KI10 API bit (bit 11) of the Output Vector Address Register (OVAR) controls the selection of KL10 or KI10 API function word format. The WORD COUNT is *decremented* and the DATA ADDRESS is *incremented* following each output data transfer. The OWAR is cleared by RESET.

Note that all 23 bits of the DATA ADDRESS are incremented regardless of the API format selection. The API format selection only determines what is gated to the API function word. For a KA10 standard (API function 1) type interrupt, bits 13–35 are not asserted on the I/O bus and are therefore not used. The word count must still be programmed, however.

All bit positions of the OWAR are illustrated in Figure 3-6 and defined in Table 3-3.

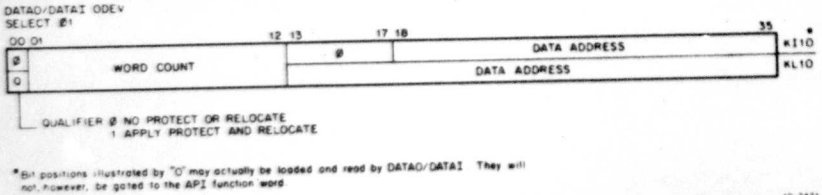


Figure 3-6 Output Word Count/Address Register (OWAR)

Table 3-3 Output Word Count/Address Register (OWAR) Bit Definitions

Format	Bit	Definition
KI API	00	This bit is not used in KI10 API format mode. Although it can be loaded and read by DATAO/DATAI, it is not gated to the KI10 API function word.
KL API	00	QUALIFIER. Loaded by DATAO and read by DATAI. When set, QUALIFIER asserts bit 6 (Q) in the KL10 API function word format to specify protection and relocation to be applied to the DATAO interrupt (API function 4) operand address.
KI/KL API	01–12	WORD COUNT. Loaded by DATAO and read by DATAI. This 12-bit word count must be loaded with the message block size in Host words. The count is decremented by one following each DATAO to the Output Data Register (ODR).
KI API	13–17	These bits are not used in KI10 API format mode. Although they can be loaded and read by DATAO/DATAI and will count in conjunction with bits 18–35, they are not gated to the I/O bus for the KI10 API format.
KI API	18–35	DATA ADDRESS. These bits form an 18-bit data address counter which supplies the 18-bit data address for the KI10 API function 4 (DATAO) interrupt. That is, they specify the operand address for the DATAO. They can be loaded by DATAO and read by DATAI. Initially loaded with the address of the first word to be transferred, the counter is incremented by one after each DATAO interrupt.
KL API	13–35	DATA ADDRESS. Same description as for bits 18–35 in KI format except that all 23 bits of the data address counter are enabled to the KL10 API function word.

3.4.1.4 Output Vector Address Register (OVAR) - The Output Vector Address Register (OVAR) is a 36-bit register loadable and readable by DATAO and DATAI, respectively. It is selectable in both standard and vector interrupt modes of operation and is selected by a REGISTER SELECT-bit code of 10 (OCSR bits 28 and 29). The right portion (bits 13–35) of the register contains the VECTOR ADDRESS for a status/control vectored interrupt (API function 2) and thus has meaning only in vector mode of interrupt service. Bits 00, 01, 04, 05, and 06 of the left portion of the register contain diagnostic control bits and bits 11 and 12 are control bits for selecting the output direction interrupt mode. The diagnostic control bits can be set only when MAINT MODE (OCSR bit 20) and IMP

PORT DISABLED (OCSR, bit 19) are set. When MAINT MODE is cleared, the diagnostic function bits are cleared. The API format mode bit 11 (OUT KI10 API) has meaning only when bit 12 (OUT STD INT) is cleared. With OUT KI10 API (bit 11) set, KI10 API format is specified for device interrupt (i.e., 18-bit vector and DATAO interrupt address pointers); when OUT KI10 API is cleared, KL10 API format is specified for device interrupt (i.e., 23-bit vector and DATAO interrupt address pointers). When OUT STD INT (bit 12) is set, KA10 standard (not vector) interrupt mode is specified; OUT KI10 API (bit 11) is meaningless, and all API interrupts are generated as function type 1 (i.e., bits 13–35 are not transmitted on the I/O bus). When OUT STD INT is cleared, vector interrupt mode is specified and status/control interrupts are generated as API function 2 (vector) and output data interrupts are API function 4 (DATAO). The OVAR is initialized by RESET. The default interrupt mode of the AN10/AN20 is for KL10 API format with vectored interrupts.

Each bit position of the OVAR is illustrated in Figure 3-7 and defined in Table 3-4.

The interrupt modes supportable on the various CPU types are defined in Table 3-5.

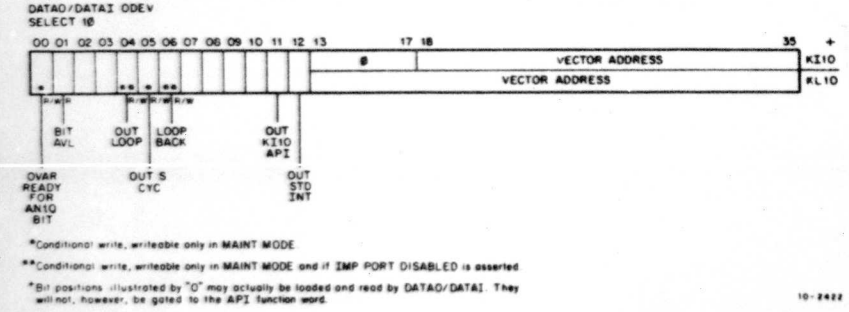


Figure 3-7 Output Vector Address Register (OVAR)

Table 3-4 Output Vector Address Register (OVAR) Bit Definitions

Format	Bit	Definition
N/A	00	OVAR RDY FOR AN10 BIT. The OVAR RDY FOR AN10 BIT is a diagnostic status flag indicating that the IMP is ready for another data bit. OVAR RDY FOR AN10 BIT is readable by a DATAI of OVAR and is writable by a DATAO to OVAR only when MAINT MODE (OCSR bit 20) is set. The programmable writing of OVAR RDY FOR AN10 BIT is for diagnostic purposes only, and is used in conjunction with the diagnostic loop capabilities to simulate the IMP's readiness for data. Either RESET or clearing of MAINT MODE clears this flip-flop.
N/A	01	BIT AVL (BIT AVAILABLE). The OCON BIT AVL bit is a status flag indicating that the AN10 has a data bit assembled and ready for transmission to the IMP. BIT AVL controls the assertion of the A21 YOUR AN10 BIT Signal on the AN10/AN20-IMP cable. It is cleared by the AN10/AN20 when the IMP takes the data bit as indicated by the negation of the I2A RDY FOR AN10 BIT signal. It is useful diagnostically for monitoring proper operation of the AN10/AN20 in the diagnostic loop back modes. BIT AVL is a read-only bit readable by a DATAI of OVAR. It is cleared by RESET and when OUT MSG BSY is unasserted.
N/A	02	Currently undefined.
N/A	03	Currently undefined.
N/A	04	OUT LOOP. OUT LOOP is a read/write diagnostic control bit writeable only when MAINT MODE (OCSR bit 20) is set and when IMP PORT DISABLED is asserted. When set, OUT LOOP internally connects the demand/response data handshake control signals together in a manner that self-sustains the AN10/AN20 data output for the duration of the message length. This feature permits diagnosability of the AN10/AN20 output device section and may be used in conjunction with OUT S CYC (OVAR bit 05). While AN10 READY does not need to be set, I2A IMP READY will be internally generated by the AN10/AN20 425 ms after setting OUT LOOP in order to enable the data handshake signal gating. OUT LOOP is cleared by RESET and by the clearing of MAINT MODE and IMP PORT DISABLED. It is disabled by LOOP BACK (OVAR bit 06).

Table 3-4 Output Vector Address Register (OVAR) Bit Definitions (Cont)

Format	Bit	Definition
N/A	05	OUT S CYC (Out Single Cycle). OUT S CYC is a read/write diagnostic control bit writeable only when MAINT MODE (OCSR bit 20) is set. When set, OUT S CYC selects OVAR RDY FOR AN10 BIT as the source for the OCON RDY FOR AN10 BIT signal rather than I2A RDY FOR AN10 BIT on the AN10/AN20-IMP cable. In this manner, the demand/response handshake sequence necessary for transferring data bits is interrupted and may be diagnostically simulated. OVAR RDY FOR AN10 BIT must be programmably set and cleared to cycle the AN10/AN20 data handshake sequence. Using this feature, AN10/AN20 output transfers may be single-stepped for diagnostic purposes. OUT S CYC works in conjunction with the mutually exclusive bits OUT LOOP (OVAR bit 04) and LOOP BACK (OVAR bit 06). It is cleared by RESET and by the clearing of MAINT MODE.
N/A	06	LOOP BACK. LOOP BACK is a read/write diagnostic control bit writeable only when MAINT MODE (OCSR bit 20) is set and when IMP PORT DISABLED is asserted. When set, LOOP BACK internally connects the output and input data and data handshake control signals together in a manner that the AN10/AN20 will self-sustain transmitting data to itself. Both the output and input sections must be programmed in order to support data loop back. AN10 READY (IVAR bit 10) must be set in order to internally simulate I2A IMP READY and to qualify the data handshake signal gating. For further diagnosis, this internal data loop back may be single stepped by setting either or both OUT S CYC (OVAR bit 05) and IN S CYC (IVAR bit 05). LOOP BACK disables OUT LOOP and IN LOOP. It is cleared by RESET and by the clearing of MAINT MODE and IMP PORT DISABLED. I2A IMP READY sets 425 ms after the logical ANDing of OVAR LOOP BACK and IVAR AN10 READY. Note, however, that IVAR AN10 READY does not set until 30 ms after the DATAO command to the IVAR.
N/A	07–10	Currently undefined.

Table 3-4 Output Vector Address Register (OVAR) Bit Definitions (Cont)

Format	Bit	Definition
N/A	11	OUT KI10 API. OUT KI10 API is loaded by DATAO and read by DATAI. This bit is defined only when OVAR bit 12 (OUT STD INT) is cleared. When set, it specifies KI10 API format for output device interrupts. That is, vector and DATAO interrupt pointers are 18-bit. When cleared, KL10 API format is specified; i.e., 23-bit address pointers for vector and DATAO interrupts. OUT KI10 API is cleared by RESET.
N/A	12	OUT STD INT (Output Standard Interrupt). OUT STD INT is loaded by DATAO and read by DATAI. This bit specifies the interrupt mode type for output device interrupts. When cleared: a. Selects vector interrupt mode. b. Status interrupts are generated as API function 2 (vector). c. Output data interrupts are generated as API function 4 (DATAO). d. KI10 or KL10 API format is as designated by OVAR bit 11. When set: a. Selects KA10 standard (not vector) interrupt mode. b. Definition of OVAR bit 11 is disabled. c. All API interrupts are generated as function type 1. When no IOB PI REQ SYNC and IOB PI GRANT is generated on the I/O bus (e.g., KA10 host CPU connection), no API function word is transferred. OUT STD INT is cleared by RESET.
KI API	13–17	These bits are not used in KI10 API format mode. Although they can be loaded and read by DATAO/DATAI, they are not gated to the I/O bus for a KI10 API function word transfer.

Table 3-4 Output Vector Address Register (OVAR) Bit Definitions (Cont)

Format	Bit	Definition
KI API	18–35	VECTOR ADDRESS. The VECTOR ADDRESS is an 18-bit register which supplies the interrupt vector address for KI10 API function 2 (status) interrupts from the AN10/AN20 output device section.
KL API	13–35	VECTOR ADDRESS. The KL API VECTOR ADDRESS has the same definition as bits 18–35 in KI API format, except that this is a 23-bit register for supplying the vector address in accordance with the KL10 API function word format.

Table 3-5 Interrupt Modes Correlated to CPU Types

	CPU Type		
OVAR Bits 11–12 Code	KA10	KI10	KL10
00	No	No	Yes
01	Yes	Yes	Yes
10	No	Yes	Yes
11	Yes	Yes	Yes

3.4.1.5 Input Control/Status Register (ICSR) - Each bit position of the Input Control/Status Register (ICSR) is illustrated in Figure 3-8 and defined in Table 3-6.

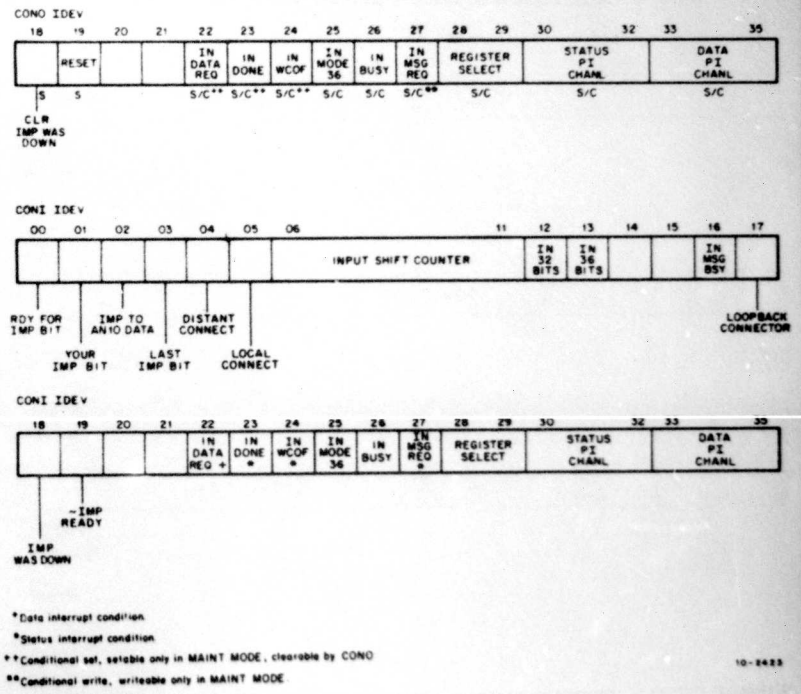


Figure 3-8 Input Control/Status Register (ICSR)

Table 3-6 Input Control/Status Register (ICSR) Bit Definitions

I/O	Bit	Definition
CONI	00	READY FOR IMP BIT signal. The ICON RDY FOR IMP BIT flip-flop is the source for the A21 RDY FOR IMP BIT signal on the AN10/AN20-IMP cable during normal operation and is internally simulated as an AN10/AN20-IMP signal during diagnostic loop modes. The ICON RDY FOR IMP BIT flip-flop is initially set by the setting of IVAR AN10 READY. Thereafter it is set upon completion of a data handshake sequence. It is cleared by clearing IVAR AN10 READY, by RESET, and by the process of receiving I2A YOUR IMP BIT from the IMP to shift in the data.
CONI	01	YOUR IMP BIT signal. The ICON YOUR IMP BIT signal is the received I2A YOUR IMP BIT signal on the AN10/AN20-IMP cable during normal operations and is internally simulated as an AN10/AN20-IMP signal during diagnostic loop modes. The ICON YOUR IMP BIT signal is the output of a multiplexer which selects one of several source signals as defined in Table 3-7 (the multiplexer is enabled by I2A IMP READY). The I2A YOUR IMP BIT signal is described in Section 3.3.1.
CONI	02	IMP TO AN10 DATA signal. The ICON IMP TO AN10 DATA signal is the received I2A IMP TO AN10 DATA signal on the AN10/AN20-IMP cable during normal operation and is internally simulated as an AN10/AN20-IMP signal during diagnostic loop modes. ICON IMP TO AN10 DATA is the output of a multiplexer which selects one of several source signals as defined in Table 3-8 (the multiplexer is enabled by I2A IMP READY). The I2A IMP TO AN10 DATA signal is described in Section 3.3.1.
CONI	03	LAST IMP BIT signal. The ICON LAST IMP BIT signal is the received I2A LAST IMP BIT signal on the AN10/AN20-IMP cable during normal operation and is internally simulated as an AN10/AN20-IMP signal during diagnostic loop modes. ICON LAST IMP BIT is the output of a multiplexer which selects one of several source signals as defined in Table 3-9 (the multiplexer is enabled by I2A IMP READY). Refer to Section 3.3.1 for further information pertaining to I2A LAST IMP BIT.

Table 3-6 Input Control/Status Register (ICSR) Bit Definitions (Cont)

I/O	Bit	Definition
CONI	04	DISTANT CONNECTION. When DISTANT CONNECTION is set, it indicates that the distant receiver/driver interface is enabled. Selection of the DISTANT CONNECTION bit is controlled by a switch on the M8612 module. This selection is independent of the handshake mode selection.
CONI	05	LOCAL CONNECTION. When LOCAL CONNECTION is set it indicates that the local receiver/driver interface is enabled. Selection of the LOCAL CONNECTION bit is controlled by a switch on the M8612 module. This selection is independent of the handshake mode selection.
CONI	06–11	The input data register shift counter. The counter is cleared by DATAI of the Input Data Register (IDR) and by RESET.
CONI	12	IN 32 BITS. Asserted whenever 32 or more bits have been shifted into the Input Data Register (IDR) from the IMP. Cleared by a DATAI of the IDR and by RESET.
CONI	13	IN 36 BITS. Asserted whenever 36 bits have been shifted into the Input Data Register (IDR) from the IMP. Cleared by a DATAI of the IDR and by RESET.
CONI	14	Currently undefined.
CONI	15	Currently undefined.
CONI	16	IN MSG BUSY. IN MSG BUSY is a status flag indicating that an input message is in process. It is set after receipt of the first bit of the first word of the message. It is the reception of this first bit that causes an IN MSG REQ interrupt over the status PI channel to signal the Host that a message is ready to be received. IN MSG BUSY is not cleared until the last bit of the message is received and IN DONE (bit 23) is set. IN MSG BUSY enables the input data handshake control and facilitates segmenting the input message into multiple data blocks. Besides being cleared by IN DONE, IN MSG BUSY, is also cleared by RESET.
CONI	17	LOOPBACK CONNECTOR. LOOPBACK CONNECTOR is asserted whenever the local AN10/AN20 loopback test connector (70-13963) is installed in place of the AN10/AN20-IMP cable.

Table 3-6 Input Control/Status Register (ICSR) Bit Definitions (Cont)

I/O	Bit	Definition
CONI	18	IMP WAS DOWN. ICSR IMP WAS DOWN is set by the assertion of I2A IMP READY (bit 19 a zero). It indicates that the READY line of the IMP "flapped" (i.e., the IMP went down and came back up). The last message in transit, if any, must be discarded and error recovery procedures invoked. This bit is a status-flag only and generates no interrupt. It does not halt any message transmission and should be examined by software before and after each message input or output. It is also set by device RESET (bit 19), IOB RESET, or system power up. It is cleared by CLR IMP WAS DOWN. It is used in conjunction with bit 19 (-IMP READY) to indicate the four states that might occur during a message transmission: (1) IMP is up and has not been down, (2) IMP was down but is now up, (3) IMP is now down, and (4) IMP was down and is down again; refer to Table 3-10 for ICSR bits 18 and 19 truth table.
CONO	18	CLR IMP WAS DOWN. CLR IMP WAS DOWN, when asserted, clears the ICSR IMP WAS DOWN error condition.
CONI	19	-IMP READY. -IMP READY, when asserted, means that the IMP is down (i.e., the I2A IMP MASTER READY line of the IMP is not asserted). This condition indicates the IMP has malfunctioned or has detected an error in the message transmission between the AN10/AN20 and the IMP. The IMP momentarily "flaps" the READY line to notify the AN10/AN20 of an IMP error or IMP detected error. Assertion of IMP READY causes the IMP WAS DOWN bit to set. Refer to Table 3-10 for ICSR bits 18 and 19 truth table. The I2A IMP READY flag also gates the OCON RDY FOR AN10 BIT, ICON IMP TO AN10 DATA, ICON LAST IMP BIT, and ICON YOUR AN10 BIT signal multiplexers. A 425 ms delay for relay debounce is provided between the time the I2A IMP MASTER READY line is asserted and the time the I2A IMP READY flip-flop sets (negation of bit 19).

Table 3-6 Input Control/Status Register (ICSR) Bit Definitions (Cont)

I/O	Bit	Definition
		For diagnostic purposes, a local IMP READY is simulated in the AN10/AN20 (LOCAL IMP READY = OUT LOOP + IN LOOP + LOOP BACK • AN10 READY). Again, a 425 ms delay for relay debounce is provided between the time the LOCAL IMP READY condition is asserted and the time I2A IMP READY sets.
CONO	19	RESET. RESET (set only) initializes all status conditions associated with the AN10/AN20 input and output sections. RESET unconditionally sets ICSR IMP WAS DOWN to guarantee hardware and software synchronization with the IMP. The function of RESET is identical to that of IOB RESET.
CONO/CONI	20	Currently undefined.
CONO/CONI	21	Currently undefined.
CONO/CONI	22	IN DATA REQ. IN DATA REQ indicates that the AN10/AN20 has assembled a word of bits from the IMP and is ready for the Host to take it by DATAI. IN DATA REQ is a data interrupt condition, requires IN BUSY to be set as a prerequisite, and is set by the AN10/AN20 upon assembly of either a 32-bit or 36-bit Host word as specified by IN MODE 36 (bit 25). Until IN BUSY is set, a maximum of 32 bits may be assembled by the AN10/AN20. The IN DATA REQ data interrupt is cleared by; (1) DATAI of the assembled word, (2) RESET, and (3) by a CONO writing a zero to bit 22. As soon as the Input Data Register (IDR) is emptied (by DATAI), the AN10/AN20 will input additional bits for another word. For diagnostic purposes, IN DATA REQ may be set by CONO bit 22 if MAINT MODE (OCSR bit 20) is set. The REGISTER SELECT bits (bits 28 and 29) are initialized to 00 when IN DATA REQ is set.

Table 3-6 Input Control/Status Register (ICSR) Bit Definitions (Cont)

I/O	Bit	Definition
CONO/CONI	23	IN DONE. IN DONE is cleared by a CONO that writes a binary zero to bit 23 and by RESET. It is setable by a CONO with bit 23 asserted only when MAINT MODE is set. It is also set upon storing in memory (via DATAI) the last bit of the message, including any padding. As it sets, IN BUSY is cleared. Concurrent with transmission of the last message bit, including IMP padding, the IMP asserts the I2A LAST IMP bit signal which generates ICON LAST IMP BIT which in turn sets ICON LAST IMP BIT RCVD. The AN10/AN20 pads with zeros any remaining empty bit positions in the word being assembled and issues a DATAI interrupt. As soon as the data buffer is read by DATAI, IN DONE is set which in turn generates a status interrupt to terminate the transfer. Clearing IN DONE clears ICON LAST IMP BIT RCVD. Input word count overflow need not occur in order to set IN DONE.
CONO/CONI	24	IN WCOF (Input Word Count Overflow). IN WCOF is cleared by a CONO that writes a binary zero to bit 24 and by RESET. It is setable by a CONO with bit 24 asserted only when MAINT MODE (OCSR bit 20) is set. It is also set upon storage in memory (via DATAI) of a word which results in the word count register decrementing to zero; i.e., upon storage of the last word of a message block. In WCOF issues a status interrupt to request a new input buffer. This feature facilitates message segmenting across page boundaries, data mode switching within a message, and scatter-write capability. If ICON LAST IMP BIT RCVD is set at the time IN WCOF occurs, IN DONE is also set. Setting of IN WCOF clears IN BUSY (bit 26) which in turn clears IN 36 BITS (bit 13). If IN DONE is not set, the AN10/AN20 is free to assemble another word of 32 bits concurrent with setup of a new input message block. This definition applies to both standard and vector modes of interrupt service.

Table 3-6 Input Control/Status Register (ICSR) Bit Definitions (Cont)

I/O	Bit	Definition
CONO/CONI	25	IN MODE 36. IN MODE 36 is set and cleared by a CONO of bit 25. It controls the data format mode. When set, IN MODE 36 specifies 36 bits of message data per Host word. When cleared, IN MODE 36 is interpreted as MODE 32. That is, each Host word contains 32 bits of data, left-justified. IN MODE 36 is cleared (1) when IN BUSY (bit 26) is cleared (e.g., by IN WCOF or IN DONE), and (2) by RESET. The data mode should be selected concurrently with setting IN BUSY.
CONO/CONI	26	IN BUSY. IN BUSY is set by a CONO of bit 26 at CONO SET pulse time to initiate an input transfer in response to an IN MSG REQuest status interrupt. Upon setting IN BUSY, if MODE 32 is selected and 32 bits are assembled, an immediate data interrupt is issued; otherwise the additional required bits are assembled. IN BUSY should not be set until the IN MSG REQ status interrupt is received. IN BUSY is cleared by assertion of either IN DONE (bit 23) or IN WCOF (bit 24) which in turn clears IN MODE 36 and sets the REGISTER SELECT BITS to 01 to select the Word Count/Address Register (IWAR) in anticipation of loading a new word count and current address by DATAO. IN BUSY can be cleared by a CONO that writes a zero to bit 26.
CONO/CONI	27	IN MSG REQuest. IN MSG REQ is a status interrupt flag that sets upon receipt of the first bit of the message from the IMP. It is cleared by setting IN BUSY and by RESET. IN MSG REQ indicates that the IMP has a message available and an input transfer needs to be initiated. For diagnostic purposes, IN MSG REQ may be written by CONO of bit 27 if MAINT MODE is set.

Table 3-6 Input Control/Status Register (ICSR) Bit Definitions (Cont)

I/O	Bit	Definition
CONO/CONI	28–29	REGISTER SELECT. The REGISTER SELECT bits are programmable in both standard and vector interrupt mode of operation. They are set and cleared by CONO of bits 28–29 and determine the destination (or source) register for subsequent DATAOs (or DATAIs) according to the following decode. 00 Input Data Register (IDR) 01 Input Word Count/Address Register (IWAR) 10 Input Vector Address Register (IVAR) Setting IN DATA REQ (bit 22) initializes the register selection to 00, addressing the Input Data Register (IDR) for subsequent DATAO(I) execution. The register selection may be changed by a CONO for diagnostic and maintenance purposes. The termination of a message, or message block, clears IN BUSY which in turn sets the register selection to 01 to address the Input Word Count/Address Register (IWAR) in anticipation of loading a new message block count and address pointer.
CONO/CONI	30–32	STATUS PI CHANNEL. The status PI assignment is set and cleared by a CONO of bits 30–32. These bits specify the PI channel over which AN10/AN20 status interrupts are generated. Defined status interrupts are IN DONE, IN WCOF, and IN MSG REQ.
CONO/CONI	33–35	DATA PI CHANNEL. The data PI assignment is set and cleared by a CONO of bits 33–35. These bits specify the PI channel over which INput DATA REQuest interrupts are generated.

Table 3-7 Multiplexer Selection of YOUR IMP BIT Source Signal Decode Chart

IVAR/OVAR MAINTENANCE SIGNALS			"YOUR IMP BIT" Source Signal
LOOP BACK	IN LOOP	IN S CYC	
0	0	0	I2A YOUR IMP BIT (IMP Cable)
0	0	1	IVAR YOUR IMP BIT
0	1	0	ICON RDY FOR IMP BIT
0	1	1	IVAR YOUR IMP BIT
1	0	0	OCON YOUR AN10 BIT
1	0	1	IVAR YOUR IMP BIT

Table 3-8 Multiplexer Selection of IMP TO AN10 DATA Source Signal Decode Chart

IVAR/OVAR MAINTENANCE SIGNALS		"IMP TO AN10 DATA" Source Signal
LOOP BACK	IN LOOP	
0	0	I2A IMP TO AN10 DATA (IMP Cable)
0	1	IVAR IMP TO AN10 DATA
1	0	OCON AN10 TO IMP DATA

Table 3-9 Multiplexer Selection of LAST IMP BIT Source Signal Decode Chart

IVAR/OVAR MAINTENANCE SIGNALS		"LAST IMP BIT" Source Signal
LOOP BACK	IN LOOP	
0	0	I2A LAST IMP BIT (IMP Cable)
0	1	IVAR LAST IMP BIT
1	0	OCON LAST AN10 BIT

Table 3-10 ICSR Bits 18 and 19 Truth Table

ICSR BIT 18 IMP WAS DOWN	ICSR BIT 19 -IMP RDY	IMP STATUS FOR MESSAGE TRANSMISSION
0	0	IMP IS UP AND HAS NOT BEEN DOWN
1	0	IMP WAS DOWN BUT IS NOW UP
0	1	IMP IS DOWN
1	1	IMP WAS DOWN, CAME UP, BUT IS DOWN AGAIN

3.4.1.6 Input Data Register (IDR) – The Input Data Register (IDR) (Figure 3-9) is a 36-bit shift register readable by DATAI and loadable by DATAO for diagnostic purposes. The IDR is selectable by a REGISTER SELECT bit code of 00 (ICSR bits 28 and 29), and is unconditionally selected (REGISTER SELECT bits initialized to 00) by the setting of IN DATA REQ (ICSR bit 22). In 32-bit mode, only the leftmost 32 bits are read and loaded. For data transfers from the IMP, the most significant bit is shifted in first. The leftmost 32 bits are filled first and then, if 36-bit mode is specified, the rightmost bits are assembled. The IDR is cleared by RESET.

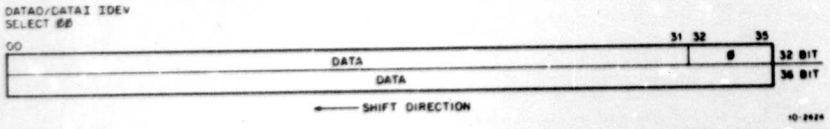


Figure 3-9 Input Data Register (IDR)

3.4.1.7 Input Word Count/Address Register (IWAR) – The Input Word Count/Address Register (IWAR) is a 36-bit register loadable and readable by DATAO and DATAI, respectively. It is selectable and *must be used* in both standard interrupt and DATAI interrupt modes of operation. It is selected by a REGISTER SELECT bit code of 01 (ICSR bits 28 and 29). The REGISTER SELECT bits are automatically switched to code 01 upon the clearing of IN BUSY (ICSR bit 26) in anticipation of loading a new word count/current address.

This register supplies the address parameter information for the API function word of the DATAI (function 5) interrupt request. In addition, it contains the 12-bit WORD COUNT parameter necessary for termination control of the block transfer. An 18-bit DATA ADDRESS is supplied for the KI10 and a 23-bit DATA ADDRESS plus QUALIFIER is supplied for the KL10. The QUALIFIER specifies relocation and protection in accordance with the KL10 API function word format. The IN KL10 API bit (bit 11) of the Input Vector Address Register (IVAR) controls the selection of KL10 or KI10 API function word format. The WORD COUNT is *decremented* and the data address is *incremented* following each input data transfer. The IWAR is cleared by RESET.

Note that all 23 bits of the DATA ADDRESS are incremented regardless of the API format selection. The API format selection only determines what is gated to the API function word. For a standard (API function 1) type interrupt, bits 13–35 are not asserted on the I/O bus and are therefore not used. The word count, however, must be programmed in any case.

All bit positions of the IWAR are defined in Table 3-11 and illustrated in Figure 3-10.

Table 3-11 Input Word Count/Address Register (IWAR) Bit Definitions

Format	Bit	Definition
KI API	00	This bit is not used in KI10 API format mode. Although it can be loaded and read by DATAO/DATAI, it is not gated to the KI10 API function word.
KL API	00	QUALIFIER. Loaded by DATAO and read by DATAI. When set, QUALIFIER asserts bit 6 (Q) in the KL10 API function word format to specify protection and relocation to be applied to the DATAI interrupt API (function 5) operand address.
KI/KL API	01–12	WORD COUNT. Loaded by DATAO and read by DATAI. This 12-bit word count must be loaded with the message block size in Host words. The count is decremented by one following each DATAI to the Input Data Register (IDR).
KI API	13–17	These bits are not used in KI10 API format mode. Although they can be loaded and read by DATAO/DATAI and will count in conjunction with bits 18–35, they are not gated to the I/O bus for the KI10 API format.
KI API	18–35	DATA ADDRESS. These bits form an 18-bit data address counter which supplies the 18-bit data address for the KI10 API function 5 (DATAI) interrupt. That is, they specify the operand address for the DATAI. They can be loaded by DATAO and read by DATAI. Initially loaded with the address of the first word to be transferred, the counter is incremented by one after each DATAI interrupt.

Table 3-11 Input Word Count/Address Register (IWAR) Bit Definitions (Cont)

Format	Bit	Definition
KL API	13–35	DATA ADDRESS. Same description as for bits 18–35 in KI format except that all 23 bits of the data address counter are enabled to the KL10 API function word.

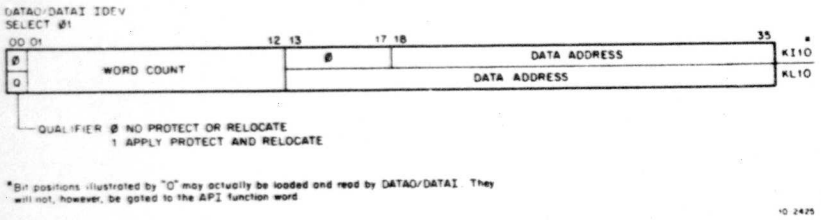


Figure 3-10 Input Word Count/Address Register (IWAR)

3.4.1.8 Input Vector Address Register (IVAR) – The Input Vector Address Register (IVAR) is a 36-bit register loadable and readable by DATAO and DATAI, respectively. It is selectable in both standard and vector interrupt modes of operation and is selected by a REGISTER SELECT bit code of 10 (ICSR bits 28 and 29). The right portion (bits 13–35) of the register contains the VECTOR ADDRESS for a status/control vectored interrupt (API function 2) and thus has meaning only in vector mode of interrupt service. Bits 01–05 of the left portion of the register contain diagnostic status and control bits, bits 06–08 are operational status bits, bit 09 enables 2-way or 4-way handshaking, bit 10 enables AN10 READY status signifying the readiness of the AN10/AN20 to communicate over the network, and bits 11 and 12 are control bits for selecting the input direction interrupt mode. The diagnostic status and control bits can be set only when MAINT MODE (OCSR bit 20) and IMP PORT DISABLED (OCSR bit 19) are set. When MAINT MODE is cleared, the diagnostic status and control bits are cleared. The API format mode bit 11 (IN KI10 API) has meaning only when bit 12 (IN STD INT) is cleared. With IN KI10 API (bit 11) set, KI10 API format is specified for device interrupt (i.e., 18-bit vector and DATAI interrupt address pointers); when IN KI10 API is cleared, KL10 API format is specified for device interrupt (i.e., 23-bit vector and DATAI interrupt address pointers). When IN STD INT (bit 12) is set, KA10 standard (not vector) interrupt mode is specified; IN KI10 API (bit 11) is meaningless, and all API interrupts are generated as function type 1 (i.e., bits 13–35 are not transmitted on the I/O bus). When IN STD INT is cleared, vector interrupt mode is specified and status/control interrupts are generated as API function 2 (vector) and input data interrupts are API function 5 (DATAI). The IVAR is initialized by RESET. The default interrupt mode of the AN10/AN20 is for KL10 API format with vectored interrupts.

Each bit position of the IVAR is defined in Table 3-12 and illustrated in Figure 3-11.

The interrupt modes supportable on the various CPU types are defined in Table 3-13.

Table 3-12 Input Vector Address Register (IVAR) Bit Definitions

Format	Bit	Definition
N/A	00	Currently undefined.
N/A	01	IVAR YOUR IMP BIT. IVAR YOUR IMP BIT is a diagnostic status-flag simulating the IMP's assertion of the YOUR IMP BIT signal on the AN10/AN20-IMP cable. It is readable by DATAI of the IVAR and is writeable by DATAO to the IVAR only when MAINT MODE (OCSR bit 20) is set. The programmable writing of IVAR YOUR IMP BIT is for diagnostic purposes only, and is used in conjunction with the diagnostic loop back capabilities to simulate the IMP's transmission of a data bit to the AN10/AN20. It is cleared by RESET and by clearing MAINT MODE.
N/A	02	IVAR IMP TO AN10 DATA. IVAR IMP TO AN10 DATA is a diagnostic flip-flop simulating the IMP's assertion of the data over the AN10/AN20-IMP cable that is to be shifted into the least significant bit of the IDR. It is readable and writeable by DATAI and DATAO to the IVAR only when MAINT MODE and IMP PORT DISABLED in the OCSR are set. IVAR IMP TO AN10 DATA is the source of data when IN LOOP is set. It is cleared by RESET and by clearing MAINT MODE and IMP PORT DISABLED.
N/A	03	IVAR LAST IMP BIT. IVAR LAST IMP BIT is a diagnostic status-flag simulating the last bit of the IMP data message. It may be read and written by DATAI and DATAO of the IVAR only when MAINT MODE and IMP PORT DISABLED in the OCSR are set. IVAR LAST IMP BIT is the source signal for ICON LAST IMP BIT when IN LOOP (IVAR bit 04) is set. It is cleared by RESET and by clearing MAINT MODE and IMP PORT DISABLED.

Table 3-12 Input Vector Address Register (IVAR) Bit Definitions (Cont)

Format	Bit	Definition
N/A	04	IN LOOP. IVAR IN LOOP (INput LOOP) is a read/write diagnostic control-bit setable only when MAINT MODE and IMP PORT DISABLED in the OCSR are set. When set, IN LOOP internally connects the demand/response data handshake control signals together in a manner that will self-sustain the AN10/AN20 data input until ICON LAST IMP BIT RCVD (IVAR bit 08) is set via IVAR LAST IMP BIT. IVAR IMP TO AN10 DATA is the source of input data. This feature permits diagnosing the AN10/AN20 input device section and may be used in conjunction with IN S CYC (IVAR bit 05). AN10 READY (IVAR bit 10) must be set in order to enable the input timing logic. IN LOOP is cleared by RESET and by the clearing of MAINT MODE and IMP PORT DISABLED. It is disabled by LOOPBACK. IN LOOP generates a local IMP MASTER READY signal which sets I2A IMP READY 425 ms later to enable the data handshake signals.
N/A	05	IN S CYC (IN Single CYCle). IN S CYC is a read/write diagnostic control bit accessible only when MAINT MODE in the OCSR is set. When set, IN S CYC selects IVAR YOUR IMP BIT as the source for the ICON YOUR IMP BIT signal rather than the I2A YOUR IMP BIT signal on the AN10/AN20-IMP cable. In this manner, the demand/response handshake sequence necessary for receiving data bits is interrupted and may be simulated for diagnosis. IVAR YOUR IMP BIT must be set by the program and cleared to cycle the AN10/AN20 data handshake sequence. Using this feature, AN10/AN20 input transfers may be single-stepped for diagnostic purposes. IN S CYC works in conjunction with the mutually exclusive bits IN LOOP (IVAR bit 04) and LOOPBACK (OVAR bit 06). It is cleared by RESET and by the clearing of MAINT MODE.

Table 3-12 Input Vector Address Register (IVAR) Bit Definitions (Cont)

Format	Bit	Definition
N/A	06	ICON YOUR IMP BIT UP. ICON YOUR IMP BIT UP is a flip-flop set by assertion of the ICON YOUR IMP BIT multiplexer output to signify that the IMP is transmitting a data bit. It is cleared approximately 100 ns after being set or after READY FOR IMP BIT has been asserted to the IMP the minimum specified time (100 ns for a local connection or 1.5 μs for a distant connection), whichever occurs last. It is also cleared by RESET. Its purpose is to detect the leading edge of ICON YOUR IMP BIT, a requirement necessary in order to support 2-way handshaking.
N/A	07	ICON I2A DATA. ICON I2A DATA is a flip-flop which stores a copy of the last data bit received and shifted into the input Data Register (IDR). It is loaded at the same time that the data bit is shifted in. It is cleared by RESET.
N/A	08	ICON LAST IMP BIT RCVD. ICON LAST IMP BIT RCVD is a flip-flop set concurrent with shifting into the IDR the last bit of the message as specified by assertion of the ICON LAST IMP BIT multiplexer output. (Refer to the definition of LAST IMP BIT in the ICSR for the possible sources of this signal.) This bit is used to control the padding (zero filling) of any unused bits in the last message word. It is cleared concurrent with the clearing of IN DONE (ICSR bit 23) and by RESET.
N/A	09	2-WAY HANDSHAKE. IVAR 2-WAY HANDSHAKE, when set, enables 2-way handshaking on data input. It may be ready by DATAI, but is loadable by DATAO only when AN10 READY is not asserted. It may, however, be set by DATAO concurrent with the setting of AN10 READY. It is cleared by clearing AN10 READY and by RESET. Clearing 2-WAY HANDSHAKE enables 4-way handshaking. Four-way handshaking of data is recommended except in the case of a distant cable connection of several hundred meters.

Table 3-12 Input Vector Address Register (IVAR) Bit Definitions (Cont)

Format	Bit	Definition
N/A	10	AN10 READY. AN10 READY is loaded by DATAO and may be read 30 ms later by DATAI. When asserted, provided IMP PORT DISABLED is not set, this bit closes the AN10 READY relay to turn around the A2I AN10 RDY TEST signal from the IMP into assertion of the A2I AN10 MASTER RDY signal. AN10 READY applies to both the input and output device sections of the AN10/AN20. It signifies that the AN10/AN20 is powered up, is operational, and that the network control program is loaded (i.e., the AN10/AN20 is ready to communicate over the network). AN10 READY is cleared by a power failure and upon power up, as well as by RESET. When the AN10 READY relay is closed, a 30 ms contact debounce is provided following which AN10 READY may be read by DATAI and the A2I RDY FOR IMP BIT signal is gated to the IMP bus to enable input data transfers. Should an output transfer be programmed and I2A RDY FOR AN10 BIT be asserted, the A2I YOUR AN10 BIT signal will also be asserted following this 30 ms relay closure debounce. AN10 READY is gated to I2A IMP READY in internal diagnostic Loopback mode. When IMP PORT DISABLED is asserted, AN10 READY will still set after the 30 ms relay debounce time out, but the relay will not be closed. This permits diagnostic testing with AN10 READY without affecting a connected IMP.
N/A	11	IN KI10 API. IN KI10 API is loaded by DATAO and read by DATAI. This bit is defined only when IVAR bit 12 (IN STD INT) is cleared. When set, it specifies KI10 API format for input device interrupts. That is, vector and DATAI interrupt address pointers are 18 bits. When cleared, KL10 API format is specified; i.e., 23-bit address pointers for vector and DATAI interrupts. IN KI10 API is cleared by RESET.
N/A	12	IN STD INT (Input Standard Interrupt). In STD INT is loaded by DATAO and read by DATAI. This bit specifies the interrupt mode for input device interrupts.

Table 3-12 Input Vector Address Register (IVAR) Bit Definitions (Cont)

Format	Bit	Definition
		When cleared: a. Selects vector interrupt mode. b. Status interrupts are generated as API function 2 (vector). c. Input data interrupts are generated as API function 5 (DATAI). d. KI10 or KL10 API format is as designated by IVAR bit 11. When set: a. Selects KA10 standard interrupt mode (not vector). b. Definition of IVAR bit 11 is disabled. c. All API interrupts are generated as function type 1. When no IOB PI REQ SYNC and IOB PI GRANT is generated on the I/O bus (e.g., KA10 host CPU), no API function word is transferred. IN STD INT is cleared by RESET.
KI API	13–17	These bits are not used in KI10 API format mode. Although they can be loaded and read by DATAO/DATAI, they are not gated to the I/O bus for a KI10 API function word transfer.
KI API	18–35	VECTOR ADDRESS. The VECTOR ADDRESS is an 18-bit register which supplies the interrupt vector address for KI10 API function 2 (status) interrupts from the AN10/AN20 input device section.
KL API	13–35	VECTOR ADDRESS. The KL API VECTOR ADDRESS has the same definition as bits 18–35 in KI API format, except that this is a 23-bit register for supplying the vector address in accordance with the KL10 API function word format.

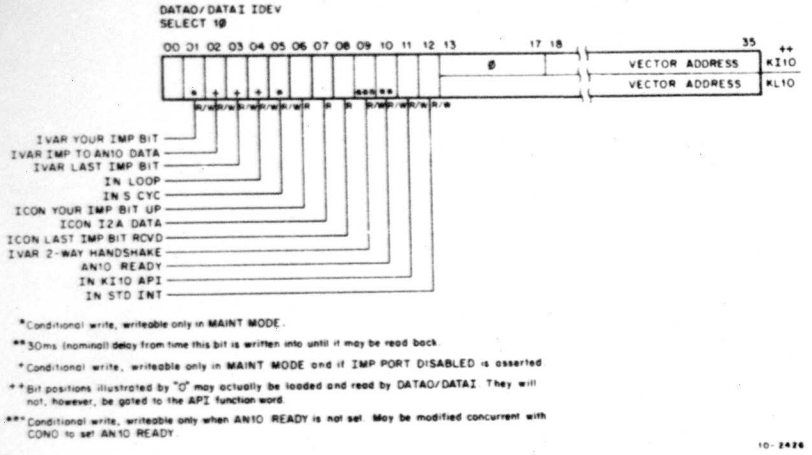


Figure 3-11 Input Vector Address Register (IVAR)

Table 3-13 Interrupt Modes Correlated to CPU Type

IVAR Bits 11 – 12 Code	CPU Type		
	KA10	KI10	KL10
00	No	No	Yes
01	Yes	Yes	Yes
10	No	Yes	Yes
11	Yes	Yes	Yes

3.4.2 API Function Word Format

3.4.2.1 KI10 API Format – KI10 API function word format is enabled with KI10 API (bit 11) asserted and STD INT (bit 12) cleared in both the IVAR and OVAR registers. When so selected, the API function bits asserted on the I/O bus by the AN10/AN20 are illustrated in Figure 3-12.

Table 3-14 lists the KI10 API function code, usage, and the interrupt address source register.

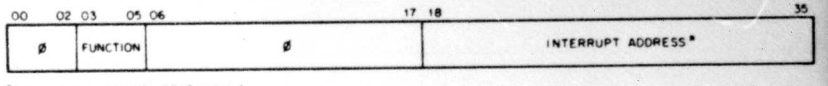


Figure 3-12 KI10 API Format

Table 3-14 KI10 API Function Codes

Function Code	Usage	Interrupt Address Source Register
0	Standard interrupt, KA10	0
1	Standard interrupt, KI10	0
2	Status vector interrupt	OVAR for output IVAR for input
3	Not asserted	Not asserted
4	DATAO data interrupt	OWAR
5	DATAI data interrupt	IWAR
6–7	Not asserted	Not asserted

3.4.2.2 KL10 API Format – KL10 API function word format is enabled with both KI10 API (bit 11) and STD INT (bit 12) cleared in both the IVAR and OVAR registers. When so selected, the API function bits asserted on the I/O bus by the AN10/AN20 are as illustrated in Figure 3-13. Table 3-15 lists the KL10 API function code, usage, and the interrupt address source register. This mode is the default selection for the AN10/AN20.

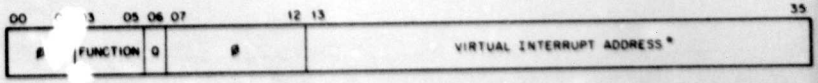


Figure 3-13 KL10 API Format

Table 3-15 KL10 API Function Codes

Function Code	Usage	Q Source	Virtual Interrupt Address Source
0	Standard interrupt, KA10	0	0
1	Standard interrupt, KI10/KL10	0	0
2	Status vector interrupt	0	OVAR for output IVAR for input
3	Not asserted	Not asserted	Not asserted
4	DATAO data interrupt	OWAR	OWAR
5	DATAI data interrupt	IWAR	IWAR
6–7	Not asserted	Not asserted	Not asserted

CHAPTER 4
TECHNICAL DESCRIPTION

4.1 GENERAL

In the following technical description, the names AN10 and AN20 will be referenced together where the interface is referred to by name and where the text applies to both the AN10 and the AN20. However, since the AN20 uses AN10 components, references to signal names and logic states documented under an AN10 assembly and which incorporate the name AN10 will not have the name AN20 optionally substituted in this text so that the references will be exactly as found in the print set and attendant documentation. The AN20 reader should nevertheless note that the text applies to the AN20 as well. (Refer to Paragraph 3.3.)

4.2 SIMPLIFIED ARPANET AND AN10/AN20 INTERFACE DESCRIPTION

Figure 1-1 illustrates a typical section of the ARPANET with AN10 and AN20 Interface Options interfacing the DECsystem-10 and DECSYSTEM-20 T-series Host computers (Packet Switching Systems) to the ARPANET Interface Message Processors (IMPs). The AN10/AN20 Interface Option supports either local [less than 9 meters (30 feet)] or distant [less than 610 meters (2000 feet)] connections to the IMP. A separate AN10/AN20 is required for each T-series Host to IMP connection.

The AN10 is packaged in an H956 DECsystem-10 style cabinet and connects directly to the external I/O bus of a T-series DECsystem-10 Host in order to provide a Host-interface to the ARPANET IMP. It is also compatible with the KA10 or K110 I/O bus.

The AN20 is packaged in a DECSYSTEM-20 style H9502 cabinet and requires a DIB20 I/O Bus Adapter mounted within the DECSYSTEM-20 cabinetry in order to integrate a DECSYSTEM-20 T-series Host to the ARPANET.

Figure 4-1 illustrates the AN10/AN20 logic assembly via a simplified block diagram. The AN10/AN20 is designed as two functional device sections (input and output) which share a common I/O interface to the Host. Each section is independently programmable for controlling message transfers.

The AN10/AN20 is a block transfer-device specifically designed to use the K110/KL10 vector and DATAO/DATAI interrupt capability (API functions 2, 4, and 5). KA10 I/O bus interrupt mode may, however, be programmably selected. It will handle I/O instruction executions in either "fast" bus or "slow" bus mode. Each transfer direction (input to the Host or output from the Host) provides separate priority interrupt channel assignments for status and data interrupts. The hardware architecture is designed such that for a given transfer direction, a data and a status interrupt cannot occur simultaneously. A data interrupt is generated for every word transferred. In K110/KL10 vector interrupt mode, however, data interrupts cycle steal from the Host CPU to move data to/from the memory location pointed to by the word count/address register without requiring software intervention.

Each device section (input and output) of the AN10/AN20 has four major registers: control/status, data, word count/address, and vector (Figure 4-1). All except the control/status register are loaded by DATAO and read by DATAI. The referenced register is controlled by register select bits in the control/status registers. Each register is described in Chapter 3.

Figure 4-1 also illustrates the partitioning of the AN10/AN20 logic blocks among the modules composing the logic assembly.

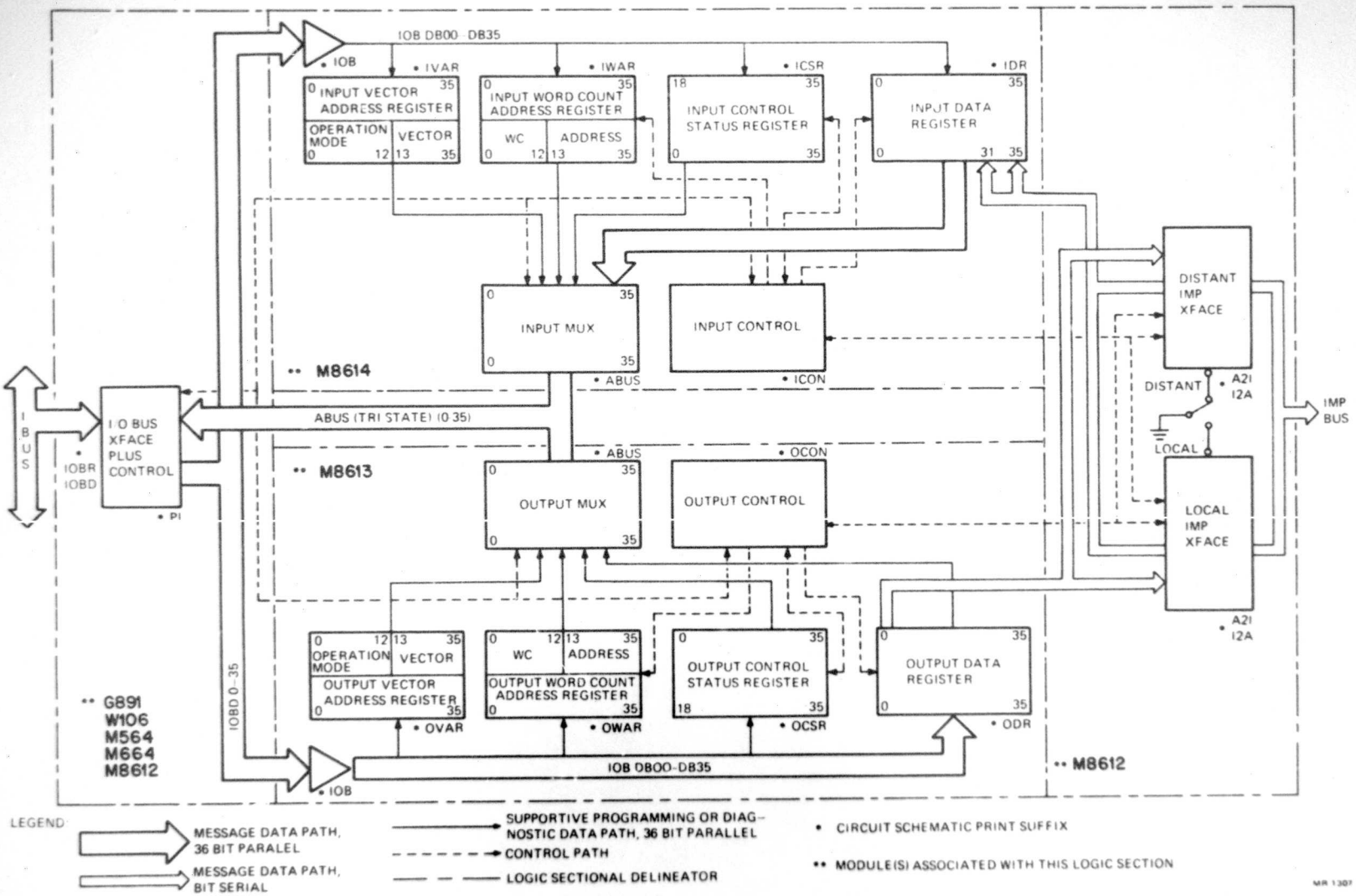


Figure 4-1 AN10/AN20 Logic Assembly Block Diagram

Note that the input section logic is primarily on one module (M8614) and the output section logic is primarily on another module (M8613) with supporting logic on other modules (M8612, G891, W106, M564, and M664). In particular, note that the M8612 module contains the I/O Bus interface control as well as the IMP Bus interface logic. The M564, M664, and W106 modules receive and drive the I/O Bus signals as required by the M8612. The G891 serves as an I/O Bus crobar module to preserve bus integrity during power up/down sequences.

Within each module partition of Figure 4-1, the engineering drawing circuit schematic prefix for each logic block element is provided for ease in identifying where the logic is located; e.g., on the M8614 module signals prefixed "ICON" are generated by logic illustrated on engineering drawing D-CS-M8614-0-ICON and signals prefixed "ICSR" are generated by logic illustrated on engineering drawing D-CS-M8614-0-ICSR. Likewise, signals prefixed "OCON" are generated by logic illustrated on engineering drawing D-CS-M8613-0-OCON and signals prefixed "OCSR" are generated by logic illustrated on engineering drawing D-CS-M8613-0-OCSR.

The I/O bus interface control logic is documented under the M8612 module with the exception of the I/O bus receivers and drivers which are documented within engineering prints D-BS-AN10-0-IOBR and D-BS-AN10-0-IOBD, respectively.

4.3 IMP DATA HANDSHAKING PROTOCOL

Data is transferred between the AN10/AN20 and the IMP with a bit serial asynchronous demand/response handshake per bit protocol. (See Section 3.3.3.) As discussed, the AN10/AN20 program can select either two-way or four-way handshaking. The handshake mode is a function of the receiver and therefore applies to the input section of the AN10/AN20 only. The difference lies in whether the receiver waits for the negation of the YOUR BIT signal before asserting READY FOR BIT, or reasserts READY FOR BIT a predetermined time after negation of READY FOR BIT. This time delay is 100 ns for a local IMP connection and 1.5 μs for a distant connection. The effect of this difference is whether two or four transitions of the handshake signals between the AN10/AN20 and the IMP are monitored. Four-way handshaking provides positive synchronization, but two-way handshaking saves considerable time over long cable connections. (Refer to Figures 3-1 and 3-2.)

A knowledge of this handshake protocol is necessary to understand the operation of the AN10/AN20 control and timing circuit. Figure 4-2 illustrates a simplified handshake control logic diagram to bridge the gap between the handshake protocol design and the actual implementation within the AN10/AN20 circuit schematics. A specific transfer direction is not indicated since the sender could be the AN10/AN20 with the receiver being the IMP, or vice versa. Regardless of the transfer direction, however, "RDY FOR BIT" is asserted by the receiver and "YOUR BIT" is asserted by the sender. Figure 4-3 represents the handshake control timing of Figure 4-2.

Before any transmission can take place, the receiver must be initialized. In the AN10/AN20 this corresponds to setting IVAR AN10 READY (IVAR bit 10). Initialization of the receiver sets the READY FOR BIT flip-flop which in turn asserts READY FOR BIT on the interconnecting cable (1, Figure 4-3). Likewise, when the sender wants to transmit data, a START MSG signal initiates the transmit control logic. This corresponds to setting OCSR BUSY (OCSR bit 26) in the AN10/AN20. The transmit control logic fetches the first message word from the sender memory and prepares the first bit for transmission. When a bit is ready, the transmit control logic sets the BIT AVAILABLE flip-flop. The coincidence of READY FOR BIT and BIT AVAILABLE enables the sender to assert YOUR BIT on the cable signifying that data is on the bus ready to be taken by the receiver (2, Figure 4-3).

Assertion of YOUR BIT activates the receiver control logic to shift in the data bit (5, Figure 4-3) and, an appropriate time delay later, to clear the READY FOR BIT flip-flop to remove READY FOR BIT from the cable to signify to the sender that the data has been received (3, Figure 4-3).

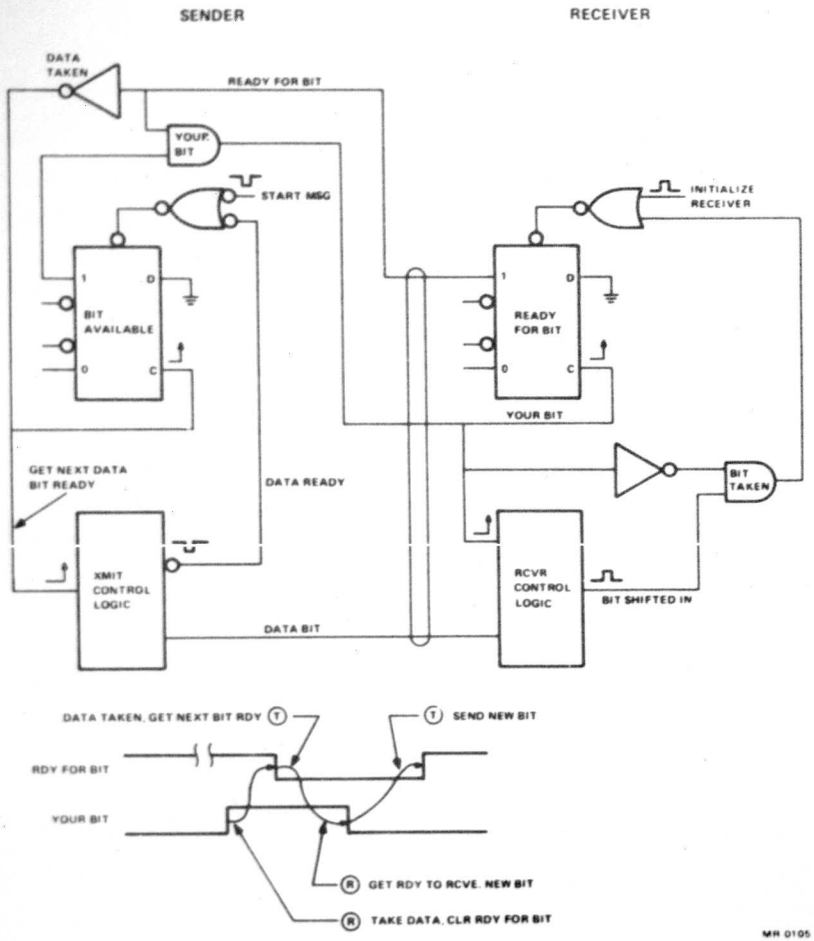


Figure 4-2 HOST-IMP Handshake Control, Simplified Logic Diagram

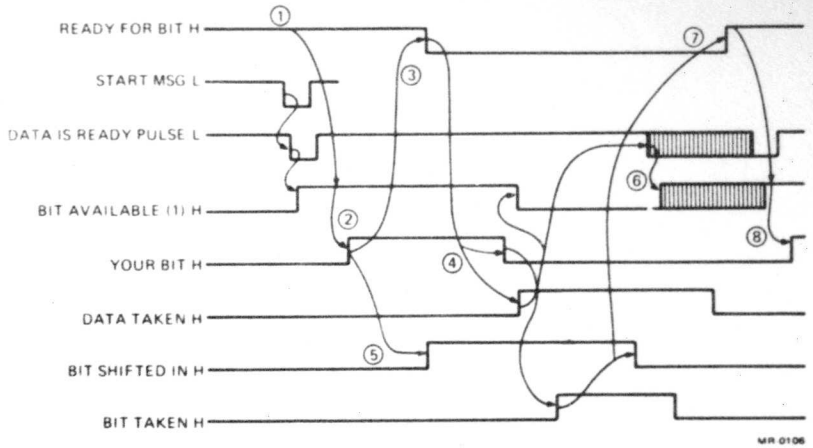


Figure 4-3 Simplified HOST-IMP Handshake Control Timing Diagram

When the sender sees the negation of READY FOR BIT, YOUR BIT is removed from the bus and DATA TAKEN is asserted (4, Figure 4-3) to clear the BIT AVAILABLE flip-flop and to activate the transmit control logic to get the next data bit ready.

The negation of YOUR BIT coincident with the data bit shifted in by the receiver, defines a BIT TAKEN condition which sets READY FOR BIT preparatory to receiving the next data bit (7, Figure 4-3). At the same time, the sender is preparing the next data bit. When the bit is ready, the DATA IS READY PULSE sets BIT AVAILABLE (6, Figure 4-3). As indicated by Figure 4-3, the time relationship between the assertion of READY FOR BIT and the setting of BIT AVAILABLE is variable The exact timing is a function of the cable length (propagation delay time), the sender and receiver circuit design, and the sender and receiver word lengths. That is, the sender may retrieve a new data word from memory on a different bit transmission than that which causes the receiver to store an assembled data word in memory. For this reason, it is imperative that DATA TAKEN clear BIT AVAILABLE so that assertion of READY FOR BIT will not give an erroneous YOUR BIT signal assertion.

Eventually, both READY FOR BIT and BIT AVAILABLE will be asserted to drive YOUR BIT on the bus for transmission of the next bit (8, Figure 4-3). This process continues until the last bit of the message is transferred.

4.4 AN10/AN20 SYSTEM FLOW DIAGRAM

The AN10/AN20 is the interface adapter designed to connect a DECsystem-10 or DECSYSTEM-20 to an ARPANET IMP. It is a hardware component in a packet-switching communications network system. As such, its operation only has meaning in the context of the system's environment within which it operates. The AN10/AN20 system flow diagram illustrated in Figure 4-4 is designed to bridge this gap between the logic schematics of the interface design and its application as it interfaces between the DECsystem-10/20 and the IMP.

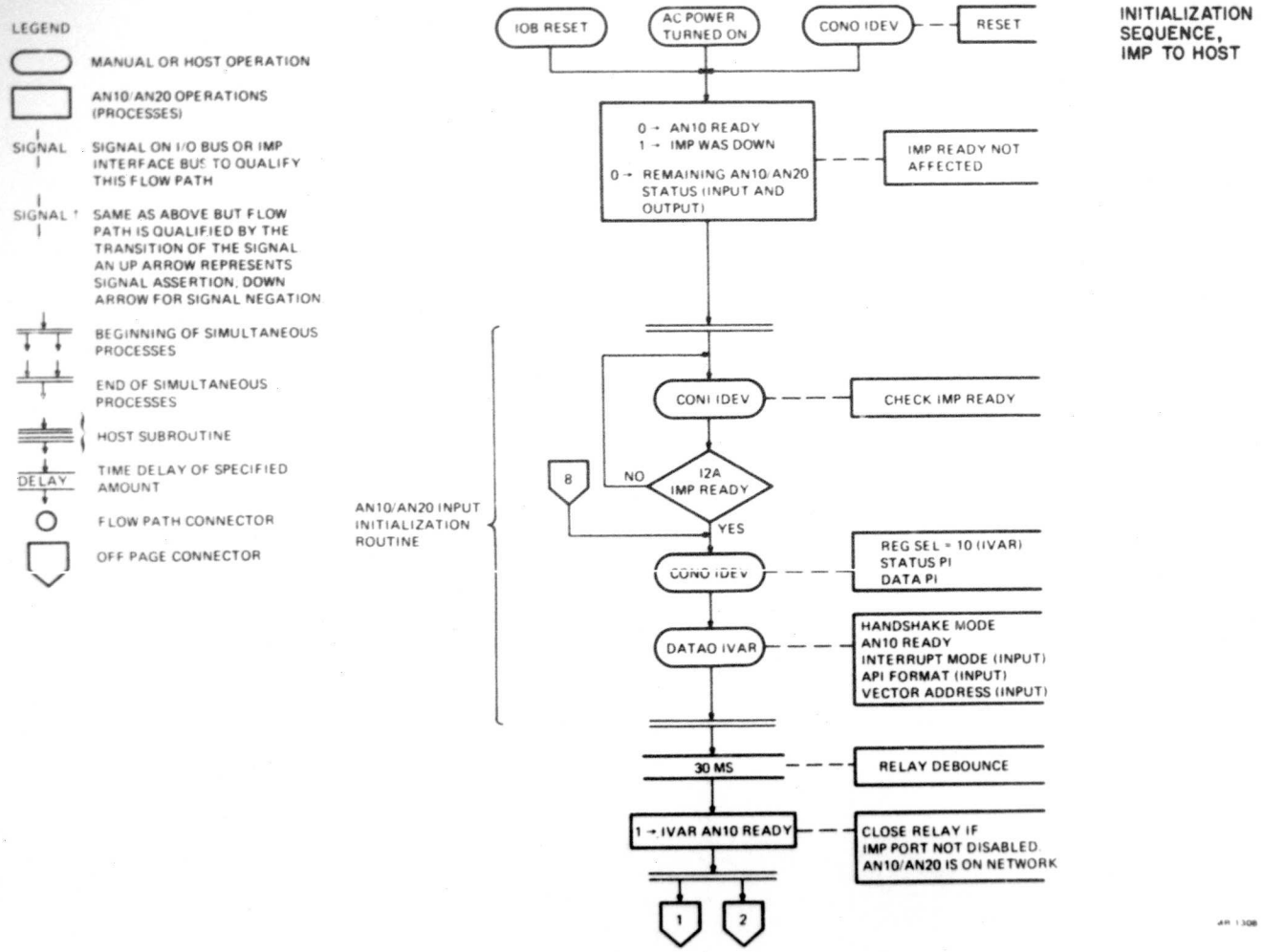


Figure 4-4 AN10/AN20 Flow Diagram (Sheet 1 of 9)

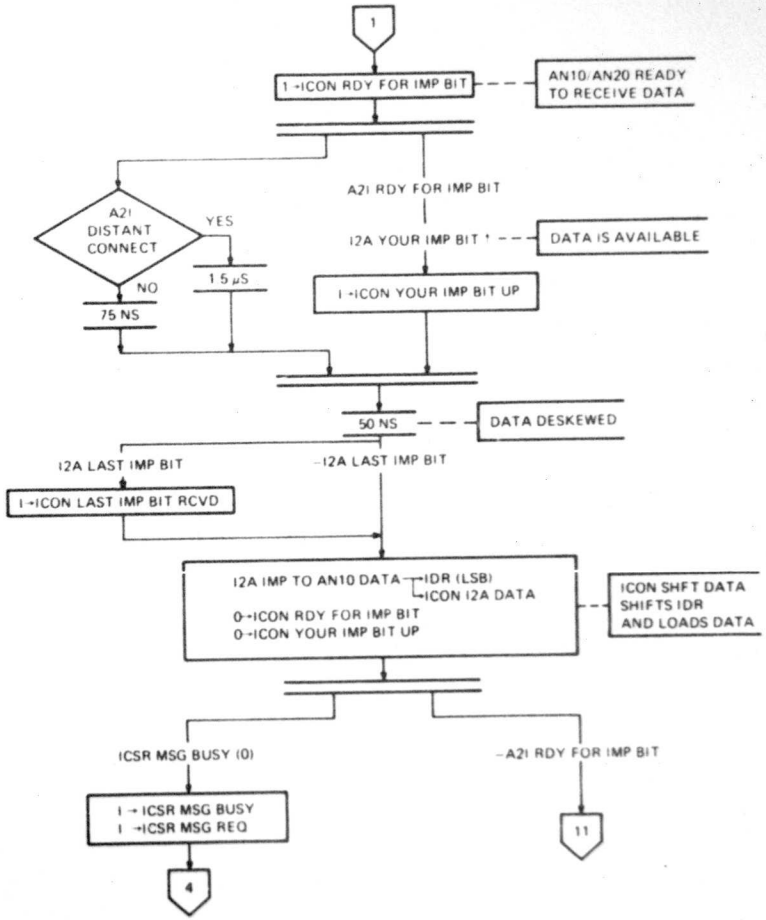


Figure 4-4 AN10/AN20 Flow Diagram (Sheet 2 of 9)

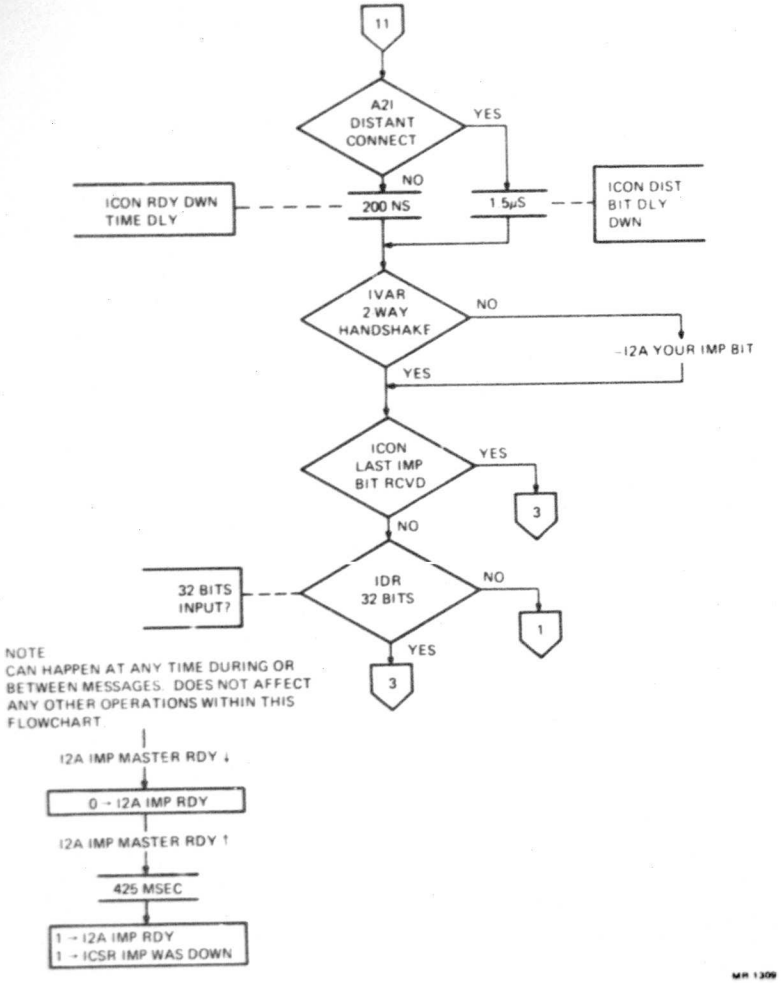


Figure 4-4 AN10/AN20 Flow Diagram (Sheet 3 of 9)

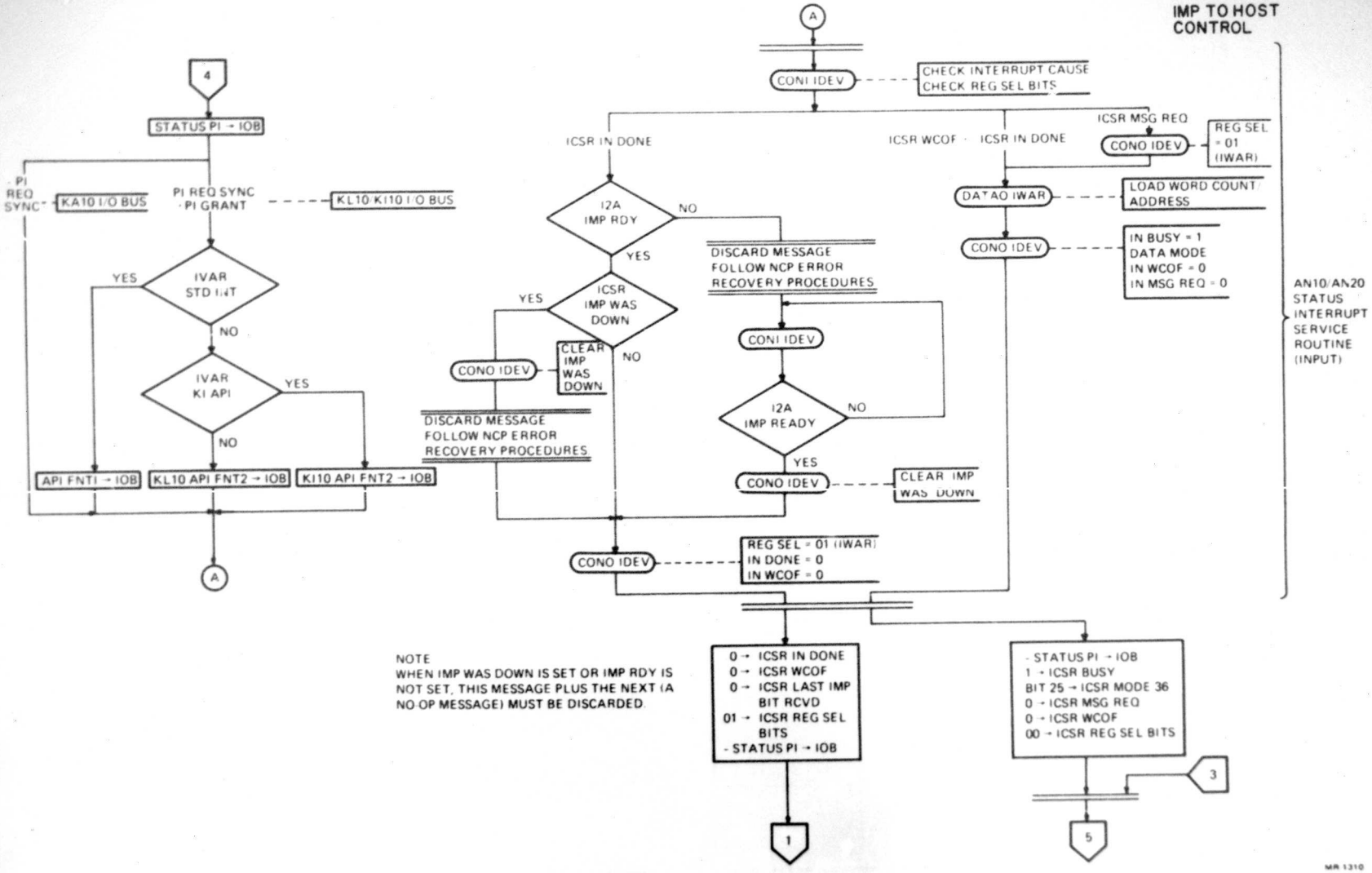


Figure 4-4 AN10/AN20 Flow Diagram (Sheet 4 of 9)

I6

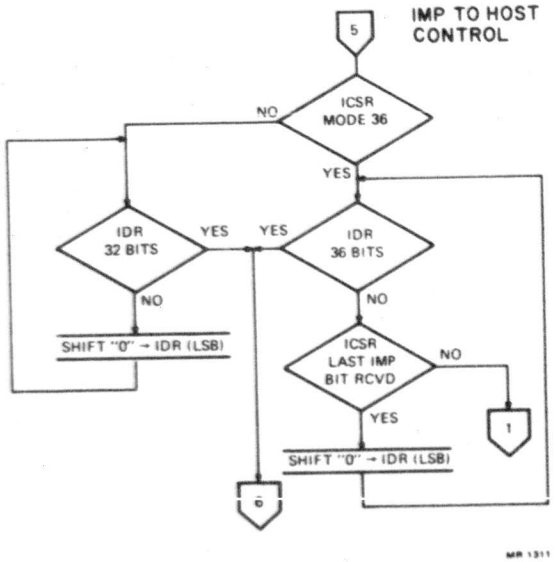


Figure 4-4 AN10/AN20 Flow Diagram (Sheet 5 of 9)

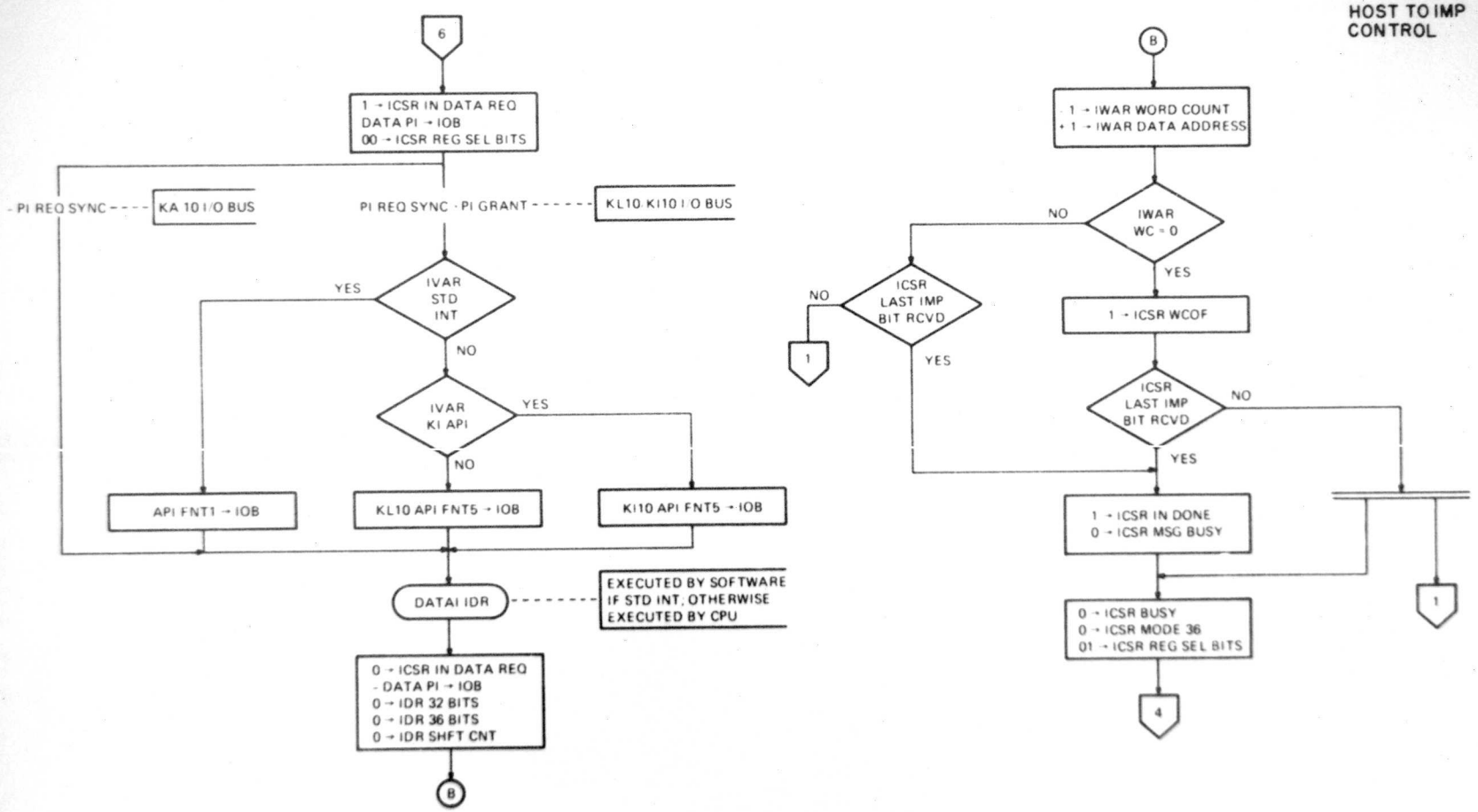


Figure 4-4 AN10/AN20 Flow Diagram (Sheet 6 of 9)

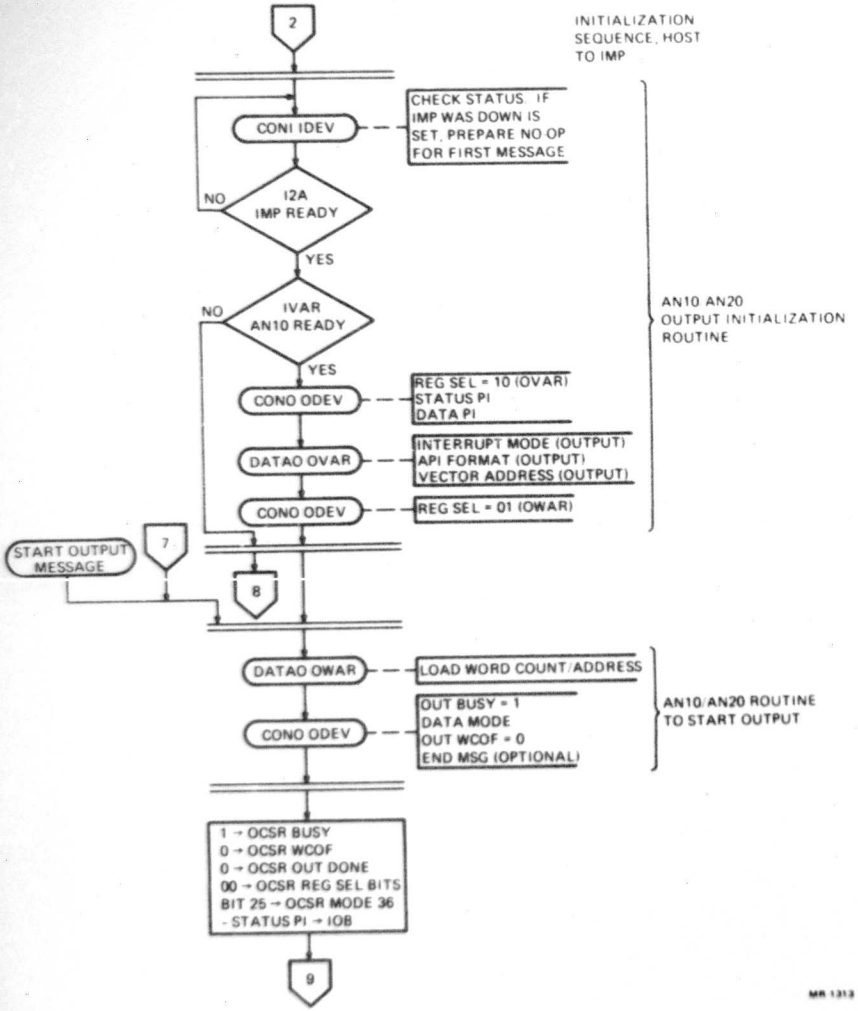


Figure 4-4 AN10/AN20 Flow Diagram **(Sheet 7 of 9)**

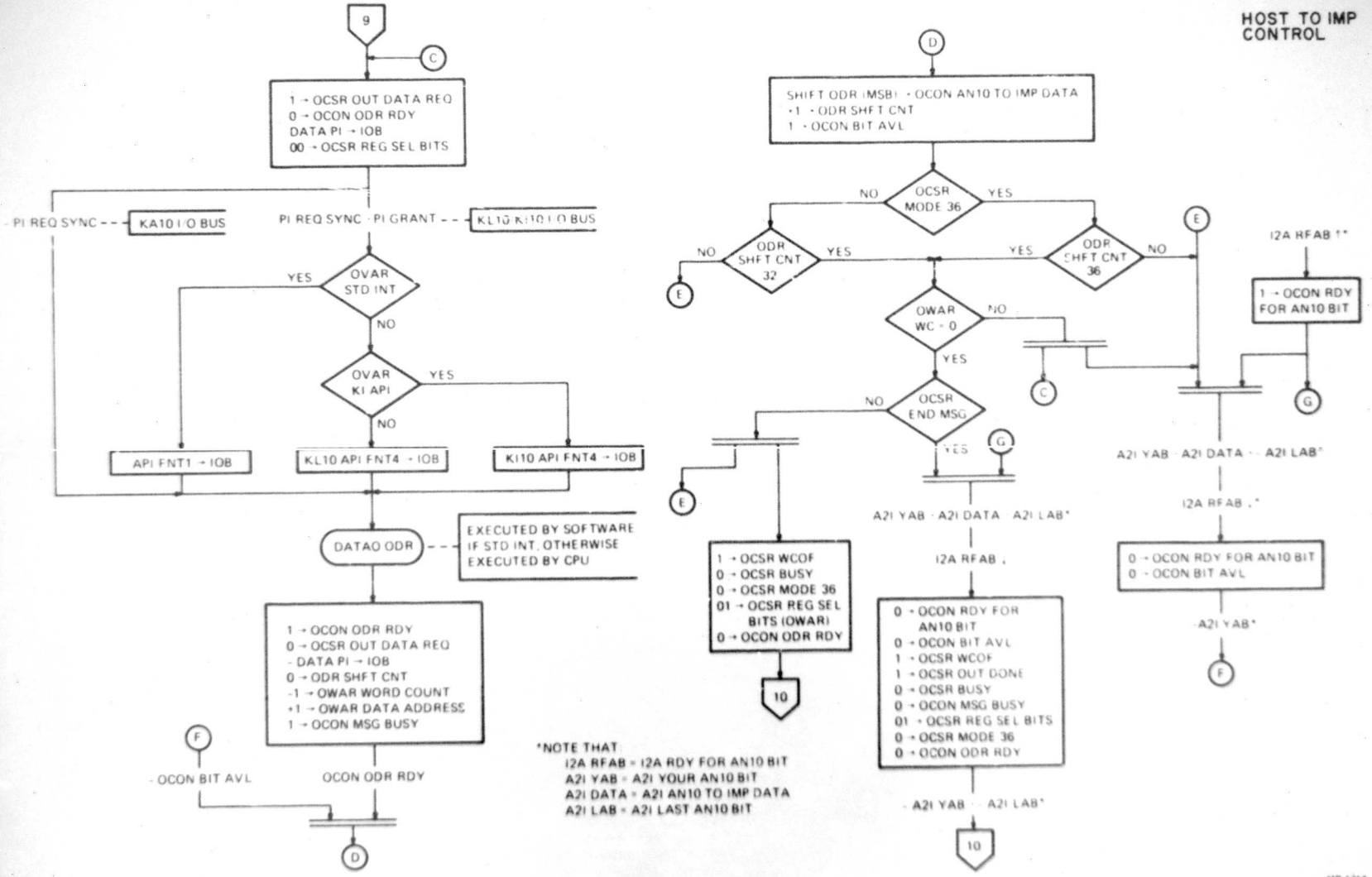


Figure 4-4 AN19/AN20 Flow Diagram (Sheet 8 of 9)

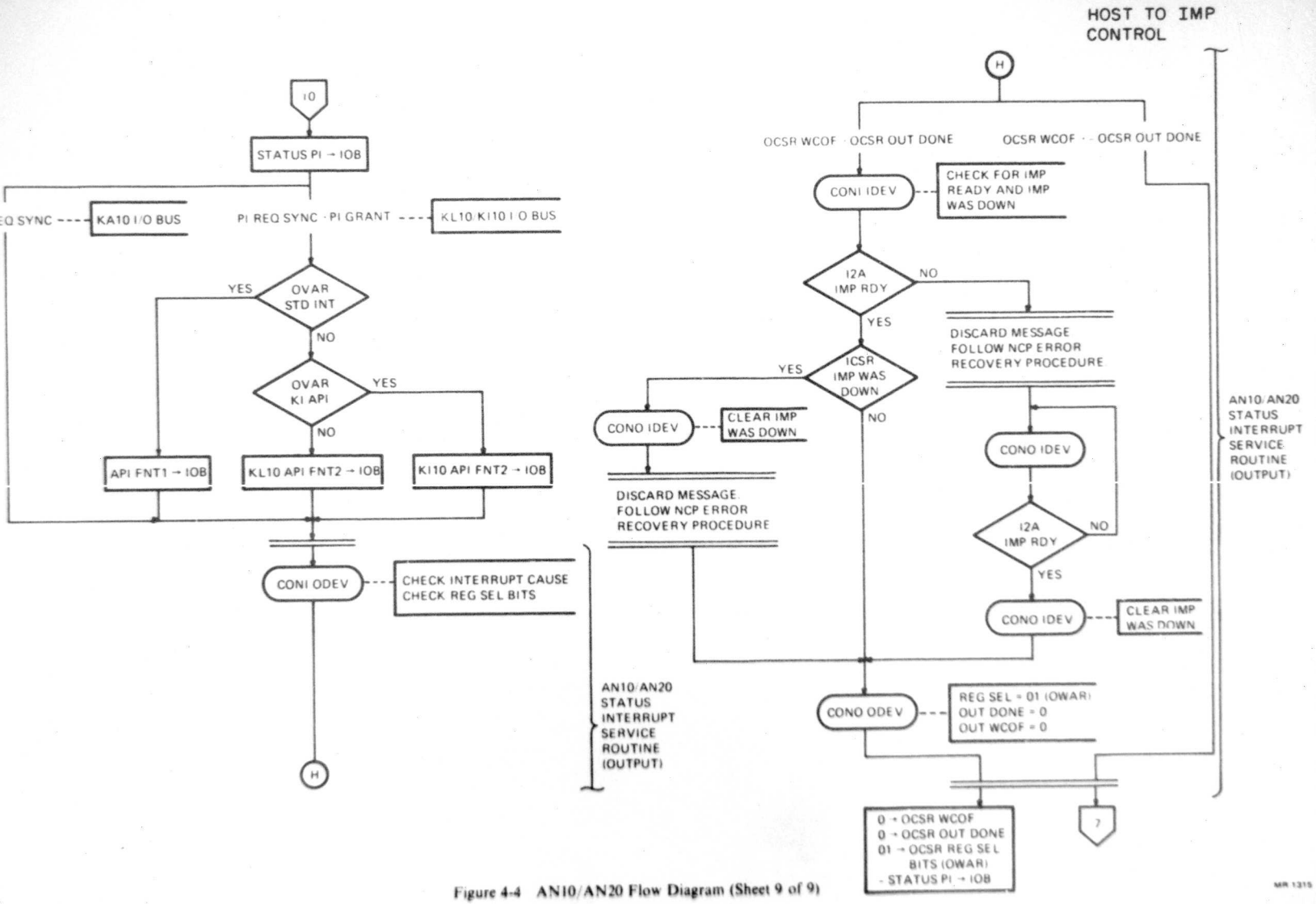


Figure 4-4 AN10/AN20 Flow Diagram (Sheet 9 of 9)

B7

The flow diagram makes no attempt to describe the network software communications and control protocol, but does illustrate how the AN10/AN20 may be programmed and the logical operations which result. Figure 4-4 is therefore a mix of DECsystem-10/20 I/O commands to the AN10/AN20, key DECsystem-10/20 I/O bus control signals, IMP interface bus control signals, and key signals and states within the AN10/AN20. The relationship between these elements and their interactions is illustrated.

The flow diagram is composed of three major divisions: initialization sequence (both input and output), host to IMP transfer control, and IMP to host transfer control. The reader may relate these latter two sections to the description in Paragraphs 4.5 and 4.6, respectively.

4.5 OUTPUT CONTROL LOGIC

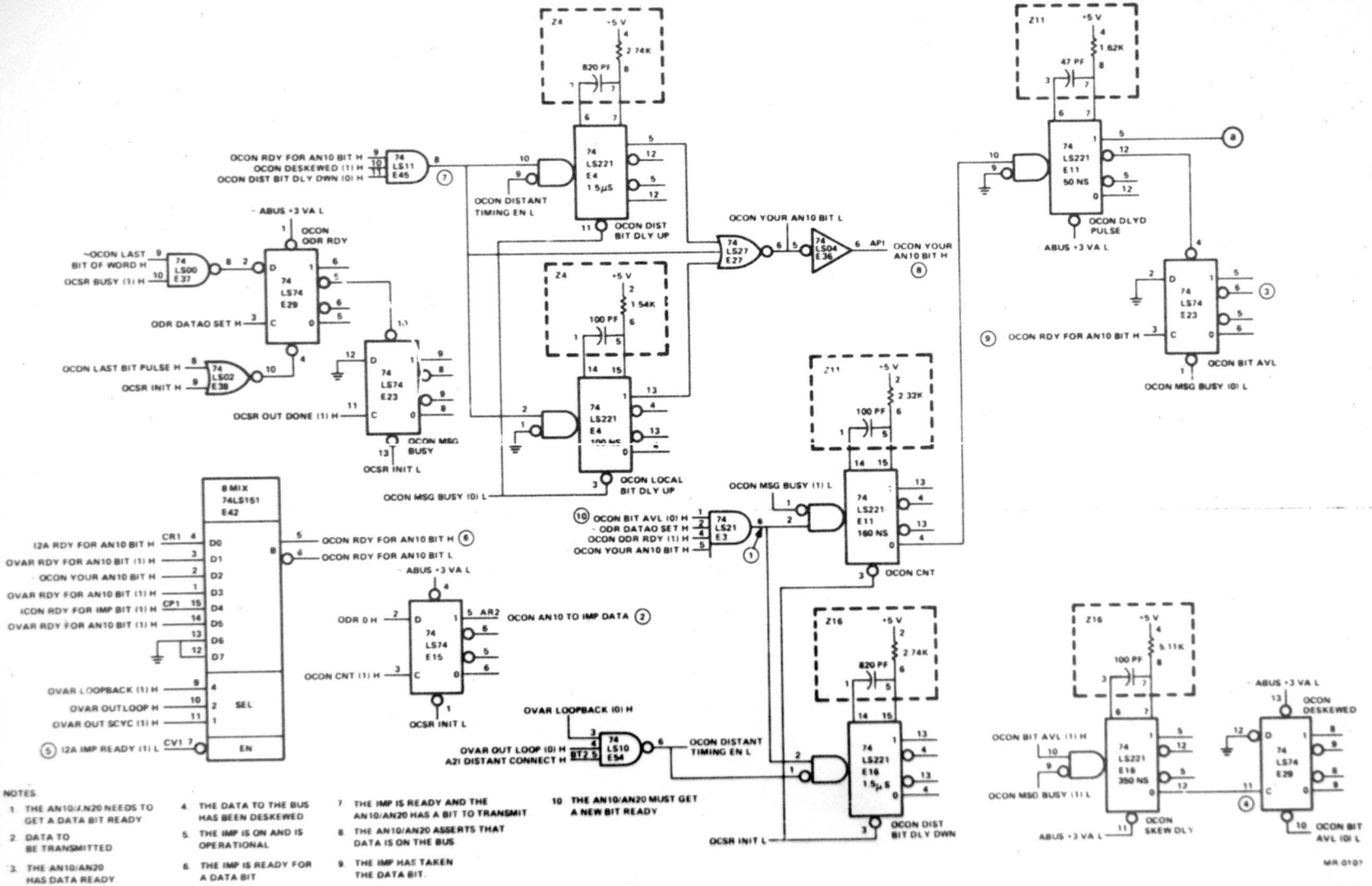
Figure 4-5 illustrates the AN10/AN20 output control logic. The key handshake control logic flow points are marked and annotated on this illustration. When the four inputs to the output control synchronization gate E3 are satisfied, the output (1, Figure 4-5) is asserted to indicate that the AN10/AN20 needs to prepare a data bit for transmission to the IMP. A 160 ns pulse, OCON CNT, is triggered. Also, if the M8612 local/distant switch is set for a distant IMP interface connection, the 1.5 μs pulse OCON DIST BIT DLY DWN will be triggered. This OCON DIST BIT DLY DWN signal is used to assure that the handshake control signal OCON YOUR AN10 BIT (8, Figure 4-5) is unasserted for at least 1.5 μs in a distant connection in order to preserve proper handshake control timing if the IMP receives data in two-way handshake mode.

OCON CNT immediately copies the most significant bit of the output data register (ODR) into the AN10/AN20 to IMP data flip-flop OCON AN10 TO IMP DATA (2, Figure 4-5) which drives the data line to the IMP. This buffering of the transmit data bit allows the AN10/AN20 to fetch a new host data word concurrent with sending the last bit of the current data word to the IMP. OCON CNT is also used to shift the ODR and to increment the ODR shift counter (see drawing D-CS-M8613-0-ODR). The shift counter keeps track of how many bits have been shifted and informs the OCON logic when 32 or 36 bits have been shifted out, depending upon the programmed data mode, to signify when the ODR is empty. When the ODR is empty, the AN10/AN20 must do one of three things.

1. Request a new host data word (WC=0)
2. Request a new buffer of the message to transmit (WC=0 but OCSR END MSG=0)
3. Inform the IMP that the bit about to be sent is the last bit of the message (WC=0 and OCSR END MSG=1). (Refer to Figure 4-5, sheet 2 of 2.)

At the end of OCON CNT, a 50 ns OCON DLYD PULSE is triggered to sample the ODR empty detection logic and to set OCON BIT AVL (3, Figure 4-5) to signify that a bit has been shifted out and is available for presentation to the IMP. If this bit is the last bit of the message, OCON LAST AN10 BIT must be set to inform the IMP that this is the last message bit. Both the AN10 TO IMP DATA and LAST AN10 BIT signals to the IMP are deskewed by OCON BIT AVL initiating a 350 ns one-shot (OCON SKEW DLY) which in turn sets OCON DESKEWED, (4, Figure 4-5).

The YOUR AN10 BIT handshake signal may now be asserted to the IMP whenever it acknowledges readiness to receive a bit. Before any data can be transferred, the IMP must be on and operational. This is signified by I2A IMP READY which conditions all incoming signals from the IMP (e.g., 5, Figure 4-5). When the IMP is on and is ready to receive an AN10/AN20 data bit, it asserts I2A RDY FOR AN10 BIT over the interconnecting cable. In on-line operation, this signal is then gated through the 8 X 1 multiplexer to assert OCON RDY FOR AN10 BIT (6, Figure 4-5).



NOTES:

1. THE AN10/AN20 NEEDS TO GET A DATA BIT READY
2. DATA TO BE TRANSMITTED
3. THE AN10/AN20 HAS DATA READY
4. THE DATA TO THE BUS HAS BEEN DESKEWED
5. THE IMP IS ON AND IS OPERATIONAL
6. THE IMP IS READY FOR A DATA BIT
7. THE IMP IS READY AND THE AN10/AN20 HAS A BIT TO TRANSMIT
8. THE AN10/AN20 ASSERTS THAT DATA IS ON THE BUS
9. THE IMP HAS TAKEN THE DATA BIT.
10. THE AN10/AN20 MUST GET A NEW BIT READY

Figure 4-5 AN10/AN20 Output Control, Logic Diagram (Sheet 1 of 2)

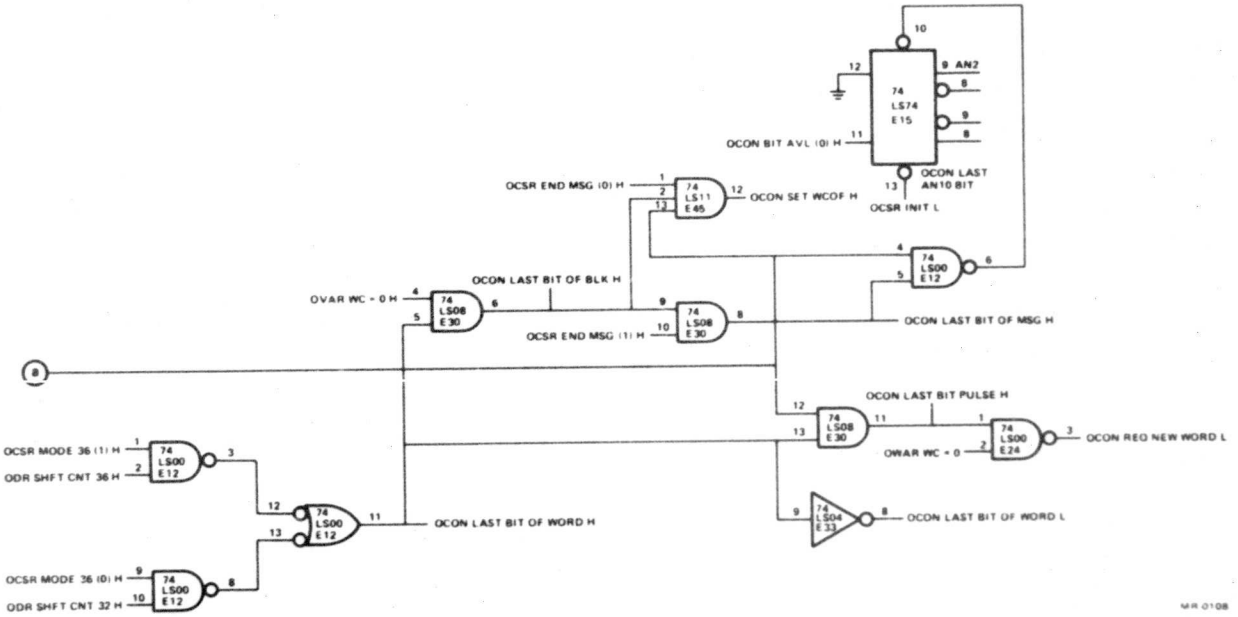


Figure 4-5 AN10/AN20 Output Control, Logic Diagram (Sheet 2 of 2)

The three-input AND gate at 7, Figure 4-5 synchronizes the conditions prerequisite to the AN10/AN20 asserting OCON YOUR AN10 BIT (8, Figure 4-5) which drives the signal to the IMP declaring that a data bit is available to be read. To summarize, these conditions are as follows.

1. The IMP is ready to receive a bit.
2. The AN10/AN20 has provided ample data/control signal deskew time.
3. OCON YOUR AN10 BIT has been unasserted a minimum of 1.5 μs if the AN10/AN20 has been selected for a distant connection.

Just as OCON YOUR AN10 BIT must be unasserted a minimum specified time in order to maintain proper synchronization with the IMP, so also must it be asserted a minimum specified time; 100 ns for a local connection and 1.5 μs for a distant connection. The one-shots triggered by the signal at 7, Figure 4-5 guarantee this timing specification. Of course, OCON YOUR AN10 BIT must also remain asserted at least until the IMP acknowledges receipt of the data bit by dropping OCON RDY FOR AN10 BIT. Therefore, OCON YOUR AN10 BIT remains asserted until the one shot(s) time out or the IMP acknowledges taking the data bit, whichever occurs last.

As the IMP drops OCON RDY FOR AN10 BIT to acknowledge data receipt, OCON BIT AVL is cleared (9, Figure 4-5). When OCON BIT AVL clears and the OCON LOCAL/DIST BIT DLY UP one-shots have timed out, the AN10/AN20 responds by dropping OCON YOUR AN10 BIT. These conditions synchronize at 10, Figure 4-5 whether or not more data is in the ODR (OCON ODR RDY). When more data is available in the ODR, the E3 synchronizing AND gate output signal (1, Figure 4-5) is asserted and the above data handshake/control sequence repeats.

4.5.1 1-of-8 Multiplexer Generation of OCON RDY FOR AN10 BIT Signal

The purpose of the 1-of-8 multiplexer E42 is to generate the OCON RDY FOR AN10 BIT signal used during normal operation of the AN10/AN20 as well as during diagnostic testing. During normal operation, SEL inputs 1, 2, and 4 will be logical lows and the READY FOR AN10 BIT signal, originally generated by the IMP and regenerated within the AN10/AN20 as I2A RDY FOR AN10 BIT H (6, Figure 4-5), will be selected as the source for OCON RDY FOR AN10 BIT. During maintenance testing, SEL inputs 1, 2, and 4 will be asserted high as indicated on drawing D-CS-M8613-0-OCON. Table 3-2 is a decode chart for the selection of the READY FOR AN10 BIT source signal. The only qualifying factor common to all inputs is ENable, I2A IMP READY (1) L, (5, Figure 4-5). Use of the multiplexer permits programmable loop back and single cycle handshake diagnosis of the AN10/AN20 output control logic without having to physically disconnect the IMP cable. All but the IMP cable drivers and receivers may be tested in this manner.

4.5.2 OCON LAST AN10 BIT Flip-Flop

OCON LAST AN10 BIT flip-flop E15 is set in conjunction with the last data bit of a message being sent to the IMP and remains set until the OCON BIT AVL flip-flop is cleared. This clearing of OCON LAST AN10 BIT sets the OCSR OUT DONE and OCSR WCOF flip-flops (see drawing D-CS-M8613-0-OCSR) to terminate the AN10/AN20. The setting of OCSR OUT DONE clears both OCSR BUSY and OCON MSG BUSY. A status interrupt sequence is then initiated over the assigned PI channel via OCSR STAT INT which enables PI STAT OUT INT (see D-CS-M8612-0-PI). The clearing of OCSR BUSY alters the OCSR RA1/RA2 register selection flip-flops to point to the OWAR in anticipation of the loading of the word count/data address of the first buffer of the next message to be sent.

4.5.3 Host Word Request Logic

Except for the case of the transfer of the last bit of the message, the AN10/AN20 requests a new host word concurrent with the transmission to the IMP of the last bit of the current host word. The ODR shift count is ANDed with the programmed data mode to produce the signal OCON LAST BIT OF WORD indicating an empty output data register (ODR). If the word count has *not* expired, OCON REQ NEW WORD is generated by OCON DLYD PULSE to direct set OCSR OUT DATA REQ. This in turn initiates a data request interrupt over the assigned PI channel for fetch of a new host word by setting the PI DATAO REQ flip-flop (see drawing D-CS-M8612-0-PI).

Should the word count have expired (OWAR WC=0) at the time OCON LAST BIT OF WORD is detected, and providing OCSR END MSG is not specified, OCON DLYD PULSE will generate the strobe OCON SET WCOF to direct set OCSR WCOF. OCSR BUSY is in turn cleared, but in this case OCSR OUT DONE and OCON MSG BUSY *are not* cleared. This signifies that the AN10/AN20 has completed transferring the current buffer of the current message and that the next buffer of the message needs to be selected for transmission. OCSR WCOF generates OCSR STAT INT to initiate the PI ENA STAT OUT INT status interrupt request sequence over the assigned PI channel (see D-CS-M8612-0-PI). The clearing of OCSR BUSY alters the OCSR RA1/RA2 register selection flip-flop to point to the OWAR in anticipation of the programmable loading of the word count/data address of the next buffer of the message.

Setting OCSR BUSY by CONO in conjunction with the data mode and END MSG as appropriate will continue the AN10/AN20 operation. OCSR BUSY sets OCSR OUT DATA REQ to initiate a data request interrupt for the first word of the new buffer.

4.6 INPUT CONTROL LOGIC

Figure 4-6 illustrates the AN10/AN20 input control logic. The important points marking the handshake control logic flow are annotated on this illustration. In order to communicate with the IMP, the IVAR AN10 READY flip-flop must be set (IVAR bit 10). This causes the AN10/AN20's READY relay to close, looping back to the IMP the AN10 MASTER READY signal. In this manner, the IMP is informed of the AN10/AN20's operational readiness. Setting IVAR AN10 READY also provides the initial clock of the ICON RDY FOR IMP BIT flip-flop (1, Figure 4-6, sheet 2 of 2). The asserted output of ICON RDY FOR IMP BIT enables the RDY FOR IMP BIT line driver (D-CS-M8612-0-A2I) to indicate that the AN10/AN20 is ready to receive a data bit from the IMP.

To properly synchronize with the IMP, especially in two-way data handshake mode, RDY FOR IMP BIT must remain asserted a guaranteed minimum time. The ICON LOCAL/DIST BIT DLY UP one-shots preserve this minimum timing for the switch-selectable local or distant IMP interface connection, respectively. When the appropriate one-shot time out expires (local or distant), ICON RDY UP DLY OVER is clocked *on* (5, Figure 4-6, sheet 1 of 2).

The I2A IMP READY signal (2, Figure 4-6, sheet 1 of 2) indicates that the IMP is on-line and is operational and enables the ICON YOUR IMP BIT, OCON LAST IMP BIT, and ICON IMP TO AN10 DATA signal selection multiplexers. When a data bit is ready for sending to the AN10/AN20, the IMP responds to RDY FOR IMP BIT by asserting YOUR IMP BIT and IMP TO AN10 DATA on the interconnecting AN10/AN20-IMP cable. These signals are received as I2A YOUR IMP BIT and I2A IMP TO AN10 DATA, and are gated through the enabled signal selection multiplexers as ICON YOUR IMP BIT and ICON IMP TO AN10 DATA, respectively (3, Figure 4-6, sheet 1 of 2).

Timing between the two data handshake signals ICON RDY FOR IMP BIT and ICON YOUR IMP BIT is asynchronous. The exact relationship and time duration is a function of many variables such as the selected interface connection (local or distant), data handshake mode (two-way or four-way), word length size differences between the host and the IMP, and the cable length. For example, in two-way handshake mode it is highly possible that the AN10/AN20 will reassert ICON RDY FOR IMP BIT

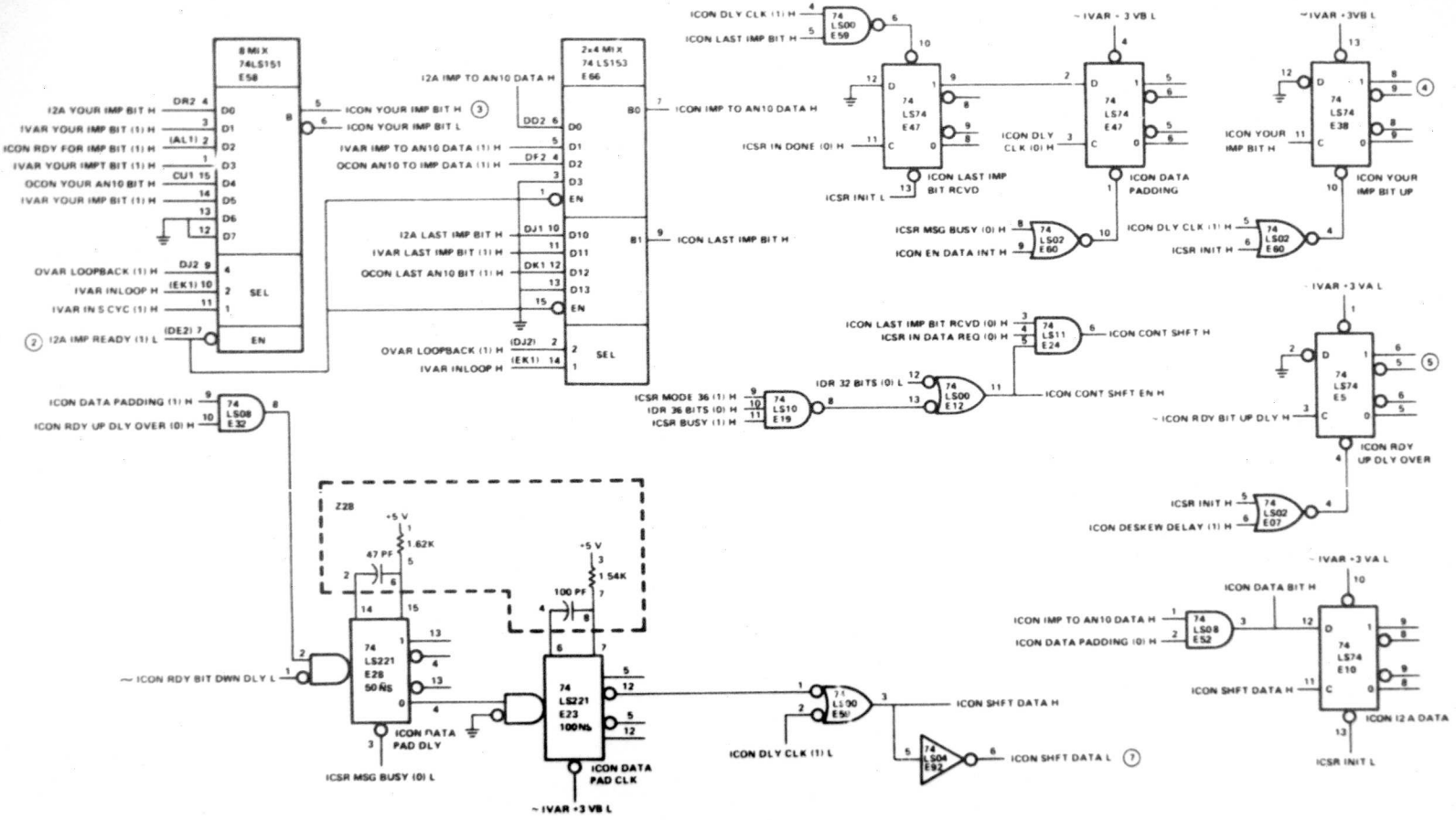
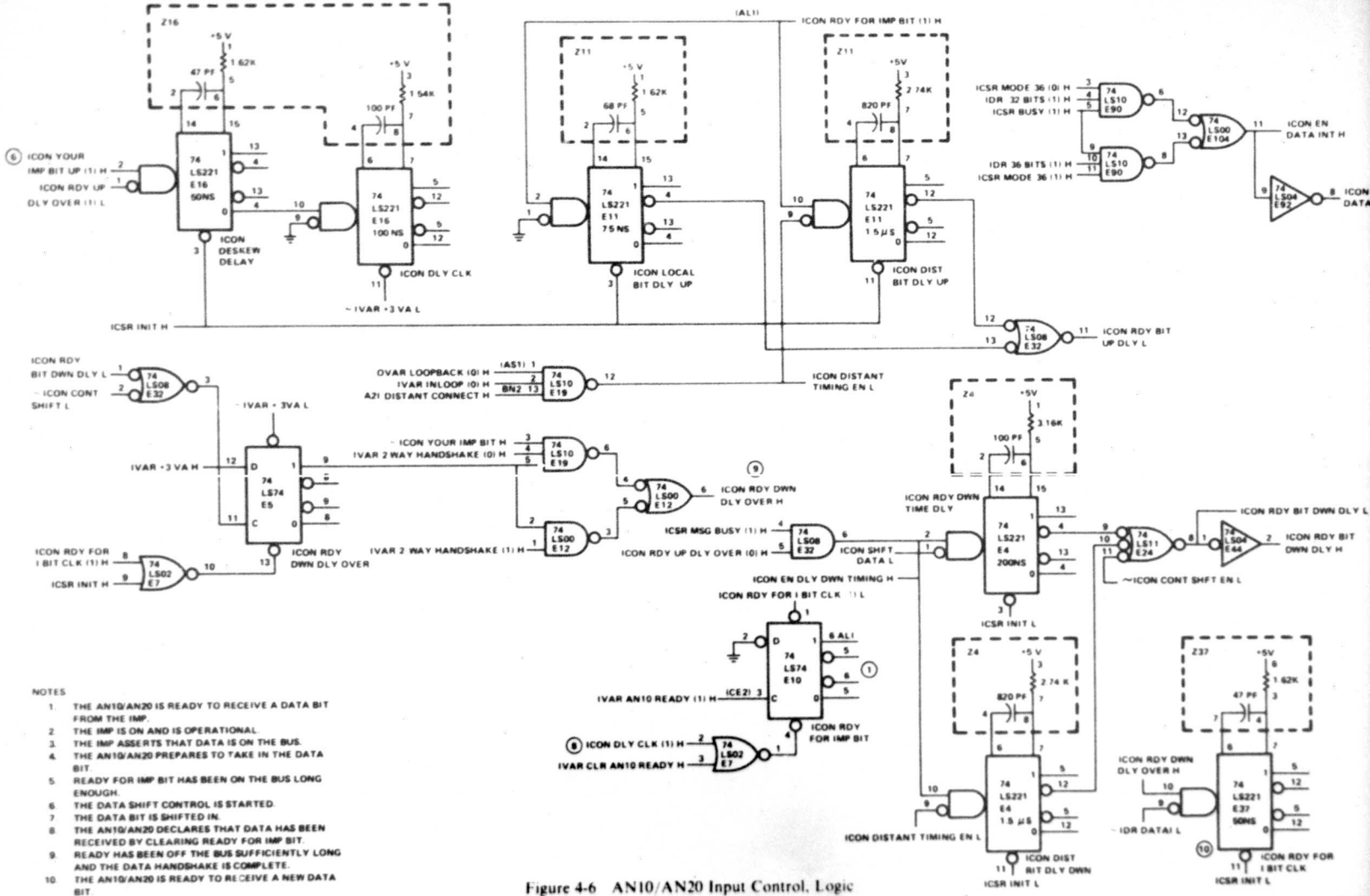


Figure 4-6 AN10/AN20 Input Control, Logic Diagram (Sheet 1 of 2)



NOTES

1. THE AN10/AN20 IS READY TO RECEIVE A DATA BIT FROM THE IMP.
2. THE IMP IS ON AND IS OPERATIONAL.
3. THE IMP ASSERTS THAT DATA IS ON THE BUS.
4. THE AN10/AN20 PREPARES TO TAKE IN THE DATA BIT.
5. READY FOR IMP BIT HAS BEEN ON THE BUS LONG ENOUGH.
6. THE DATA SHIFT CONTROL IS STARTED.
7. THE DATA BIT IS SHIFTED IN.
8. THE AN10/AN20 DECLARES THAT DATA HAS BEEN RECEIVED BY CLEARING READY FOR IMP BIT.
9. READY HAS BEEN OFF THE BUS SUFFICIENTLY LONG AND THE DATA HANDSHAKE IS COMPLETE.
10. THE AN10/AN20 IS READY TO RECEIVE A NEW DATA BIT.

Figure 4-6 AN10/AN20 Input Control, Logic Diagram (Sheet 2 of 2)

preparatory to receiving the next data bit before the IMP's negation of YOUR IMP BIT will have had time to propagate along the cable and through the ICON YOUR IMP BIT signal multiplexer. In fact, ICON RDY UP DLY OVER may even be set before the negation of YOUR IMP BIT is seen by the AN10/AN20. For this reason, the AN10/AN20 synchronizes with the rising edge of ICON YOUR IMP BIT rather than with the dc signal level. The leading edge is latched by the ICON YOUR IMP BIT UP flip-flop (4, Figure 4-6, sheet 1 of 2).

The ICON DESKEW DELAY one-shot (6, Figure 4-6, sheet 2 of 2) synchronizes the above handshake signal timing necessary for the reading of a data bit from the IMP. Once this one-shot triggers, a sequence of events is initiated to shift the data bit into the input data register and to acknowledge receipt of the data by dropping the RDY FOR IMP BIT signal. Key to this operation is ICON DLY CLK which triggers following the 50 ns data deskew.

ICON DLY CLK forms one of the two OR conditions which asserts ICON SHFT DATA (7, Figure 4-6, sheet 1 of 2), the term used to shift the input data register (IDR) and to increment the IDR shift counter (refer to D-CS-M8614-0-IDR). Data is shifted into bit 31 of the IDR until all 32 bit positions are filled. Then, if 36-bit mode is selected, the next four bits are shifted into IDR bits 32-35. The shift counter is used in conjunction with the data mode to indicate when the IDR is full. Concurrent with this, ICON DLY CLK clears ICON RDY FOR IMP BIT to acknowledge that the data has been received (8, Figure 4-6, sheet 2 of 2).

In addition to the above, ICON SHFT DATA stores a copy of the received data bit in ICON I2A DATA, and initiates the one-shot timing guaranteeing that ICON RDY FOR IMP BIT is turned off a sufficiently long time. Furthermore, the AN10/AN20 cannot reassert ICON RDY FOR IMP BIT until it is able to receive the next data bit. The ICON RDY DWN TIME DLY one-shot therefore serves the dual purpose of assuring a minimum off-time of this signal for a local interface connection, as well as providing sufficient time for (1) incrementing the IDR shift counter to determine whether or not the IDR is full and (2) determining if the *last* IMP bit was just received. The negated state of ICON CONT SHFT EN and ICON CONT SHIFT is used to indefinitely extend the delay initiated by the one shot(s) should one of the above conditions be detected, requiring extension of the time before the AN10/AN20 is ready to receive a new bit. The ICON DIST BIT DLY DWN one-shot is only used to guarantee a minimum distant connection off time of ICON RDY FOR IMP BIT.

Once all the internal delay conditions are satisfied, ICON RDY DWN DLY OVER (1) H is set. This flip-flop output is then checked against the data handshake mode selected by the program to determine whether or not the AN10/AN20 must wait for the IMP's negation of ICON YOUR IMP BIT before producing the signal ICON RDY DWN DLY OVER H (9, Figure 4-6, sheet 2 of 2). This latter signal triggers the ICON RDY FOR I BIT CLK one-shot (10, Figure 4-6, sheet 2 of 2) which provides the signal pulse to directly set ICON RDY FOR IMP BIT. With ICON RDY FOR IMP BIT set, the AN10/AN20 declares that it is ready to receive the next data bit. This bit-by-bit handshake sequence continues until the last bit of the message is received.

4.6.1 Input Signal Selector Multiplexers

The three input signals from the IMP required for the AN10/AN20 to receive data are routed through signal selection multiplexers, one for each of the signals I2A YOUR IMP BIT, I2A IMP TO AN10 DATA, and I2A LAST IMP BIT. Use of the multiplexers facilitates implementation of the various programmable loopback and single cycle handshake control diagnostic features of the AN10/AN20. In this manner, the input control logic may be exercised and diagnosed by providing diagnostic signals to simulate the IMP's response. Without physically disconnecting the AN10/AN20-IMP cable, all but the cable drivers and receivers may be tested. During normal operation, port 0 of each multiplexer is selected to route the IMP cable signals through to the input control logic. All other input ports are used for diagnostic purposes.

4.6.2 Input Message Start Up

Upon receipt of the first bit of a message, the AN10/AN20 sets ICSR MSG BUSY. This flip-flop stays set for the entire message transmission. Its use distinguishes the first bit of a message from the first bit of a newly assigned input buffer space for a message already in progress (see drawing D-CS-M8614-0-ICSR). ICSR MSG BUSY in turn sets ICSR MSG REQ to initiate a status interrupt to the host, informing the host that the IMP is currently sending a message and that the AN10/AN20 needs an input buffer assignment and data format specification in order to transfer the message to the host memory. The AN10/AN20 will continue to receive bits from the IMP until a count of 32 bits in the IDR is reached, at which time ICON CONT SHFT EN will be dropped, disabling ICON CONT SHFT, and thereby suspending data handshaking with the IMP as described in Paragraph 4.6. Refer also to Figure 4-6. This allows host software 31-bit times to respond to the IN MSG REQuest interrupt before the AN10/AN20 will impose a handshake delay to the IMP.

After Host software has loaded the first input buffer allocation pointer into the IWAR (word count plus data address), a CONO must be executed to the ICSR to clear IN MSG REQ (bit 27) and to set IN BUSY (bit 26). The data format mode (bit 25) must also be specified. With IN BUSY set and 32-bit mode selected (ICSR MODE 36=0), the AN10/AN20 will assert ICON EN DATA INT (Figure 4-6, sheet 2 of 2) as soon as 32 bits are assembled in the IDR. This sets ICSR IN DATA REQ (D-CS-M8614-0-ICSR) to initiate a data interrupt request sequence over the assigned PI channel. The DATAI executed in response to this interrupt, either hardware executed under API function type 5 control or software executed, increments the IWAR data address pointer, decrements the IWAR word count, and clears the IDR shift counter (D-CS-M8614-0-IDR) as well as the interrupt request flip-flop ICSR IN DATA REQ. With the IDR count initialized, ICON EN DATA INT is dropped and ICON CONT SHFT EN is again asserted to continue AN10/AN20 data handshaking with the IMP. Refer to Paragraph 4.5 for further discussion on how this handshake process is handled.

In the case of 36-bit mode data transfers, the AN10/AN20 may temporarily suspend handshaking with the IMP if the first 32 bits of the first word of the current message buffer are gathered before ICSR BUSY is set. However, as soon as ICSR MODE 36 and ICSR BUSY are set, ICON CONT SHFT will be reenabled and the remaining bits gathered to fill all 36 bits of the IDR. At this time, ICON CONT SHFT EN will be dropped to suspend data handshaking while the assembled word is being transferred to the host memory. ICON EN DATA INT (Figure 4-6, sheet 2 of 2) will be asserted and a data interrupt sequence executed as described above.

4.6.3 Input Message Termination

An input message transfer, once started, continues until the IMP asserts ICON LAST IMP BIT concurrent with the last data bit being transferred. This may require one or more input buffer allocations before the message is complete. As discussed previously, the DATAI executed (either under hardware or software control) decrements the IWAR word count (D-CS-M8614-0-IWAR). When the word count decrements to zero, IWAR WC=0 is asserted to set ICSR WCOF (D-CS-M8614-0-ICSR). This asserts one of the three OR conditions composing ICSR STAT INT. A word count overflow input status interrupt is thereby posted to the host CPU over the assigned PI channel. The setting of ICSR WCOF also clears ICSR BUSY. Note, however, that ICSR MSG BUSY is not cleared. That is, ICSR BUSY delineates the portion of the input message stream allocated to the currently assigned message buffer space in host memory whereas ICSR MSG BUSY delineates the entire input message bit stream.

The clearing of ICSR BUSY alters the ICSR RA1/RA2 register selection flip-flops (D-CS-M8614-0-ICSR) to point to the IWAR in anticipation of the programmable loading of a new word count/data address in the IWAR for the next buffer allocation of the input message stream. Note that the setting of ICSR WCOF and the clearing of ICSR BUSY does not directly couple to the data handshake control logic described in Paragraph 4.6. The AN10/AN20 will therefore continue receiving bits from

the IMP until 32 bits are left-justified and assembled in the IDR. If the host software has not responded within 32-bit times of the word count overflow interrupt by executing a DATAO load of a new IWAR word count and address and a CONO to the ICSR to set ICSR BUSY and to select the data format mode for the assigned buffer allocation, then the AN10/AN20 will temporarily suspend handshaking with the IMP until this is done. The suspension of data handshaking is accomplished by disabling ICON CONT SHFT EN and ICON CONT SHFT as described in Paragraph 4.6. Refer also to Figure 4-6, sheet 1 of 2.

Reception of the input message stream will continue as described above until ICON LAST IMP BIT is received. At the time ICON DLY CLK is generated to produce ICON SHFT DATA (7, Figure 4-6) for shifting this last data bit into the IDR and incrementing the IDR shift counter, ICON LAST IMP BIT RCVD is set (Figure 4-6, sheet 1 of 2). The 100 ns pulse width of ICON DLY CLK is sufficient to allow the IDR counter to increment and stabilize before determining whether or not this last message bit filled the IDR. If the IDR is not completely filled, the AN10/AN20 must zero-fill the remaining bit locations before transferring the last message word to the host memory. This is referred to as AN10/AN20 padding. To do this, the trailing edge of the ICON DLY CLK copies the asserted ICON LAST IMP BIT RCVD output to the ICON DATA PADDING flip-flop (Figure 4-6, sheet 1 of 2). This then provides the enable signal level to the ICON DATA PAD DLY one-shot.

At the time the last data bit is received, ICON RDY UP DLY OVER is cleared. This triggers ICON DIST BIT DLY DWN, if distant timing is enabled, and enables triggering of ICON RDY DWN TIME DLY by ICON SHFT DATA (Figure 4-6, sheet 2 of 2). Unless the IDR is filled (indicated by dropping ICON CONT SHFT EN), ICON RDY BIT DWN DLY will be negated upon the time-out of the(se) triggered one-shot(s). This then triggers the enabled ICON DATA PAD DLY one-shot. ICON DATA PAD CLK is triggered 50 ns later to provide the ICON SHIFT DATA clock (7, Figure 4-6) necessary to shift the first pad bit into the IDR and increment the count. A zero will be shifted because ICON DATA PADDING disables the ICON IMP TO AN10 DATA signal, forcing ICON DATA BIT low (Figure 4-6, sheet 1 of 2). ICON SHFT DATA then retriggers ICON RDY DWN TIME DLY. At the end of this 200 ns pulse, ICON RDY BIT DWN DLY is again negated to trigger ICON DATA PAD DLY for initiation of another data padding shift. This padding process continues until the IDR is filled per the data mode currently selected. When the IDR is full, ICON CONT SHFT EN will be dropped to prevent further triggering of the data padding circuitry. Note that even if distant interface timing is enabled, this data padding will take place under internally controlled AN10/AN20 timing of nominally 350 ns per pad bit shifted into the IDR.

With the IDR full, a data interrupt request sequence is initiated as discussed in previous paragraphs. At the completion of the DATAI transfer of the assembled word to host memory, ICSR IN DONE is set (D-CS-M8614-0-ICSR). An input status interrupt sequence follows to inform the host of the completed message reception. Note that the word count need not expire in order to complete the message transmission.

The setting of ICSR IN DONE clears both ICSR BUSY and ICSR MSG BUSY. As with the word count overflow interrupt, the ICSR RA1/RA2 register selection flip-flops are altered to point to the IWAR in anticipation that the next DATAO to the input device address of the AN10/AN20 will be a new word count/data address buffer allocation. As soon as the host interrupt service routine clears ICSR IN DONE, ICON LAST IMP BIT RCVD will be cleared. This then enables ICON CONT SHFT so that the ICON RDY DWN DLY OVER flip-flop may be set, thus asserting the signal ICON RDY DWN DLY OVER (9, Figure 4-6). ICON RDY FOR I BIT CLK (10, Figure 4-6) is then triggered to generate the direct set clock of ICON RDY FOR IMP BIT (1, Figure 4-6). The AN10/AN20 is thus ready to begin handshaking with the IMP for reception of a new message.

4.7 ARPANET MESSAGE PADDING

All host-to-host communication over the ARPANET occurs via regular (Type 0) messages. These messages are transmitted over the network as a continuous bit stream; i.e., there are no word boundaries within the message. Figure 4-7 illustrates the format for regular (Type 0) ARPANET messages. Note that only the message leader, the data, and the IMP padding are transmitted over the network. The leader padding is defined and transmitted only between the AN10/AN20 and the IMP to which it is connected, and applies only to regular (Type 0) messages. AN10/AN20 padding, on the other hand, is an internal function within the AN10/AN20 and is used to properly format the bits within the last word of the received message. It applies to all message types received by the AN10/AN20. Message leader padding is used to align the beginning of the data portion of the message with the beginning of a host word boundary. The design of the ARPANET protocol guarantees that between Hosts with identical word lengths, the natural word boundaries are preserved.

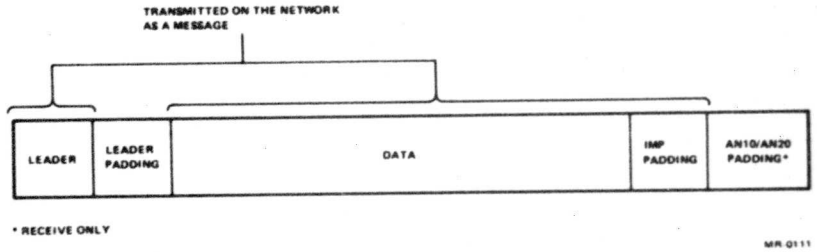


Figure 4-7 ARPANET Message Format - Regular (Type 0)

4.7.1 ARPANET Message Leader

The ARPANET message leader (Figure 4-7) is either the first 32 or 96 bits of a message: 32-bit leaders are "old style" leaders and 96-bit leaders are "new style" leaders. Either type is supported by the AN10/AN20. The leader supplies information such as message type, message ID, and message destination. For further detail, reference "INTERFACE MESSAGE PROCESSOR, SPECIFICATIONS FOR THE INTERCONNECTIONS OF A HOST AND AN IMP", Report No. 1822, Bolt Beranek and Newman, Inc., Cambridge, MA.

4.7.2 ARPANET Message Leader Padding

ARPANET message leader padding (Figure 4-7) occurs immediately after the message leader and is provided as a convenience for Hosts for which the combined Host/IMP (IMP/Host) and Host/Host leaders would otherwise not be an integral number of host memory words. There may be a maximum of nine 16-bit words of message leader padding. The number that the Host wishes to send and receive on regular (Type 0) messages is specified by bits 77-80 in the leader of a NOP (Type 4) message to the connected IMP. Message leader padding provides the means to align the beginning of the data portion of the bit stream with a Host word boundary. Message leader padding exists only across the Host/IMP interface and is not counted in the maximum 8160 bits message length.

4.7.3 ARPANET Message Padding

The ARPANET message has two types of message padding: IMP padding and AN10/AN20 padding (Figure 4-7). Note that IMP padding is transmitted over the ARPANET, but that AN10/AN20 padding is not. Message padding provides the means of recognizing the end of a message at the receiving Host. It is necessary in order to accommodate hosts with word sizes differing from the IMP's word size.

4.7.3.1 ARPANET Message IMP Padding – When the transmitting AN10/AN20 sends a message, the A2I LAST AN10 BIT signal is asserted to the IMP concurrent with transmission, to the IMP, of the last bit of the message. Since the IMP is a 16-bit machine, the last bit of the message may be at any bit location within the 16-bit assembly register that the IMP uses for translating the message bit stream into 16-bit IMP words preparatory for transmission over the ARPANET. In order to make the ARPANET transmission protocol independent of host and IMP word length boundaries, the IMP unconditionally appends a binary ONE to mark the end of the message. The IMP then ZERO-fills any empty bit positions in the last IMP word, as necessary, so as to transmit on the ARPANET a complete 16-bit "last" IMP word. The "last" IMP word may, therefore, be nothing more than IMP pad bits.

The IMP pad bits, therefore, are not transmitted to the source IMP by the transmitting AN10/AN20, but are added to the ARPANET message by the source IMP. The IMP padding is transmitted over the ARPANET and is received by both the destination IMP and Host. The destination IMP's last message bit becomes the last bit of the IMP padding and is, therefore, not the same bit as the source AN10/AN20's last bit.

4.7.3.2 AN10/AN20 Padding – AN10/AN20 padding is applicable only to input transfers. The I2A LAST IMP BIT signal is asserted by the IMP concurrent with the transmittal of the destination IMP's LAST IMP BIT to the AN10/AN20. The I2A LAST IMP BIT signal is not likely to be on a DECsystem-10/20 word boundary because of the IMP padding appended to the original message by the source IMP. The AN10/AN20, therefore, must fill out the remaining bit positions of the last assembled word of the received message with binary ZEROs. This is called AN10/AN20 padding (Figure 4-7). Note that the AN10/AN20 padding is not transmitted over the ARPANET but is generated by the destination AN10/AN20. The destination Host recovers the originally transmitted host-to-host message by stripping off all IMP and AN10/AN20 padding bits under software control. That is, by deleting all trailing binary ZEROs plus the last binary ONE in a message stream.

Figure 4-8 illustrates IMP and AN10/AN20 message padding with the destination Host software stripping off all padding bits. When referring to Figure 4-8, assume the following conditions.

1. Message leader and leader padding not illustrated.
2. The AN10/AN20 is transmitting a message to itself over the ARPANET. This is what the IMPTEST section of MD-10-DDANA and MD-10-DDANB actually does.
3. A 32-bit message is transmitted.
4. The AN10/AN20 transmits and receives the word in 32-bit mode.

4.8 AN10/AN20 AUTOMATIC PRIORITY INTERRUPT CONTROL

An I/O bus interface control of the AN10/AN20 is designed to make extensive use of the advanced automatic priority interrupt (API) control functions supported by the KI10 and KL10 central processing units. By use of the API functions, the system overhead required for servicing the AN10/AN20 is greatly reduced over that which would otherwise be required. The AN10/AN20 may, however, be optionally programmed to support the conventional KA10 polled interrupt structure.

The API function word transfer timing implemented by the AN10/AN20 is illustrated by Figure 4-9. The control logic for handling this timing is distributed across the ABus prints of the M8613 and M8614 modules and the PI print of the M8612 module. The I/O bus drivers and receivers are located on the AN10 IOBD and IOBR prints. To better explain the PI control logic, a DATAO API interrupt request sequence will be traced from start to finish in the paragraphs following. For convenience, Figures 4-10 through 4-14 duplicate portions of the PI and IOBR prints.

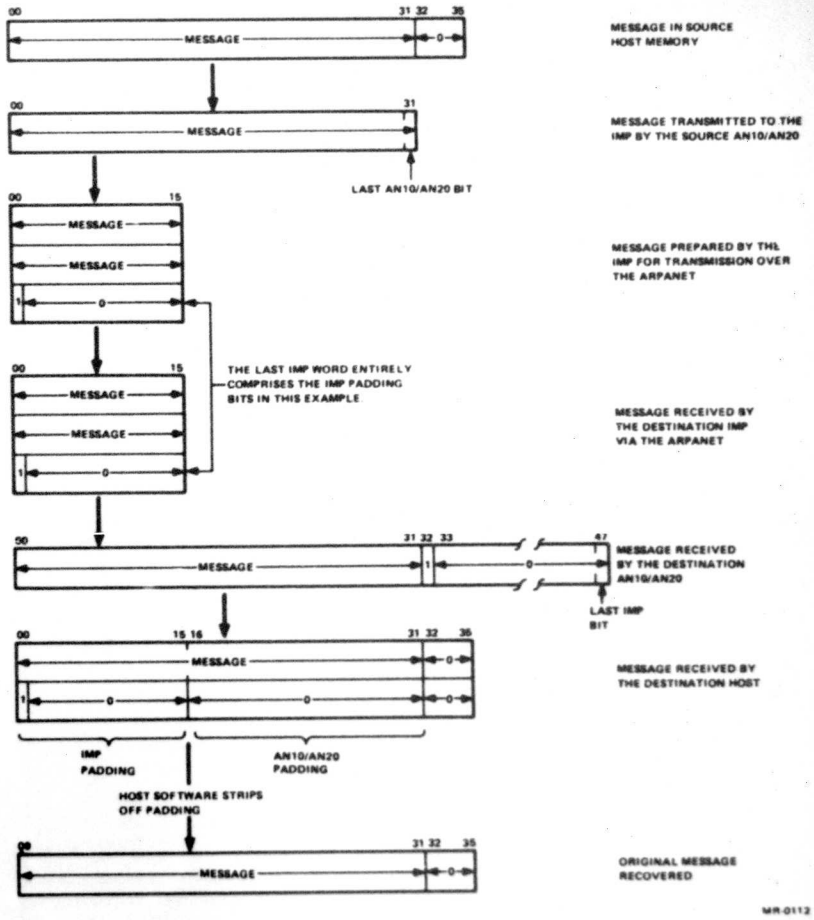


Figure 4-8 IMP and AN10/AN20 Message Padding

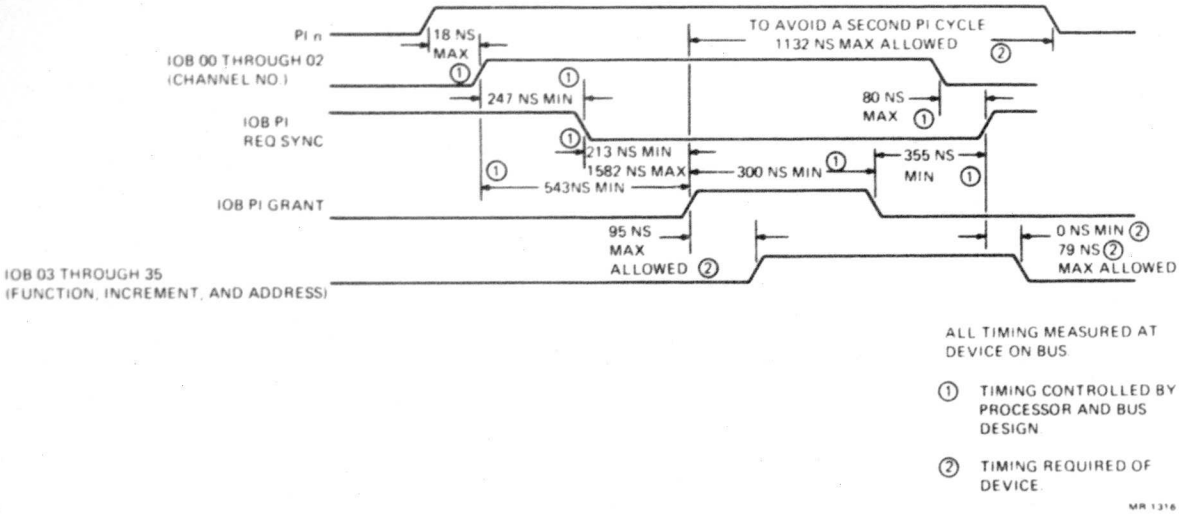


Figure 4-9 External I/O Bus API Timing Requirements

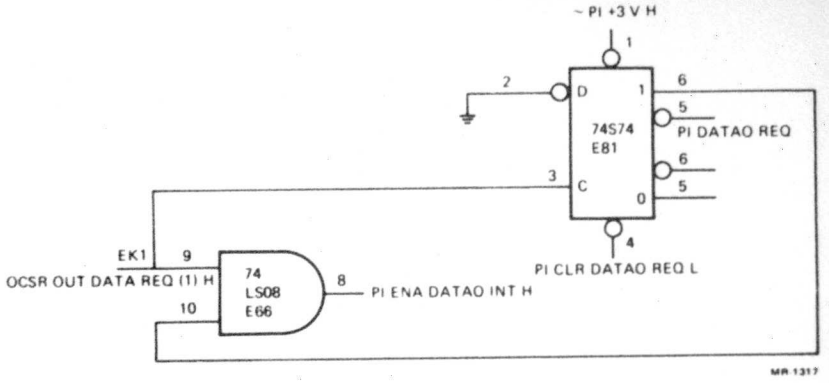


Figure 4-10 PI DATAO REQ

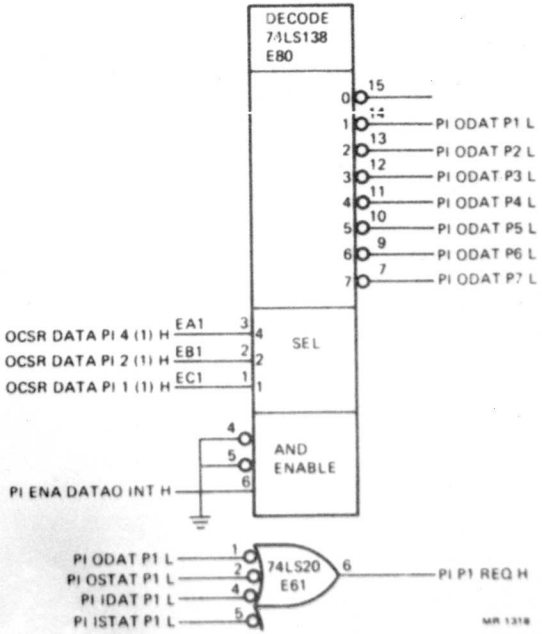


Figure 4-11 Enabling the PI Request Line

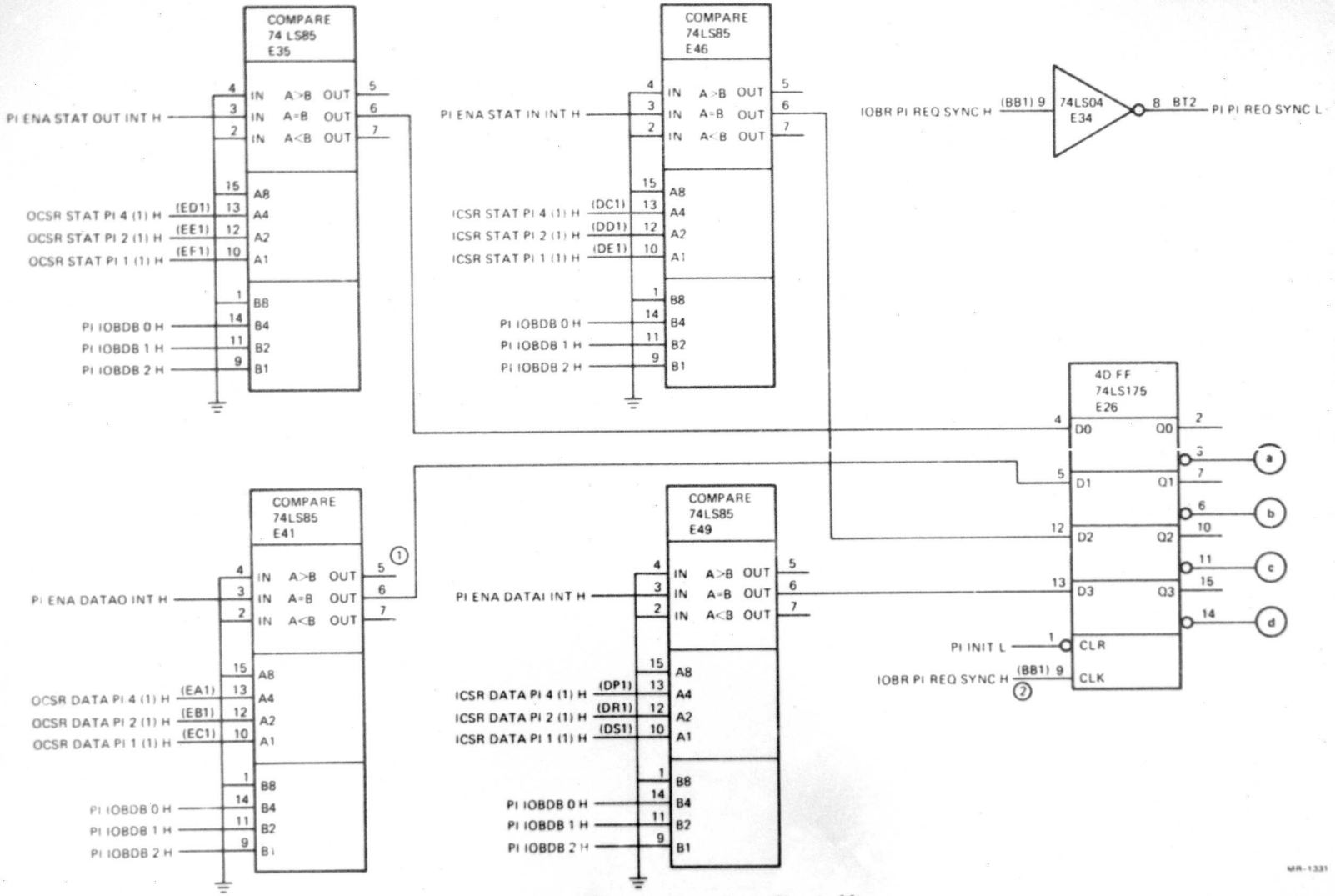
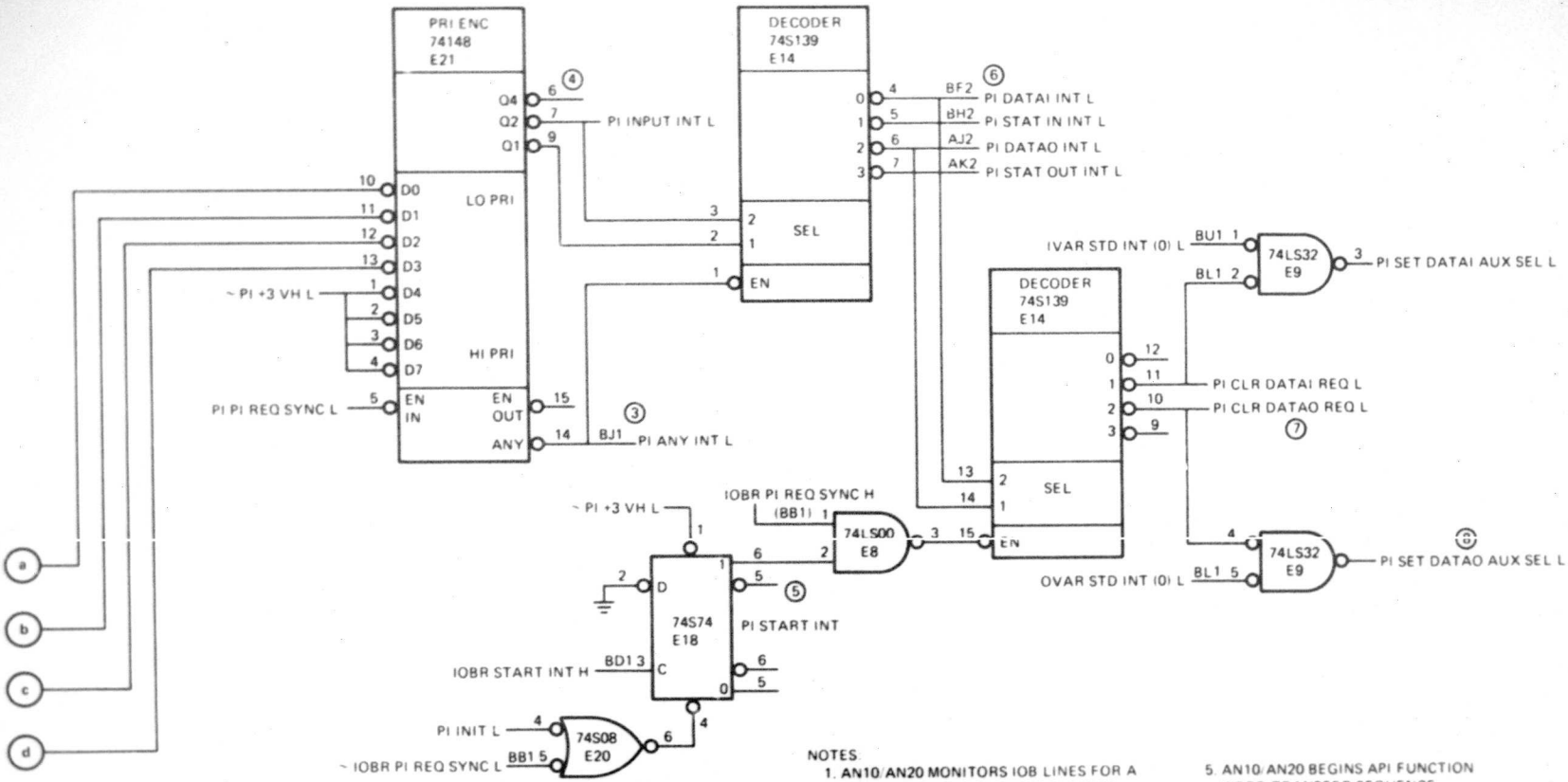


Figure 4-12 **API Interrupt Service Logic (Sheet 1 of 2)**



NOTES:

1. AN10/AN20 MONITORS IOB LINES FOR A MATCH WITH THE PI CHANNEL TO BE SERVED.
2. A VALID MATCH IS STORED.
3. AN10/AN20 WAS ISSUING A PI REQUEST ON THE CHANNEL NOW BEING SERVED. THE PI GRANT SIGNAL ON THE I/O BUS WILL THEREFORE BE INTERCEPTED.
4. THE AN10/AN20 ARBITRATES ANY INTERNAL PRIORITY CONFLICT ON THE PI CHANNEL INTERRUPT NOW BEING SERVICED BY THE HOST CPU.
5. AN10/AN20 BEGINS API FUNCTION WORD TRANSFER SEQUENCE.
6. THE API FUNCTION WORD TYPE IS SELECTED.
7. THE BUFFERED PI REQUEST FLIP FLOP MUST BE CLEARED.
8. FOR A FUNCTION 4 OR 5 API REQUEST, AN AUXILLARY DEVICE SELECT MUST BE SET SINCE THE HARDWARE EXECUTED DATAO(I) WILL HAVE NO IOS CODE.

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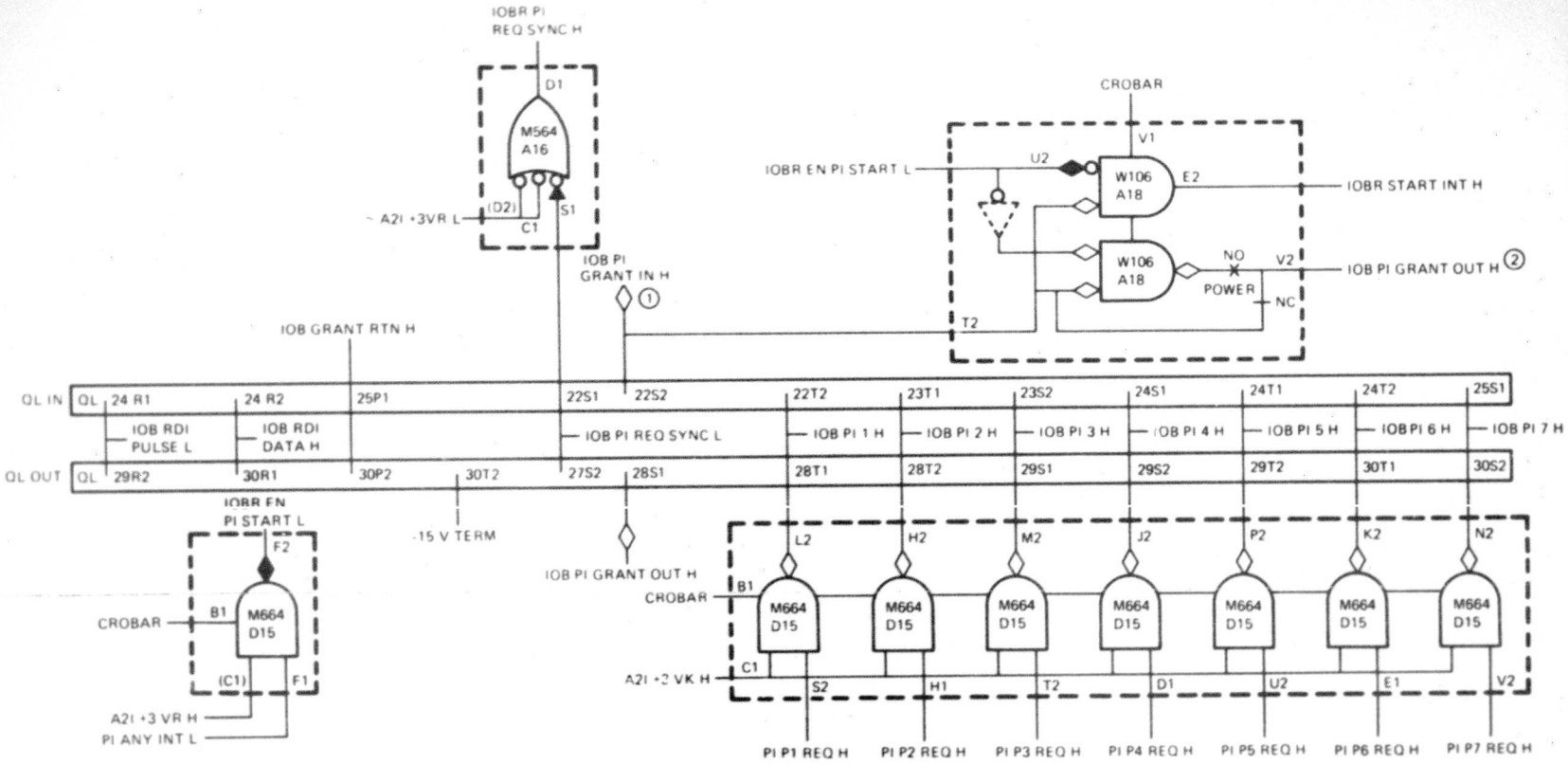
Figure 4-13 IOB PI GRANT Interception



NOTES
1. HOST CPU IS READY FOR AN API FUNCTION WORD TO BE TRANSFERRED.
2. THE AN10/AN20 INTERCEPTS PI GRANT AND INITIATES THE API FUNCTION WORD TRANSFER.

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Figure 4-13 IOB PI GRANT Interception

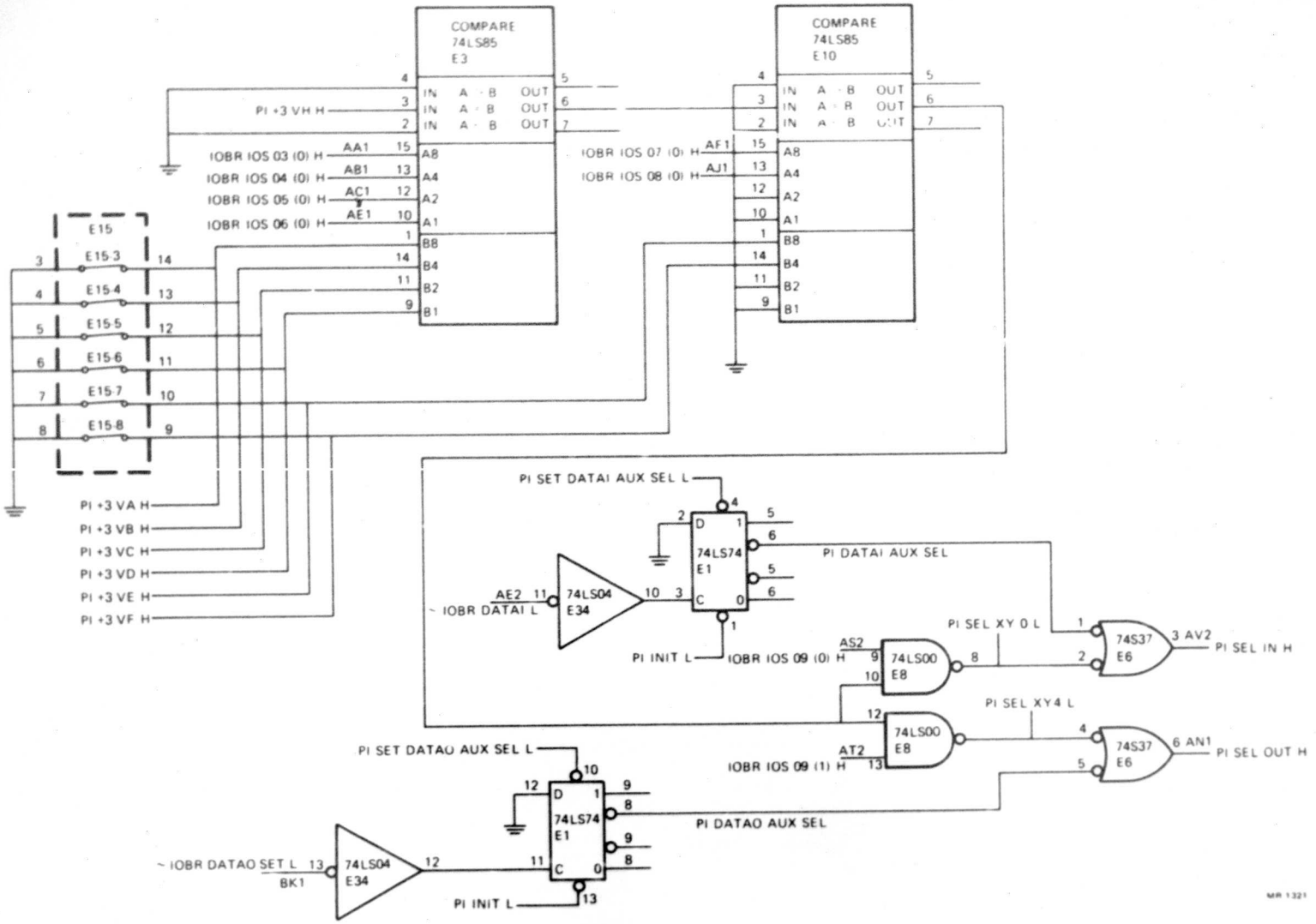


Figure 4-14 IOS Device Code Selection

When the AN10/AN20 output control needs a new word of data to transmit to the IMP, OCSR OUT DATA REQ is set to initiate the interrupt request sequence. This request is buffered by PI DATAO REQ as shown in Figure 4-10.

With this flip-flop set, PI ENA DATAO INT H is asserted to enable the priority interrupt channel decoder for data out interrupt requests (Figure 4-11). The PI REQuest line for the assigned PI channel is then driven onto the I/O bus. Illustrated in Figure 4-11 is PI REQ line 1. The reason that the interrupt request is buffered by PI DATAO REQ is that after the API function word is transferred, the PI REQuest on the I/O bus must be cleared to conform to the timing of Figure 4-9. The source of the interrupt, however, cannot be cleared until the appropriate I/O command invoked by the interrupt is executed.

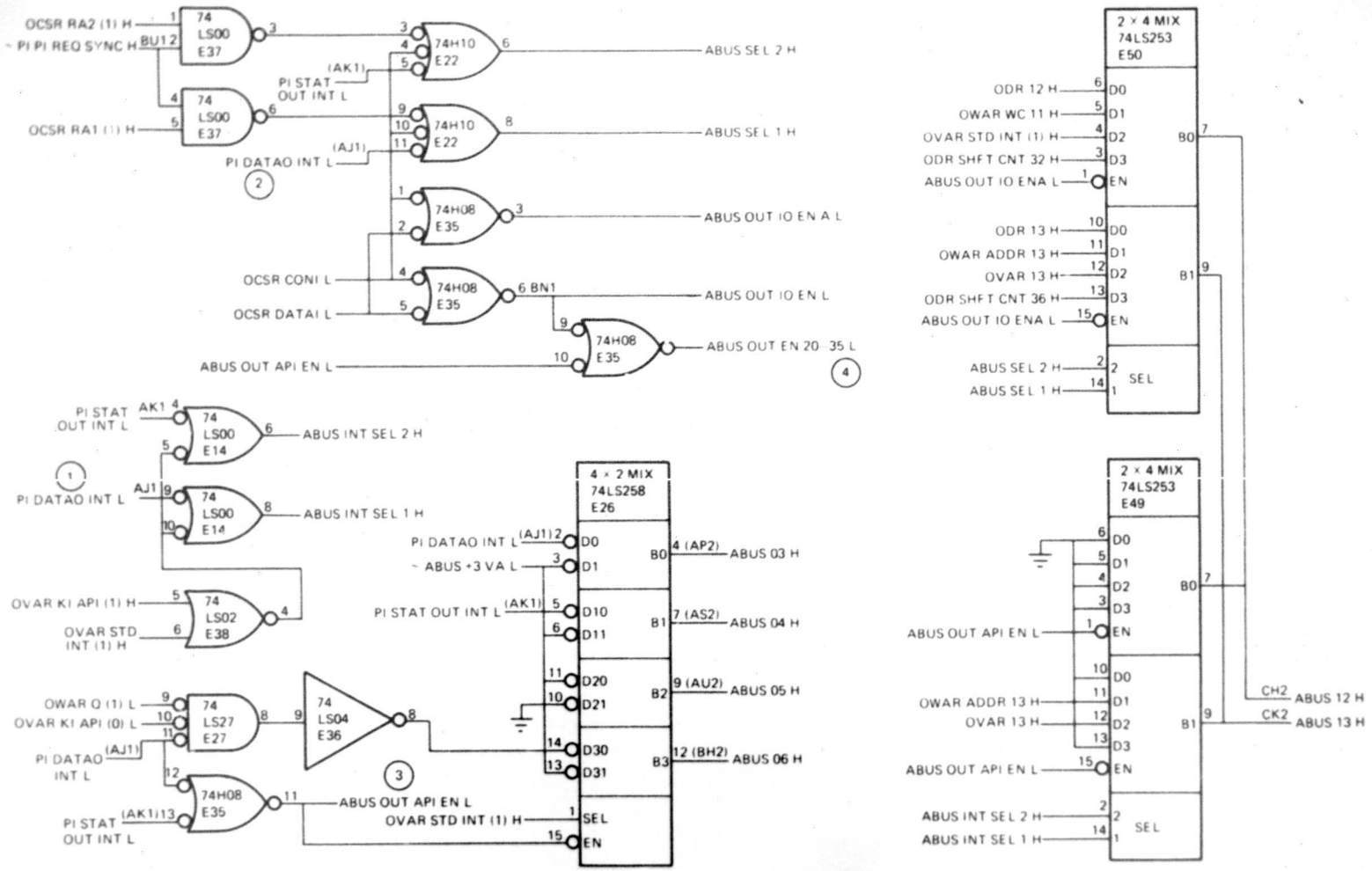
The AN10/AN20 must then wait for the Host CPU to service the priority interrupt channel over which the interrupt is requested. To do this, the IOB data lines 0–2 are continuously monitored for a match with the assigned PI channel number (1, Figure 4-12). When a match occurs concurrent with the Host CPU executing an API service cycle, I/O bus signal IOBR PI REQ SYNC will latch any and all AN10/AN20 interrupt channel matches (2, Figure 4-12). Any match stored in the 74LS175 flip-flop register will cause assertion of PI ANY INT (3, Figure 4-12). This signal means that the AN10/AN20 is in fact requesting an interrupt over the PI channel being served. The PI GRANT signal on the I/O bus must therefore be intercepted. At the same time, the 74148 priority encoder arbitrates any internal AN10/AN20 priority conflicts on the matched interrupt channel (4, Figure 4-12). Data interrupts have priority over status interrupts and input interrupts have priority over output interrupts.

When the host CPU is ready to receive the API function word, IOB PI GRANT IN is asserted (1, Figure 4-13). PI ANY INT asserts IOBR EN PI START L to block PI GRANT, asserting IOBR START INT H rather than passing the grant signal on to the next device on the I/O bus via IOB PI GRANT OUT H (2, Figure 4-13). The PI START INT flip-flop is set to initiate the API function word transfer sequence (5, Figure 4-12).

The encoded internal AN10/AN20 interrupt priority is decoded to select which API function word type will be transferred to the host CPU (6, Figure 4-12). When the selected API function word transfer is started, the buffered interrupt request flip-flop must be cleared to remove the interrupt request from the I/O bus PI request lines. This is necessary to avoid an unwanted second PI cycle. Refer to Figures 4-9, 4-10, and 7, Figure 4-12.

If the API function word is type 4 or 5 (DATAO or DATAI interrupt), an auxiliary device select must be set since the resulting CPU generated DATAO or DATAI will have no IOS select code. Note that the CPU will perform no other I/O operation before executing this required DATAO or DATAI. In this example, a DATAO interrupt (API function 4) is requested. Therefore, PI SET DATAO AUX SEL (8, Figure 4-12) will be asserted to set PI DATAO AUX SEL as illustrated in Figure 4-14. In this manner PI SEL OUT will be asserted, enabling the AN10/AN20 to respond to the subsequent DATAO. Conversely, when an API function type 5 interrupt is requested, PI SEL IN will be asserted via PI DATAI AUX SEL.

Besides causing the buffered interrupt request flip-flop to be cleared and the auxiliary AN10/AN20 device select to be asserted, PI DATAO INT (6, Figure 4-12) also enables the gating of the API function word to the I/O bus. Recall that the API function type must be asserted on I/O bus data lines 3–5 and that the address from which the DATAO is to be executed must be asserted on lines 13–35 for KL10 API format and lines 18–35 for KI10 API format. The I/O bus drivers, illustrated on print D-BS-AN10-0-IOBD, are driven from the internal 36-bit wide multiplexed tri-state ABus of the AN10/AN20. The ABus tri-state multiplexers are documented in prints D-CS-M8613-0-ABus and D-CS-M8614-0-ABUS. In the example being discussed, the ABus multiplexers in question are found on the former print. For convenience, a section of this print is illustrated in Figure 4-15.



1 PI DATAO INT ENABLES SELECTION OF PART 1 OF THE API ABUS MULTIPLEXERS FOR BITS 12–19.

2 THE DATAO INTERRUPT REQUEST ALSO ENABLES SELECTION OF PART 1 OF ABUS MULTIPLEXERS FOR BITS 20–35.

3 THE ENABLE SIGNAL FOR THE ABUS MULTIPLEXERS ASSOCIATED WITH API TRANSFERS IS ASSERTED.

4 THE ABUS MULTIPLEXERS FOR BITS 20–35 ARE ENABLED.

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Figure 4-15 API Function Word Enable Logic

For both the input (M8614) and output (M8613) modules of the AN10/AN20, ABUS bits 3-6 and 12-19 are driven from two multiplexer sets; one for CONI/DATAI operations and one for API transfers. Figure 4-15 illustrates the two ABUS multiplexers for bits 12 and 13, typical of each of these above bits. Only one multiplexer exists, however, for each of bits 20-35. This multiplexer is used for both API and I/O operations. As shown in 1, Figure 4-15, PI DATAO INT asserts ABUS INT SEL 1 to select port 1 of the API ABUS multiplexers for bits 12-19. Also, as shown at 2, Figure 4-5, ABUS SEL 1 is asserted to select port 1 of ABUS multiplexer bits 20-35. If KI10 API format is selected, however, OVAR KI API (1) H will also assert ABUS INT SEL 2H to force selection of port 3, rather than port 1, of the API ABUS multiplexers for bits 12-19. This results in forcing bits 12-17 to zero in accordance with the KI10 API format specification (see Figure 4-15 and D-CS-M8613-0-ABUS).

PI DATAO INT also asserts ABUS OUT API EN (3, Figure 4-15) to enable the ABUS multiplexers used for API transfers. ABUS bit 3 will be asserted to specify API function word type 4. ABUS OUT EN 20-35 (4, Figure 4-15) is in turn asserted to enable the multiplexers for bits 20-35. In this manner, the OWAR address register contents (23 bits for KL10 API format, 18 bits for KI10 format) will be driven onto the I/O bus via the ABUS.

When the CPU has received the API function word, IOBR PI REQ SYNC is removed from the I/O bus. This then disables the AN10/AN20 API function word transfer logic discussed previously. PI DATAO AUX SEL remains set, however, until the requested DATAO is executed by the CPU. The subsequent DATAO cycle clears both the OCSR OUT DATA REQ flip-flop that initiated the entire interrupt sequence as well as PI DATAO AUX SEL (Figure 4-14). This completes the DATAO interrupt cycle.

Vectored (API function 2) and DATAI (API function 5 interrupts operate in a similar manner to the case described in this section.

4.9 AN10/AN20 - IMP CABLE TERMINATION/ TRANSMISSION SYSTEM

Report No. 1822 published by Bolt Beranek and Newman, Inc. requires that the cable line interface to the IMP be source terminated with the cable characteristic impedance. This requirement is applicable to local and to distant IMP interfaces. With this cable transmission scheme, a voltage step of one-half the nominal level is propagated from the source to the receiver. Since the receiver is unterminated and is ideally a high impedance, this voltage step is reflected by the high-impedance termination, which results in a full-level voltage step at the receiver and another half-level voltage step propagating back to the cable driver where it is absorbed by the source termination which matches the cable characteristic impedance. Therefore, in theory, the cable signal appears as illustrated in Figure 4-16. The time duration, t, of the half-step voltage at the cable source end (Figure 4-16) is equal to the round trip cable propagation time. For the BC10T cable, the nominal propagation time is 5.28 ns/m (1.61 ns/ft). Cable capacitance causes rounding of the rising and falling edges of the signal at both ends of the cable. The degree of rounding is a function of cable type and length.

A primary disadvantage of this transmission scheme is that since a reflection is intentional at the cable receive end, the source must be carefully terminated in the cable impedance. Any mismatch will cause undesirable ringing and degradation of the desired signal waveform. Additionally, the waveform at the source end of the wire is noticeably different than at the receive end. See Figure 4-16. This can be misleading to maintenance personnel who are unaware that the signals are source terminated only.

The major advantage of this transmission scheme lies in the fact that since the receiver is unterminated and represents a high-impedance load on the cable, very little current is drawn. Therefore the voltage drop along the cable is minimal. The received voltage (received end of the wire) is essentially the same as the nominal transmitted voltage (source end of the wire). This improves the noise immunity in the cable transmission and permits usage of a smaller AWG wire than would have been required if both ends were terminated. The low signaling current also minimizes the cross-talk noise induced in other lines of the cable. Since the receiver sees a full-step reflection, the signal is clean and is reliably detected. The half-step voltage at the source end is of no concern.

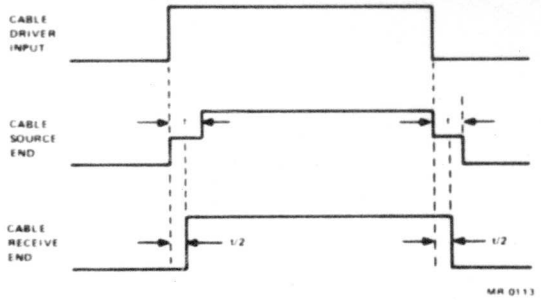


Figure 4-16 AN10/AN20 to IMP Cable Signal Waveforms

4.9.1 AN10/AN20 Local Cable Transmission

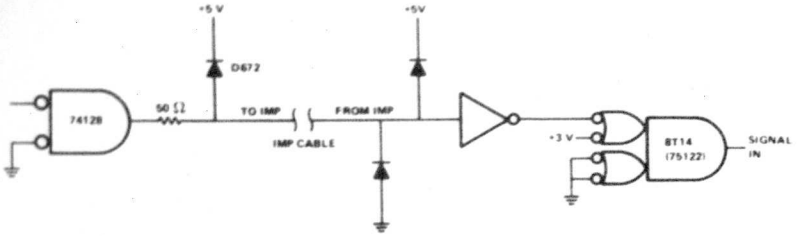
The AN10/AN20 local cable interface uses a 74128 cable driver and an 8T14 (TI75122) cable receiver terminated as illustrated in Figure 4-17A. D672 diodes are used to clip voltage excursions above +5 V and below ground. A source termination of 50 ohms is in series with the 74128 driver. Bolt Beranek and Newman, Inc. Report No. 1822 specifies a nominal termination impedance of 68 ohms. The RG174U coax cable used with a 516 or Pluribus IMP is nominally 50 ohms and the Honeywell twisted-pair I/O cable used with a 316 IMP is somewhat higher; therefore, 68 ohms is a realistic compromise termination. The AN10/AN20 achieves this effective nominal 68 ohm termination impedance through the series-impedance of the 74128 totem pole output and the 50-ohm resistor. The cable signaling current is so small that there is effectively no voltage drop across the 50 ohm resistor. The received voltage is, therefore, essentially that of the 74128 output. Figure 4-17B illustrates typical local cable connection waveforms.

4.9.2 AN10/AN20 Distant Cable Transmission

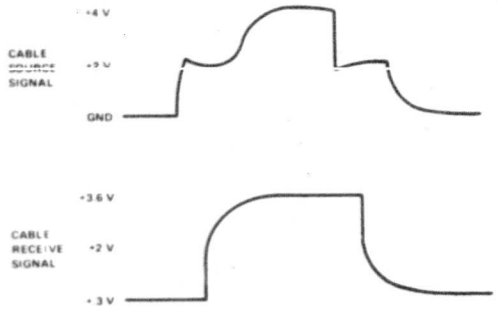
The AN10/AN20 distant cable interface uses a 75112 dual differential line driver and a 75107B receiver terminated as illustrated in Figure 4-18A. The BC10T cable supplied for the AN10/AN20 distant interface connection comprises 12 twisted pairs of 20 AWG, 7-strand tinned copper. The characteristic impedance of the controlled impedance pairs is 110 ohms ±4% for balanced operation. The minimum bend radius is six times the cable diameter. The propagation delay of signals is nominally 1.61 ns/ft.

The distant transmission line is source terminated only as illustrated in Figure 4-18A. Each line of the balanced differential pair is terminated by a resistance of 422 ohms to +5 V and 68.1 ohms to ground, resulting in a balanced termination impedance of 117 ohms for the pair. As the 75112 line driver operates, the "OFF" signal line voltage is determined by the termination resistors and is approximately 0.70 V. Conversely, the "ON" signal is pulled negative toward the -5 V supply with a current of approximately 24 mA to give an "ON" signal voltage of -0.71 V (nominal). Thus, the twisted pair cable is driven with a balanced ±0.7 V signal (1.4 V peak-to-peak). As long as the "inhibit" input of the 75112 line driver is at +3 V (always the case with the AN10/AN20), one signal output will be "ON" while the other is "OFF".

Similar to local cable transmission, previously described, the high impedance input of the unterminated receiver draws so little current that the voltage at the end of a 610 meter (2000 foot) cable is essentially the same as the driver nominal output voltage after the received half-step voltage is reflected back into the cable. Figure 4-18B illustrates a typical waveform for a 15 meter (50 foot) distant cable.



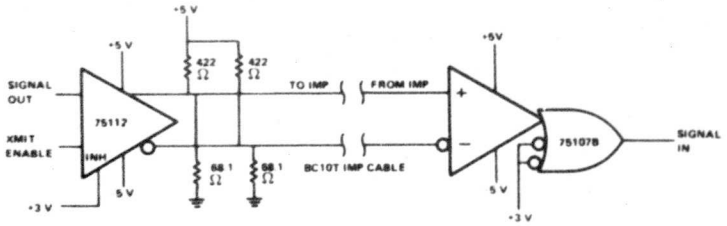
A
LOCAL CABLE TERMINATION CIRCUIT



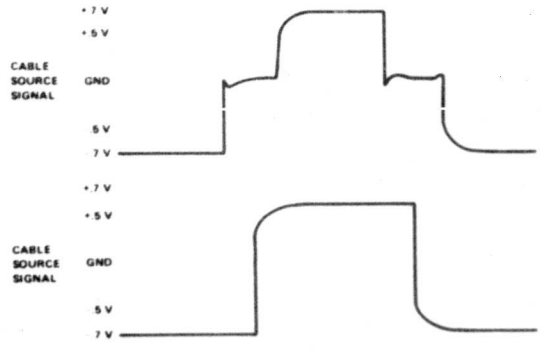
B
TYPICAL LOCAL CABLE SIGNALING WAVEFORMS

MR-0114

Figure 4-17 AN10/AN20 Local Cable Termination Circuit and Typical Signaling Waveforms



A
DISTANT CABLE TERMINATION CIRCUIT



B
TYPICAL DISTANT CABLE SIGNALING WAVEFORMS
15M(50 FT) BC10T CABLE

MR-0115

Figure 4-18 AN10/AN20 Distant Cable Termination Circuit and Typical Signaling Waveforms

A 15 meter (50 foot) distant cable connection consists of a 15 meter (50 foot) BC10T cable to the IMP plus a 1.25 meter (4 foot) BC06R cable connecting to the M8612 module. If the BC10T cable is looped back by the 70-13995 BC10T loopback connector and the signals scoped on the AN10/AN20 M8612 module, a total of 32.9 meters (108 feet) is in the circuit between the 75112 driver and the 75107B receiver. The round trip cable propagation distance is therefore 65.8 meters (216 feet). At a propagation rate of 5.28 ns/meter (1.61 ns/foot), the time duration of the half-step voltage reflection illustrated in Figure 4-18A would be approximately 348 ns.

As the cable distance is extended toward the maximum allowable 610 meters (2000 feet) the cable capacitance has a more noticeable effect on the cable signal rise and fall times. It is possible for the speed of the AN10/AN20 to switch the cable driver before the driven end of the cable has charged to its full nominal voltage after the half-step voltage is reflected back into the cable by the receiver. As long as sufficient time is allowed for the half-step reflection at the driven end of the cable to propagate to the receiver and be reflected back into the cable, a full-step will still occur at the receiver even though the driven end may never reach the full nominal voltage. The reader must be aware of this when attempting to analyze the signals over a 610 meter (2000 foot) cable between the AN10/AN20 and the IMP because the waveform pattern familiar in the previous cases is somewhat obscured in this case. Figure 4-19 illustrates a typical distant cable signaling waveform for 610 meter (2000 foot) BC10-T cable in the case of the AN10/AN20 switching the drive signal before the full nominal voltage driver output is reached. Of course, in cases where the AN10/AN20 does not switch the cable signals this rapidly, the typical waveform pattern will be recognized. Note that over a 610 meter (2000 foot) cable, the half-step voltage duration will be approximately 6.5 μs.

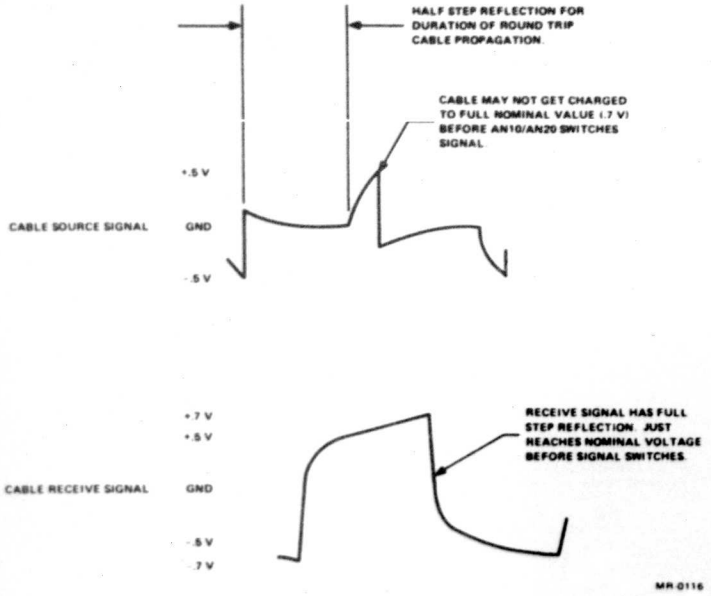


Figure 4-19 Distant Cable Signaling Waveform

CHAPTER 5
MAINTENANCE

5.1 MAINTENANCE OVERVIEW

The AN10/AN20 ARPANET Interface Option incorporates several diagnostic features designed to facilitate maintaining and troubleshooting the device. The troubleshooting capabilities include several internal loopback modes as well as the capability to single-step the handshake control signals to/from the IMP.

Most of the AN10/AN20 logic is partitioned on three modules:

1. M8612 I/O Control contains the host I/O bus interface as well as the IMP cable drivers and receivers.

2. M8613 Output Control contains all control logic and registers pertaining to output message transfers.

3. M8614 Input Control contains all control logic and registers pertaining to input message tranfers.

Refer to Figure 4-1 for a graphic illustration of this partitioning. The diagnostic features of the AN10/AN20 are designed around this partitioning of the logic to aid board level troubleshooting of the device.

CAUTION

The field engineer maintaining the AN10/AN20 should note from the module utilization print (D-MU-AN10-0-MU) that the backplane logic begins with column number 6. The first used slot in the backplane is slot 9, occupied by the M8614.

To facilitate wiring of the backplane assembly, including the quick-latch connectors, the logic mounting frame is assigned column slot numbers as illustrated in drawing D-AD-7013480 sheet 4 of 5. The 13-slot AN10/AN20 backplane is physically mounted in the slot positions numbered 6 through 18. Also, the quick-latch connector slots begin with slot 22. Connectors QL1 and QL2, however, are positioned straddling logic rows A and B as illustrated on sheet 5 of 5 of D-AD-7013480. For wirelist purposes, each connector slot occupies pins U through Z of logic row A and pins A through L of logic row B. These are the pin assignments in the AN10/AN20 backplane wire list. However, the mylar overlay for the connector wire wrap pins labels each of the seven columns of pins with the letters A through T, with each column occupying one half of a backplane slot. The columns are therefore referenced as either the "1" side or the "2" side of a backplane slot.

Because of the lettering on the mylar overlay, the print set documents the pins with the letter assignment of the overlay. The upper left pin of QL1 is therefore 22A1 and the lower right pin is 25T1. Likewise, the upper left pin of QL2 is 27A2 while the lower right pin is 30T2. In the backplane wire list these four pins are A22U1, B25L1, A27U2, and B30L2, respectively. The field engineer must therefore reference D-AD-7013480 sheet 5 of 5 to translate the quick-latch connector pin nomenclature within the print set to that of the wire list.

5.2 AN10/AN20 CABLE LOOP BACK TO THE IMP

The AN10/AN20 supports IMP cable loop back testing by providing a cable loop connector in the AN10/AN20 cabinet prewired to loop back to the IMP the following signals (refer to Chapter 3 for signal definitions):

IMP READY TEST signal to AN10 READY TEST signal
IMP MASTER READY signal to AN10 MASTER READY signal
YOUR IMP BIT signal to YOUR AN10 BIT signal
READY FOR AN10 BIT signal to READY FOR IMP BIT signal
IMP TO AN10 DATA signal to AN10 TO IMP DATA signal
LAST IMP BIT signal to LAST AN10 BIT signal

By using the IMP cable loop back connector, IMP personnel can test the conductors of the AN10/AN20-IMP cable as well as the IMP cable drivers and receivers. This loopback connector in the AN10/AN20 cabinet (ZIF connector labeled "IMP LOOP") will handle both local and distant cables.

5.3 DIAGNOSTIC LOOP BACK MODES

In order to diagnose the AN10/AN20, several diagnostic loop back modes are available. These test modes provide the capability to completely check out the AN10/AN20 without requiring an IMP as test equipment. The loopback modes include output to input loop back testing, output loop testing, and input loop testing. Each of these test modes may be single stepped. The test mode control bits are enabled by setting MAINT MODE (OCSR bit 20). IMP PORT DISABLED (OCSR bit 19) must also be set to prevent assertion of the AN10 MASTER READY signal and the data handshake signals to the IMP if an internal loop test is desired.

5.3.1 Output to Input Loop Back

Output to Input loop back may be performed either internally or externally to the AN10/AN20. To loopback externally but local to the AN10/AN20 for either a local or distant connection, the AN10/AN20-IMP cable must be disconnected from the AN10/AN20 logic assembly and the AN10/AN20 test connector 70-13963 inserted in its place. To loopback externally but at the end of the BC10T distant cable, the BC10T cable must be disconnected from the IMP and the cable must be terminated with the loopback-connector 70-13995. Both loopback connectors will loopback the following signals:

AN10 READY TEST signal to IMP READY TEST signal
AN10 MASTER READY signal to IMP MASTER READY signal
READY FOR IMP BIT signal to READY FOR AN10 BIT signal
YOUR AN10 BIT signal to YOUR IMP BIT signal
LAST AN10 BIT signal to LAST IMP BIT signal
AN10 TO IMP DATA signal to IMP TO AN10 DATA signal

External loopback is programmed by setting MAINT MODE (OCSR bit 19) in conjunction with setting LOOPBACK (OVAR bit 06). The installed cable loopback connector looks to the AN10/AN20 logic like a very fast IMP.

Internal loopback is programmed by setting IMP PORT DISABLED and MAINT MODE (OCSR bits 19 and 20) in conjunction with setting LOOP BACK (OVAR bit 06). The IMP cable receivers and drivers are disabled and the above signals (except for the READY TEST lines) are connected together by logic gates with the simulated loopback signals ORing to the same logical points as the disabled cable receiver outputs. The AN10/AN20-IMP cable does not have to be disconnected. In this case the IMP MASTER READY signal is driven from the AN10 READY flip-flop.

Both internal and external loop back may be single stepped by setting either or both OUT S CYC (OVAR bit 05) and IN S CYC (IVAR bit 05). OUT S CYC (out single cycle) selects OVAR RDY FOR AN10 BIT as the source for the RDY FOR AN10 BIT signal in the OCON RDY FOR AN10 BIT multiplexer rather than the AN10/AN20-IMP cable signal (I2A READY FOR AN10 BIT) as would normally be the case; to continue a cycle requires writing the proper polarity of OVAR RDY FOR AN10 BIT by a DATAO to the OVAR. IN S CYC (in single cycle) selects IVAR YOUR IMP BIT as the source for the YOUR IMP BIT signal in the ICON YOUR IMP BIT multiplexer rather than the AN10/AN20-IMP cable signal (I2A YOUR IMP BIT) as would normally be the case; to continue a cycle requires writing the proper polarity of IVAR YOUR IMP BIT by a DATAO to the IVAR. The data wrapped around may be monitored by reading ICON I2A DATA (IVAR bit 07). In this manner the demand/response handshake sequence necessary for transferring data is interrupted and may be simulated by the diagnostics. The AN10/AN20 internal states may be examined at each handshake sequence.

5.3.2 Output Loop

The output section of the AN10/AN20 may be looped on itself to facilitate troubleshooting problems pertinent to the M8613 output control module. This diagnostic mode is internal to the AN10/AN20 and is programmed by setting IMP PORT DISABLED and MAINT MODE (OCSR bits 19 and 20) in conjunction with setting OUT LOOP (OVAR bit 04). The AN10/AN20-IMP cable does not have to be disconnected since the cable drivers and receivers are disabled. The loop is accomplished by logically connecting the inverted form of the YOUR AN10 BIT signal to the READY FOR AN10 BIT signal, and is programmably selected to be either self-sustaining or single stepped by OUT S CYC. The data transferred may be monitored by reading AN10 TO IMP DATA (OCSR bit 02). IMP READY will set 425 ms after OUT LOOP is set to enable the data handshake multiplexers.

5.3.3 Input Loop

The input section of the AN10/AN20 may be looped on itself to facilitate troubleshooting problems pertinent to the M8614 input control module. This diagnostic mode is internal to the AN10/AN20 and is programmed by setting IMP PORT DISABLED and MAINT MODE (OCSR bits 19 and 20) in conjunction with setting IN LOOP (IVAR bit 04). The AN10/AN20-IMP cable does not need to be disconnected since the cable drivers and receivers are disabled. The loop is accomplished by logically connecting the READY FOR IMP BIT signal to the YOUR IMP BIT signal, and is programmably selected to be either self-sustaining or single stepped by IN S CYC. The data source is the read/write bit IMP TO AN10 DATA (IVAR bit 02). IMP READY will set 425 ms after IN LOOP is set to enable the data handshake multiplexers. AN10 READY must also be set to enable the input control timing logic.

5.4 MD-10-DDANA TEST OPTIONS

The diagnostics for the AN10/AN20 ARPANET interface are logically and physically divided into two programs: MAINDEC-10-DDANA, and MAINDEC-10-DDANB.

MD-10-DDANA (DDANA) is the basic ARPANET interface diagnostic designed to test the AN10/AN20 interface. DDANA is run only in EXEC mode, requires the diagnostic monitor and subroutine packages, and is not supported in USER mode.

The minimum system configuration is an operational processor with at least 64K of memory, a console TTY, a means of loading the diagnostic, and a source for all the required support files. Note that the required support files vary for different processor types.

DDANA is divided into two distinct testing phases. First, the diagnostic phase is run to verify that the hardware is functional. This phase does not require that the AN10/AN20 be connected to an IMP, as no communication will take place with it. The diagnostic can be looped back (output to input) in two

modes: Internal Loopback, which disables the cable drivers and receivers and internally connects the input to the output; and External Loopback, which requires that the special loopback connector (70-13995) be installed at the IMP end of the BC10T cable, or that the special local loopback cable connector (70-13963) be installed at the AN10/AN20.

When the functionality of the AN10/AN20 has been verified via the diagnostic as detailed above, the next step is to run the IMPTST portion of MD-10-DDANA. This is a reliability verification test, and runs in a mode similar to that of the TOPS20-AN monitor, as far as the AN10/AN20 is concerned. IMPTST requires that the AN10/AN20 be connected to the IMP, as messages will be sent out onto the network, specifying the current Host as the destination.

MD-10-DDANB (DDANB) is a program designed to run in USER mode under the TOPS20-AN Operating System. DDANB provides a means for running an equivalent of DDANA IMPTST without taking the system down to run stand-alone. DDANB implements a flexible terminal controlled running environment by providing the capability to change all important parameters including starting and stopping message transmission to/from the IMP. It also allows the user to specify an external file from which to take the commands.

5.5 AN10/AN20 ONE-SHOT TIMING SPECIFICATIONS

The AN10/AN20 control timing one-shots on the M8612, M8613, and M8614 modules are factory checked for proper pulse widths and timing relationships. However, if a timing component on one of these modules needs to be changed, it may be necessary to recheck for proper timing. The timing tolerance specification and the procedure for making the checks are outlined in the paragraphs following. An oscilloscope and diagnostic MD-10-DDANA are required.

5.5.1 One-Shot Timing Verification

Perform the following procedures to verify the AN10/AN20 one-shots are timed within specification.

1. Load MD-10-DDANA, consult listing for switch settings and operating instructions.
2. Insert 70-13963 AN10/AN20 loopback test connector in place of the IMP cable to permit local external loopback.
3. Put the M8614 module on an extender card and verify that the following pulse widths are within the specification tolerance. Loop on test 74 with external loopback selected. Consult the listing for operating procedures.

SIGNAL NAME	PIN NUMBER	NOMINAL VALUE	MINIMUM VALUE	MAXIMUM VALUE
ICON DESKEW DELAY	E01613	50 ns	40 ns	90 ns
ICON DLY CLK	E01605	100 ns	80 ns	160 ns
ICON LOCAL BIT DLY UP	E01113	75 ns	60 ns	130 ns
ICON DIST BIT DLY UP	E01105	1.5 μs	1.1 μs	2.0 μs
ICON RDY FOR I BIT CLK	E03705	50 ns	40 ns	90 ns
ICON RDY DWN TIME DLY	E00413	200 ns	160 ns	275 ns
ICON DIST BIT DLY DWN	E00405	1.5 μs	1.1 μs	2.0 μs

4. Loop on test 70 of MD-10-DDANA to verify that the following pulse widths are within the specification tolerance listed below. Consult the listing for operating procedures.

SIGNAL NAME	PIN NUMBER	NOMINAL VALUE	MINIMUM VALUE	MAXIMUM VALUE
ICON DATA PAD DLY	E02813	50 ns	40 ns	90 ns
ICON DATA PAD CLK	E02805	100 ns	80 ns	160 ns
ICSR RESET	E07213	1.5 μs	1.1 μs	2.0 μs

5. Verify that the time from the negation of ICON SHFT DATA H (E05903) to the negation of ICON RDY DWN TIME DLY (1)H (E00413) is 75 ns (see Figure 5-1). Measure this while looping on test 74 with external loopback specified. Consult listing for operating procedures.

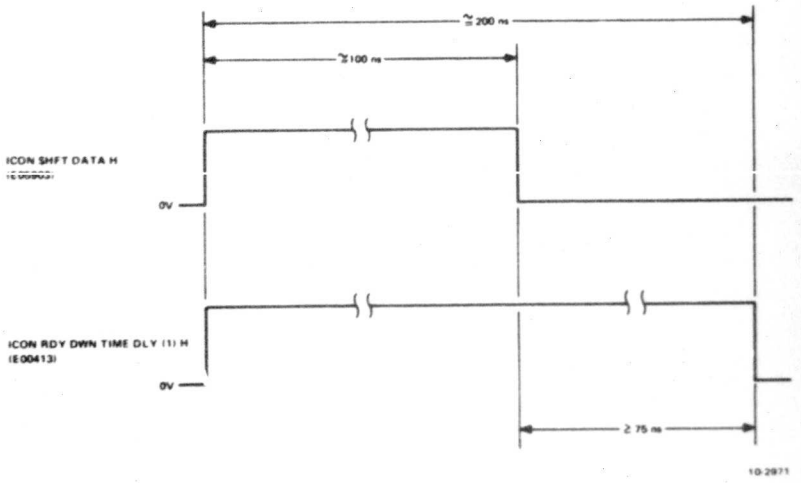


Figure 5-1 ICON SHIFT DATA H and ICON RDY DWN TIME DLY (1) H Signal Timing

6. Put the M8613 module on an extender card and verify that the following pulse widths are within the specification tolerance below. Loop on test 74 with external loopback selected. Consult listing for operating procedures.

SIGNAL NAME	PIN NUMBER	NOMINAL VALUE	MINIMUM VALUE	MAXIMUM VALUE
OCON DIST BIT DLY UP	E00405	1.5 μs	1.1 μs	2.0 μs
OCON LOCAL BIT DLY UP	E00413	100 ns	80 ns	160 ns
OCON CNT	E01113	160 ns	125 ns	220 ns
OCON DIST BIT DLY DWN	E01613	1.5 μs	1.1 μs	2.0 μs
OCON DLYD PULSE	E01105	50 ns	40 ns	90 ns
OCON SKEW DLY	E01605	350 ns	270 ns	450 ns
OCSR CONO CLR DLY	E05105	100 ns	80 ns	160 ns

APPENDIX A
SPECIFICATIONS

AN10 SPECIFICATIONS

OPTION DESIGNATION	AN10-AA (115 V/60 Hz, LOCAL) AN10-AB (230 V/50 Hz, LOCAL) AN10-BA (115 V/60 Hz, DISTANT) AN10-BB (230 V/50 Hz, DISTANT)

MECHANICAL

Height	183 cm (72 in)
Width	54 cm (21 in)
Depth	76 cm (30 in)
Weight	195 kg (430 lb)
Cab Type	H956
Skid Type	1210568-01

DEVICE PERFORMANCE

IMP Connections (switch selectable on M8612 module):

Local:	up to 9 m (30 ft) cable, source-terminated, unbalanced, single-endedly driven
Distant:	up to 610 m (2000 ft) cable, source-terminated balanced, differentially driven
Data Transfers:	Full Duplex
Data Format:	AN10/IMP: Bit Serial AN10/DECsystem-10 (Host): Word Oriented and Interrupt Driven
Data Rate:	100,000 bits per second The maximum upper limit is dependent on system configuration, software, number and type of users, and size of message transfer. The AN10/AN20 itself is capable of handshaking data at an 850K-bit rate full duplex over a 9 meter (30 foot) cable, but this rate is not supported on the T-series host.
Host Data Modes (Programmable):	36 bits 32 bits (packed left-justified within DECsystem-10 word)

B10

Interrupt Modes (Programmable):

KA10 Style
KI10/KL10 Vector Style

Signaling:

Protocol: Programmable Demand/Response two-way or four-way handshake per bit on input

Deskew: IMP to Host data deskew by 50 ns.
Host to IMP data deskew by 350 ns.

Device Codes (switch-selectable on M8612 module):

Input Device Code 520 (standard)
Output Device Code 524 (standard)

Registers:

Input Section:

Control/Status
Data
Word Count/Address
Vector Address

Output Section:

Control/Status
Data
Word Count/Address
Vector Address

Maintenance Modes:

IMP Cable Loop Back to IMP from AN10 (uses mechanical connector)

Output to Input Loop Back – internal and external (external uses loop back plug)

Output Loop Back – internal

Input Loop Back – internal

Single Cycle Handshake

CABLE LENGTH

AN10-A Standard:	9 m (30 ft) Customer Supplied
AN10-B Standard:	15 m (50 ft) BC10T-50
Optional:	30 m (100 ft) BC10T-A0
	46 m (150 ft) BC10T-A5
	61 m (200 ft) BC10T-B0
	76 m (250 ft) BC10T-B5
	152 m (500 ft) BC10T-E0
	305 m (1000 ft) BC10T-L0
	457 m (1500 ft) BC10T-L5
	610 m (2000 ft) BC10T-Y0

POWER

Steady State Current:

AN10-AA or -BA: 110–120 Vac nominal (93–128 min-max), 60 ± 1 Hz, 3 A, single phase (standard)

AN10-AB or -BB: 220–240 Vac nominal (187–256 min-max) 50 ± 1 Hz, 1.5 A, single phase (standard)

Surge Current: 10 A at 120 Vac, 60 Hz

Leakage Current: 3.5 ma. max.

Direct Current:

+5 V, 3.5 A
-15 V, 1.0 A
-5 V, 0.4 A

Power Dissipation:

360 W
310 kg cal/hr (1230 Btu/hr)

OPERATING ENVIRONMENT

Temperature 15 to 32° C (59 to 90° F)

Relative Humidity 20 to 80% with maximum wet bulb temperature of 25° C (77° F)

Altitude 2438 m (8000 ft)

C14

AN20 SPECIFICATIONS

NOTE

The AN20 is the same as the AN10 except for the cabinet (dimensions and weight), which follow.

MECHANICAL

Height	152 cm (60 in)
Width	66 cm (26 in)
Depth	76 cm (30 in)
Weight	218 kg (480 lb)
Cab Type	H9502
Skid Type	None