pdp11

MM11-S, MF11-L, and MF11-LP core memory systems

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CONTENTS

CONTENTS (Cont)

CONTENTS (Cont)

ILLUSTRATIONS

ILLUSTRATIONS (Cont)

TABLES

INTRODUCTION

This manual contains a description of the operation and maintenance of the MM11-S, MF11-L, and MF11-LP Core Memory systems. These memory systems are random access, magnetic core memories used with the PDP-11 family. The level of discussion assumes that the reader is familiar with basic digital computer theory.

Signals and data are transferred between the memory and the PDP-11 processor via the Unibus; however, this manual does not contain a description of the Unibus. A detailed description of the Unibus is contained in the *PDP-11 Peripherals and Interfacing Handbook,* DEC publication no. 112.01071.1854.

Engineering drawings are referenced by their drawing numbers. Drawings pertaining to the MF11-L are contained in the *PDP-11/40 and PDP-11/45 System Engineering Drawings Manuals.* Drawings pertaining to the MM11-S and the MF11-LP are contained in the *MM11-S Engineering Drawings Manual* and the *MF11-LP Engineering Drawings Manual,* respectively.

This manual is divided into three chapters and two appendices. Chapter 1 contains a description of the three memory systems, their purposes, and their use. Chapter 2 contains a detailed description of the logic operations, and Chapter 3 contains maintenance information, adjustment procedures, and programming tests. Appendix A contains a description of the operation of the MF11-LP. Appendix B contains descriptions of the integrated circuits not described on the engineering drawings.

CHAPTER 1
GENERAL DESCRIPTION

1.1 INTRODUCTION

The MM11-S, MF11-L, and MF11-LP Core Memory systems are coincident current, random access, magnetic core memory systems intended for use with the PDP-11 family. All three systems are basically similar in that the basic system consists of a 16-bit, 8K word memory, which uses plug-in modules that are common to all systems. Differences in the backplane or the addition of a parity controller determine the model. The MM11-S backplane limits the size of the memory to 8K. The MF11-L backplane has additional slots to allow expansion of the capacity to 24K in 8K increments. The MF11-LP is an MF11-L system to which a parity checking option has been added.

1.2 GENERAL DESCRIPTION

The MM11-S, MF11-L, and MF11-LP provide 8192 (8K) 16-bit words. The MM11-S and MF11-L require three modules; two are hex-height and the other is quad-height. One hex-height module (G110) contains the control logic, inhibit drivers, sense amplifiers, and 16-bit data register. The other hex-height module (G231) contains the address selection logic current generators, switches, and drivers. The quad-height module (H214) contains the 8K memory stack. These three modules by themselves are designated an MM11-L memory. Two additional MM11-L memories can be plugged directly into the MF11-L to expand its capacity to 24K.

The MF11-LP uses three modules similar to those of the MM11-L memory. A G109 Control Module is used instead of a G110, and an H215 Stack Module is used in place of the H214. These modules perform functions identical to those in the MM11-L memory, with the exception of additional circuitry used for parity control. Two additional bit locations, bits 17 and 16, are used to store high and low byte parity, respectively. A fourth module, an M7259, is used for the parity controller. The M7259 is a dual-height module, and it is capable of controlling parity for up to 24K words. Thus, if an MF11-LP is expanded to its optional capacity of 24K words, only one M7259 is required. The 8K incremental memory used for expansion of the MF11-LP is designated the MM11-LP.

Figures 1-1, 1-2, and 1-3 show the component sides of the modules that constitute the MM11-L memory. The MM11-LP is described in Appendix A of this manual. Table 1-1 contains a listing of the basic differences among the models of the memory systems described in this manual. Figure 1-4 shows simplified block diagrams of the three memory systems.

Since the MM11-L memory is common to both the MF11-L and the MM11-S memory systems, the description contained in the following chapters is applicable to both the MF11-L and MM11-S memory systems.

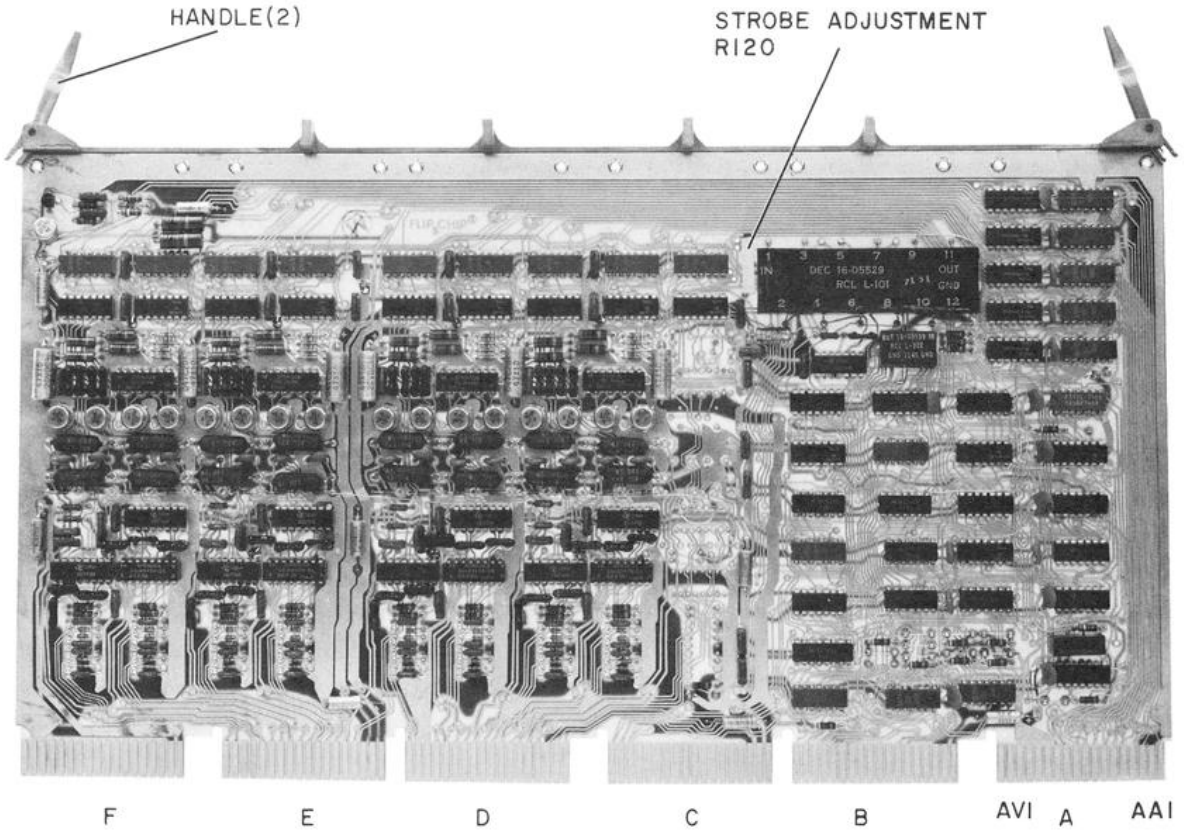


Figure 1-1 Component Side of Control Module G110

Table 1-1
Memory Configurations

Designation	Description	Reference
MM11-S	8K word memory comprising one MM11-L memory and a single system unit (4 x 6) backplane.	Chapters 1, 2, and 3
MF11-L	8K word memory comprising one MM11-L memory and a double system unit (9 x 6) backplane. Two additional MM11-L memories can be plugged in to expand the capacity to 24K.	Chapters 1, 2, and 3
MF11-LP	8K word memory with parity control comprising one MM11-LP memory and a double system unit (9 x 6) backplane. Two additional MM11-LP memories can be plugged in to expand the capacity to 24K.	Chapters 1, 2, and 3 Appendix A

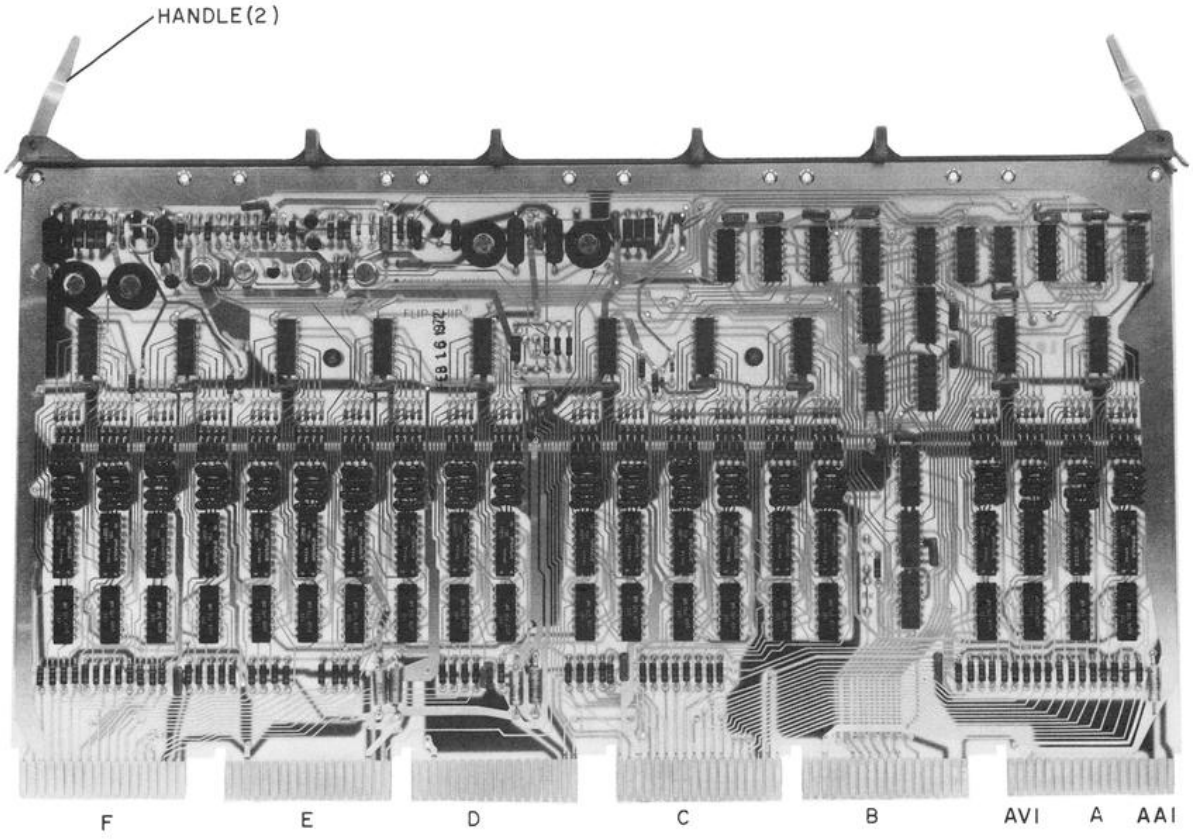


Figure 1-2 Component Side of Driver Module G231

1.2.1 Components Supplied

The MM11-S, MF11-L, and MF11-LP memories comprise the components listed in Table 1-2.

Table 1-2
Components Supplied

MM11-S	MF11-L	MF11-LP
MM11-S Backplane	MF11-L Backplane	MF11-LP Backplane
H214	H214	H215
G110	G110	G109
G231	G231	G231
M920	M920	M7259
Power Connector	Power Connector	M920
Drawings Set	Drawings Set	Power Connector
Diagnostics	Diagnostics	Drawings Set
		Diagnostics

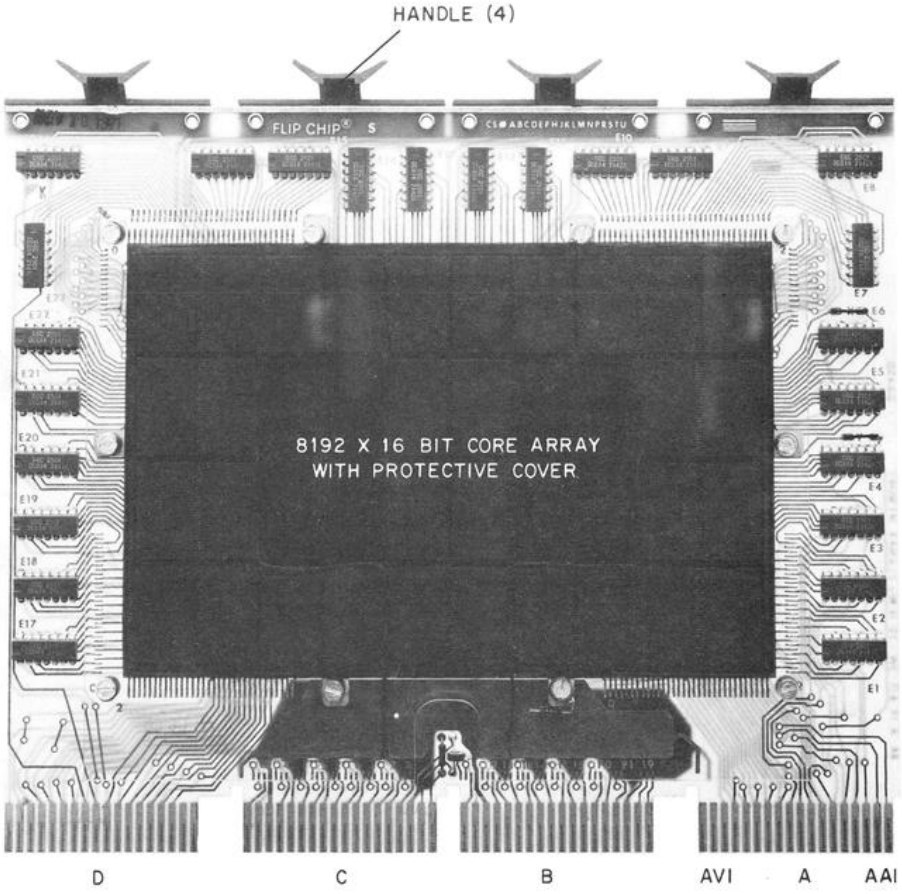


Figure 1-3 Component Side of Stack Module H214

1.3 FUNCTIONAL DESCRIPTION

The following paragraphs contain a functional description of the MM11-L memory. Each module of the MM11-L memory is also described.

1.3.1 Specifications

The general specifications of the MM11-L are listed in Table 1-3.

1.3.2 G110 Control Module

The G110 Control Module contains the memory control circuits, inhibit drivers, sense amplifiers, data register, device selector, threshold circuit, and −5V supply.

a. Memory Control Circuits – Control circuits are provided to acknowledge the request of the master device; determine which of the four basic operations (DATI, DATIP, DATO, or DATOB) is to be performed; and set up the appropriate timing and control logic to perform the desired read or write operation. If a byte operation has been selected, address line A00 L determines the byte to be selected. The actual read or write operation is selected by control lines (C00 and C01). The memory control logic also transfers data to and from the Unibus.

b. Inhibit Driver – Each bit mat contains a single inhibit/sense line that passes through all cores on the mat. To write a 0 into a selected bit, an inhibit current is passed through the inhibit/sense line that cancels the write current in the Y line. The core does not switch so it remains in the 0 state. With no inhibit current, the currents in the X and Y lines switch the core to the 1 state.

c. Sense Amplifiers – During a read operation, the sense amplifier picks up a voltage induced in the sense/inhibit winding when a core is switched from a 1 to a 0. This signal is detected and amplified by the sense amplifier whose output sets a data register flip-flop to store a 1. In effect, a 1 is read but the core is switched to the 0 state. Cores which were previously set to 0 are not affected.

d. Data Register – The data register is a 16-bit flip-flop register used to store the contents of a word after it is destructively read from memory; the same word can then be written back into memory (restored) when in the DATI mode. The register is also used to accept data from the Unibus lines to accommodate the loading of incoming data into the core memory during the DATO or DATOB cycles.

e. Device Selector – The device address is decoded in the device selector to determine if the memory bank has been addressed. Unibus address lines BUS A (17:14) L are used for device selection.

f. Threshold Circuit and –5V Supply – The threshold circuit provides a reference threshold voltage to the sense amplifiers. During a read operation, if the threshold voltage (±20 mV) is exceeded, the sense amplifier produces an output. The –5V supply provides a negative voltage for the sense amplifiers.

1.3.3 G231 Drive Module

The G231 Drive Module contains the address selection logic, switches and drivers, current generator, stack discharge circuit, and DC LO protection circuit.

a. Address Selection Logic – The core memory receives an 18-bit address from the master device. The address is latched and decoded to determine if the memory is the selected device and to determine the core location specifically addressed. If the operation is a byte operation, bus line A00 L indicates the byte to be used. The X and Y portion of the address is decoded through selection switches and a diode matrix to enable passage of read/write current through the selected X and Y drive lines of the memory. The coincidence of these currents selects the specific 16-bit core memory location desired.

b. Switches and Drivers – The switches and drivers direct the flow of current through the magnetic cores to ensure the proper polarity for the desired function. This action is necessary because a single read/write line is used, and the current for a write operation is opposite in polarity to the current required for a read operation. There are separate switches and drivers for the read and write circuits in the selection matrix.

c. Current Generators – X and Y current generators provide the current necessary to change the state of the magnetic cores. The linear rise time and amplitude of the output-current waveform have been selected to provide optimum switching of the core states and maximum signal-to-noise ratio for a wide range of temperatures.

d. Stack Discharge Circuit – The stack discharge circuit maintains the proper stack charge voltage during operation: approximately 0V during a read operation and approximately 14V during a write operation.

e. DC LO Protection Circuit – If any dc voltage is out of tolerance, DC LO L is asserted on the Unibus. It is sensed by the DC LO protection circuit which inhibits the memory operation by opening the –15V line to the current source. This prevents spurious memory operation.

1.3.4 H214 Stack Module

The H214 Stack Module contains the ferrite core array and the X-Y diode matrices. The core array consists of 16 mats, each wired in a 128 x 64 matrix. The stack also contains the resistor-thermistor combination to control the X-Y current generator temperature compensation.

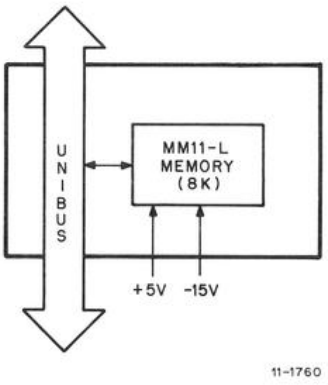
Table 1-3
MM11-L Memory Specifications

Type:	Magnetic core, read/write, coincident current, random access
Organization:	Planar, 3D, 3-wire
Capacity:	8192(8K) words

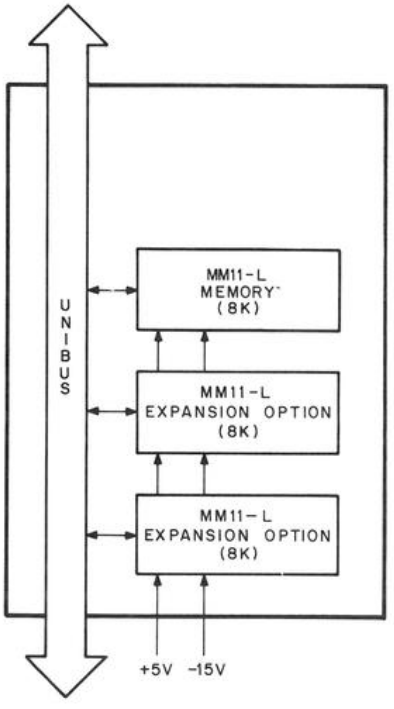
Access Time and Cycle Time:

Bus Mode	Cycle Time		Access Time
	Interleaved	Non-Interleaved	
DATI	650 ns	900 ns	400 ns
DATIP	450 ns	450 ns	400 ns
DATO-DATOB (PAUSE L)	650 ns	900 ns	200 ns
DATO-DATOB (PAUSE H)	450 ns	450 ns	200 ns

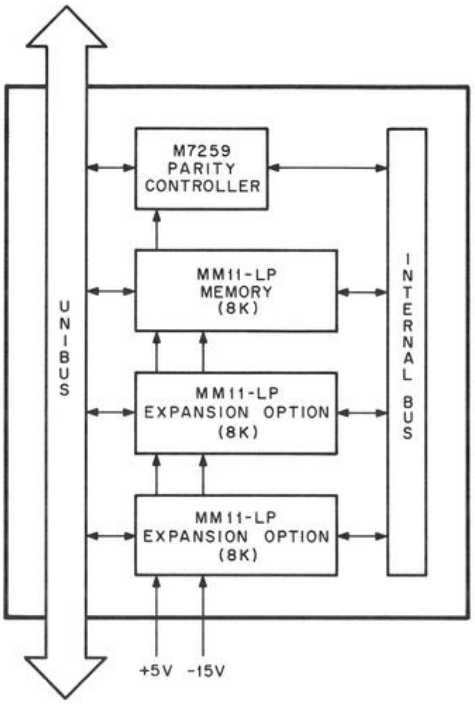
X-Y Current Margins:	±6% @ 0°C, ±7% @ 25°C, ±6% @ 50°C
Strobe Pulse Margins:	±30 ns @ 0°C, ±40 ns @ 25°C, ±30 ns @ 50°C
Voltage Requirements	+5V ±5% with less than 0.05V ripple −15V ±5% with less than 0.05V ripple
Average Current Requirements:	Stand by: +5V: 1.7A −15V: 0.5A Memory Active: +5V: 3.4A −15V: 6.0A
Power Dissipation (Worst Case):	G110 Control Module: ≃ 60W G231 Drive Module: ≃ 40W H214 Stack Module: ≃ 20W Total at maximum repetition rate: 120W
Environment:	
Ambient Temperature:	0°C to 50°C (32°F to 122°F)
Relative Humidity:	0–90% (non-condensing)



(a) MM11-S Memory



(b) MF11-L Memory



(c) MF11-LP Parity Memory

Figure 1-4 MM11-S, MF11-L, and MF11-LP Functional Block Diagram

1.3.5 Basic Memory Operations

The core memory has four basic modes of operation. The main function of the memory is simply to read or write data. Additional modes are provided, however, to allow for byte operation and to eliminate the restore cycle when it is not needed, thereby increasing overall system efficiency. The four basic memory operations are:

a. Read/restore (DATI)
b. Read Pause (DATIP)
c. Write (DATO)
d. Write byte (DATOB)

These four modes are discussed briefly in the following paragraphs.

NOTE

In the following discussions, all operations refer to the master (controlling) device. For example, the term data out indicates data flowing out of the master and into the memory.

1.3.5.1 Data In (DATI) Cycle – The DATI cycle is a read/restore memory cycle. During this operation, the memory reads the information from the selected core location, transfers it to the Unibus, and then writes the information back into the memory location. This last step is necessary because the core memory is a destructive readout device. During the first part of the cycle, the memory loads the data into a register; at tne same time, the memory applies the data to the Unibus. Then, during the second part of the cycle, the memory takes the data from the register and writes it back into the addressed memory location.

1.3.5.2 Data In, Pause (DATIP) Cycle – Normally in reading from memory, the information is destroyed in the particular location accessed, and the data must be restored. However, sometimes it is not actually necessary to restore the information after reading because the location is to have new data written into it. In this instance, eliminating the restore operation decreases the memory cycle time by approximately 50 percent. The DATIP operation is used for this purpose. The data is read from memory and the restore cycle is inhibited. Because no restore cycle is used, a DATIP must always be followed by a write cycle (either DATO or DATOB) on the same address or data in both addresses will be destroyed and the memory controller will hang the Unibus.

1.3.5.3 Data Out (DATO) Cycle – The DATO cycle is a write memory cycle used by the master device to transfer data into core memory. To ensure that proper data is stored, the memory unit must first be cleared by reading the cores (thereby setting them all to zero) before writing in the new data. During a normal DATO, the memory first performs the read operation to clear the cores and then performs a write cycle to transfer data from the bus into the selected core location. If a DATO follows a DATIP (rather than a DATI), the sequence is not the same. The DATIP clears core and generates a pause flag; the DATO skips the read cycle and immediately begins the write cycle. This process reduces DATO cycle time by approximately 50 percent.

1.3.5.4 Data Out, Byte (DATOB) Cycle – The DATOB cycle is similar in function to the DATO cycle, except that during DATOB, data is transferred into the core memory from the bus in byte form rather than as a full word. Actually, an entire word is loaded into the selected memory location: the selected byte which is new data from the bus and the non-selected byte, which is restored data from the word previously stored in that memory location. During the read cycle, the non-selected byte is saved by reading it into the data register while the selected byte is transferred into the register from the Unibus. During the write cycle, only the selected byte portion of the word is loaded into the memory location from the bus. At the same time, the non-selected byte is restored from the data register into the memory location. In effect, the memory is first cleared and then simultaneously performs a restore cycle for the non-selected byte and a write cycle for the selected byte. This mode can follow a DATIP as described above.

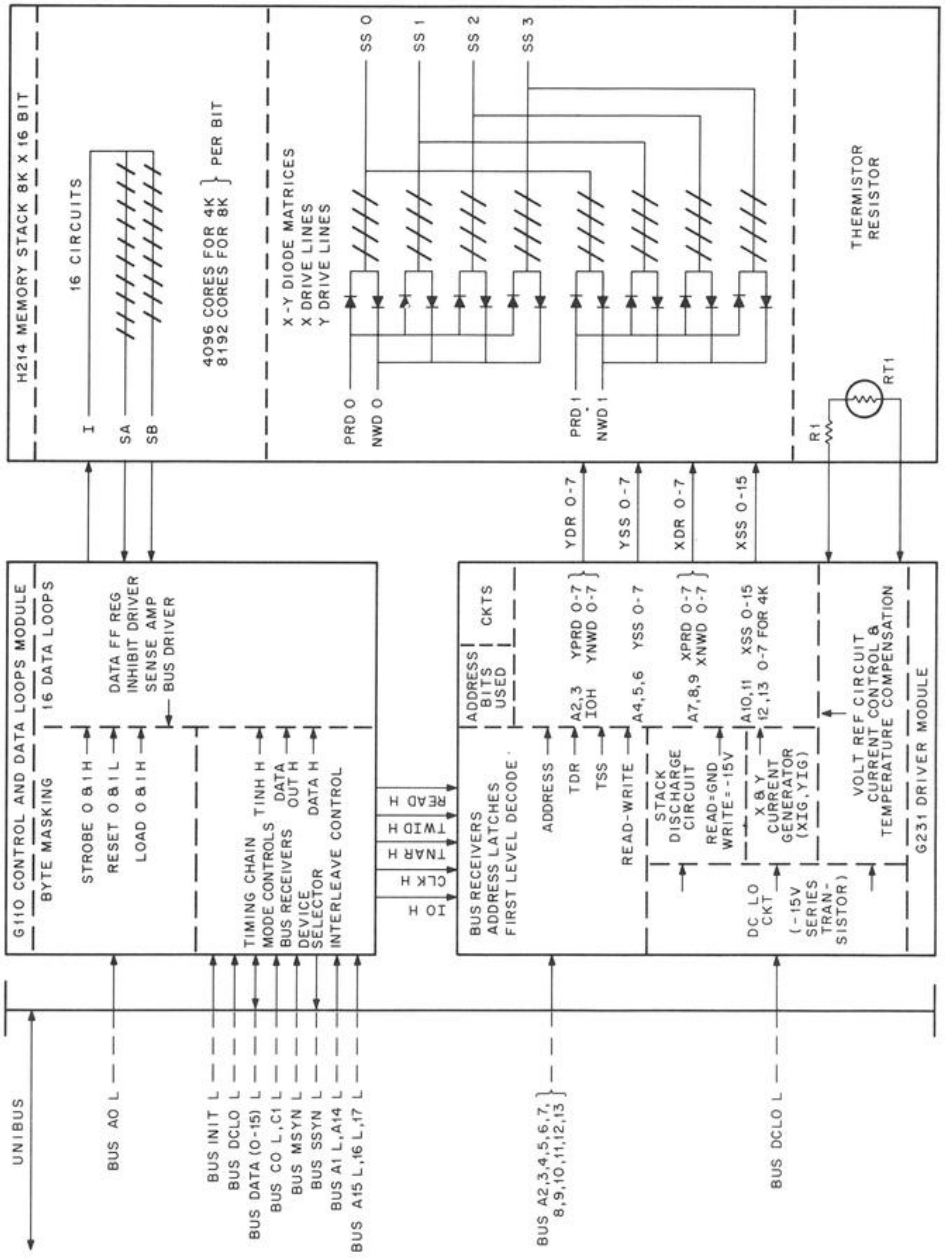


Figure 1-5 MM11-L Memory Block Diagram

CHAPTER 2
DETAILED DESCRIPTION

2.1 INTRODUCTION

This chapter provides a detailed description of the MM11-L memory. The detailed description covers the core array, device and word selection, switches and drivers, current generation, stack discharge circuit, DC LO circuit, sense/inhibit circuitry, control and timing logic, and memory operating cycles.

2.2 CORE ARRAY

The ferrite core memory consists of 16 memory mats arranged in a planar configuration. Each mat contains 8192 ferrite cores arranged in a 128 x 64 array. Each mat represents a single bit position of a word. This planar configuration provides a total of 8192 16-bit word locations. Each ferrite core can assume a stable magnetic state corresponding to either a binary 1 or a binary 0. Even if power is removed from the core, the core retains its state until changed by appropriate control signals. The outside diameter of each core is 18 mil; the inside diameter is approximately 11 mil. Each core is 4.5 mil thick.

Selection and switching of the cores is provided by three wires traversing each core in a special selection technique. An X-axis read/write winding passes through all cores in each horizontal row for all 16 mats. A Y-axis read/write winding passes through all cores in each vertical row for all 16 mats. Through the use of selection circuits which control the current applied to specific X-Y windings, any one of the 8192 word locations can be addressed for writing data into memory or reading data out of memory. A third line passes through each core on a mat to provide the sense/inhibit functions. There is one sense/inhibit line per mat. This single sense/inhibit line, as well as the selection circuits, are discussed in subsequent paragraphs.

2.3 MEMORY OPERATION

Figure 2-1 illustrates a typical portion of the core memory. An X and Y winding pass through each core in the mat. The current passing through any one winding is such that no single winding produces a magnetic field strong enough to cause a core to change its magnetic state. Only the reinforcing magnetic field caused by the coincident current of both an X and a Y winding can cause the core located at the point of intersection to change states. It is this principle that allows the relatively simple winding arrangement to select one and only one memory core out of the possible 8192 contained on each mat. The current passing through either an X or Y winding is referred to as the half-select current.

A half-select current passing through the X3 winding (Figure 2-1) from left to right produces a magnetic field that tends to change all cores in that horizontal row from the 0 to 1 state. The flux produced by the current is, however, insufficient to complete the state transition in any core. Simultaneously passing a half-select current through the Y2 winding from top to bottom produces the same effect on all cores in that particular vertical row.

Note, however, that both currents pass through only one core which is located at the intersection of the X3 and Y2 windings. This is the selected core and the combined current values are sufficient to change the state of the core. The arrows in Figure 2-1 show current direction for the write cycle.

All X and Y windings are arranged in such a manner that whenever a half-select current is passed through each, the resultant magnetic fields combine in the core at the point of intersection. This combined, full-select current ensures that the selected core is left in the binary 1 state. The currents used to select the core are referred to as write currents. A typical hysteresis loop for a core is shown in Figure 2-2.

In the MM11-L Core Memory, the X3 windings in all 16 mats are connected in series as are the Y1 windings. Therefore, whenever a full-select current flows through a selected core on one mat, it also flows through an identical core on the other 15 mats. The X3-Y2 cores on all mats switch to a binary 1, causing each of the 16 cores to become one bit of a 16-bit storage cell.

Because of the serial nature of the X-Y windings, a method must be employed to set certain cores to the 0 state; otherwise, every 16-bit word selected would be all 1s. The method used in the MM11-L Core Memory is to first clear all cores to the 0 state by reading. During the write operation, cores on particular mats are inhibited by an inhibit winding. The inhibited cores remain 0s even when identical cores on other mats are set to 1s.

The half-select current for the inhibit lines is applied from an inhibit current driver, which is a switch and a resistor between the inhibit line and –15V. The current in the inhibit line flows in the opposite direction from the write current in all Y lines and cancels out the write current in any Y line. There is a separate inhibit driver for each memory mat, and each mat represents one bit position of a word; thus, selected bits can be inhibited to produce any combination of binary 1s and 0s desired in the 16-bit word. Remember that the inhibit function is active only during write time.

The sense/inhibit lines are also used to read out information in a selected 16-bit memory cell. The specific core is selected at read time in the same manner as during the write cycle, with one notable exception: the X and Y currents are in the opposite direction. These opposite half-select currents cause all cores previously set to 1 to change to 0; cores previously set to 0 are not affected. Whenever the core changes from 1 to 0, the flux change induces a current in the sense winding of that mat. This current is detected and amplified by a sense amplifier. The amplifier output is strobed into the data register for eventual transfer to the Unibus.

Figure 2-3 shows a 16-word by 4-bit planar memory. The MM11-L Core Memory functions in the same manner except that it has 128 X lines, 64 Y lines, and 16 core mats. The core stringing is identical, and the sense windings are strung through all 8192 cores with the interchange between X63 and X64, instead of between X1 and X2.

2.4 DEVICE AND WORD SELECTION

2.4.1 Introduction

When the processor or a peripheral device desires to perform a transaction with the memory, the processor asserts an 18-bit address on Unibus address lines A⟨17:00⟩. Four of these 18 bits indicate the address of the memory as a device. Bits A⟨17:14⟩ are used for non-interleaved operation and bits A01 and A⟨17:15⟩ are used for interleaved operation. Thirteen bits A⟨13:01⟩ indicate the address of a specific word within the memory. Address bit A00 is used to select the byte (8 bits) transaction when in the DATOB mode.

The memory address is decoded by the device selection circuit on the G110 Control Module. The word address is stored in a register on the G231 Driver Module whose output is decoded to activate the X-Y line switches and drivers that select the addressed word. These circuits contain jumpers that are included or excluded to configure the memory as follows: establish a specific device address; and select interleaved or non-interleaved operation.

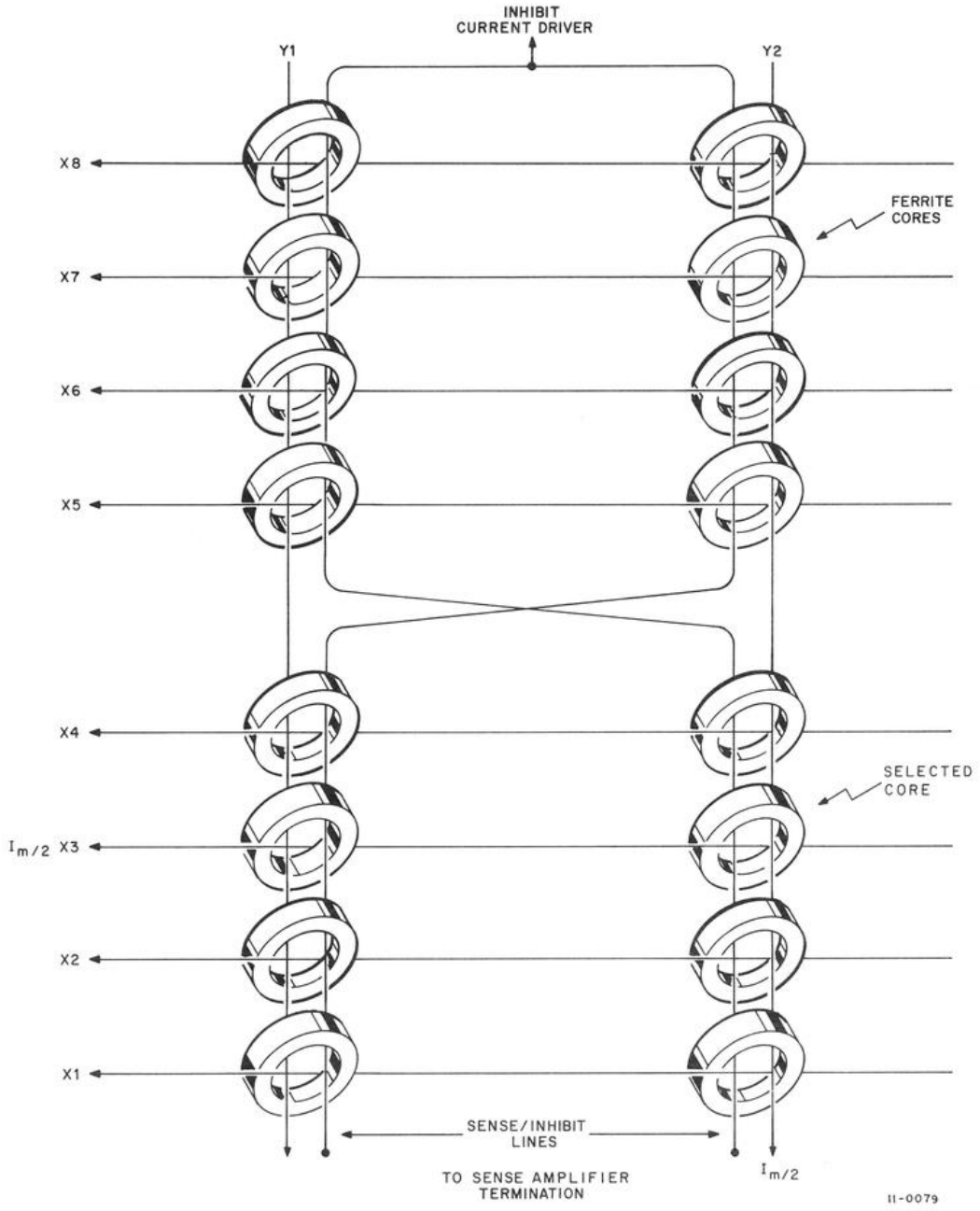


Figure 2-1 Three-Wire Memory Configuration

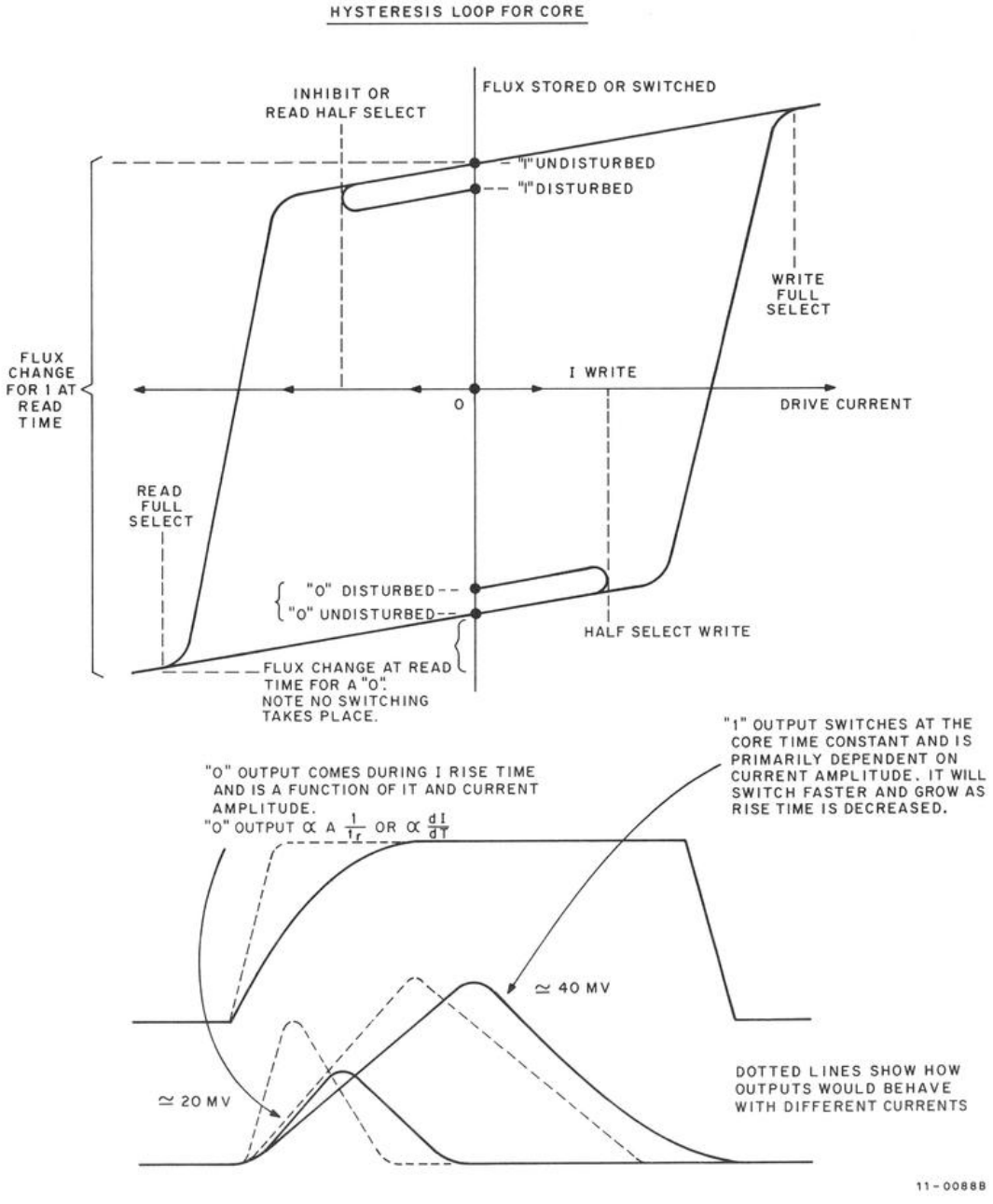


Figure 2-2 Hysteresis Loop for Core

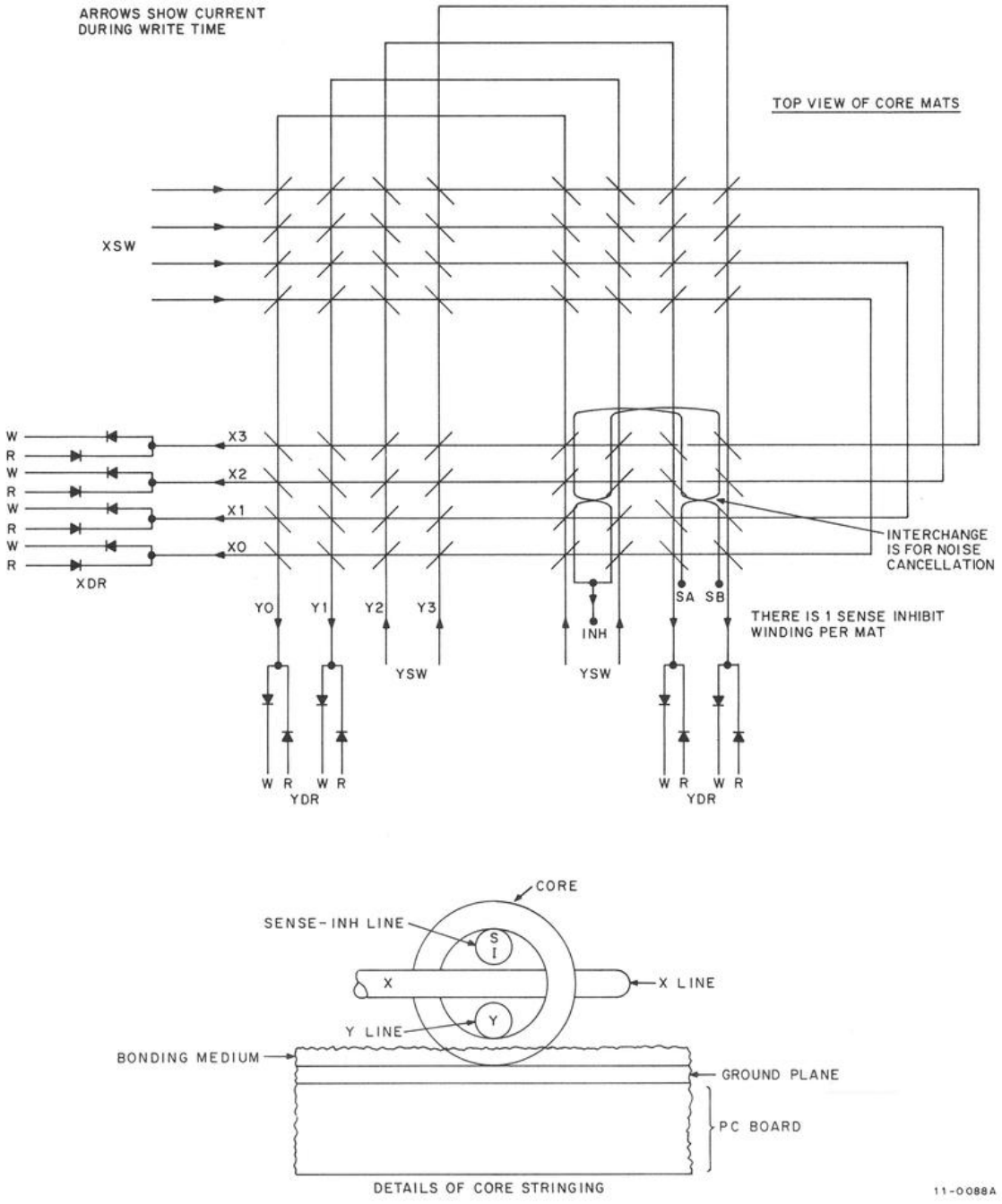


Figure 2-3 Three-Wire 3D Memory,
Four Mats Shown for a 16-Word by 4-Bit Memory

Table 2-1 lists the function of each address bit. Figure 2-4 is a simplified block diagram of the device and word address selection circuits.

Table 2-1
Addressing Functions

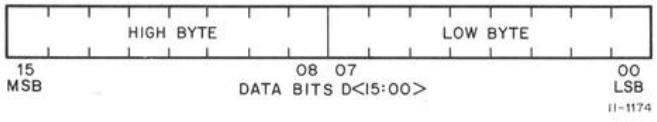
Bus Address	Function
A00	Controls Byte Mode
A01	Non-Interleaved Mode: Becomes A01H to G231 Interleaved Mode: Goes to Device Selector
A02, A03, A01H*	Decode Y Drivers
A04, A05, A06	Decode Y Switches
A07, A08, A09	Decode X Drivers
A10, A11, A12	Decode X Switches
A14	Non-Interleaved Mode: Goes to Device Selector Interleaved Mode: Becomes A01H to G231
A15, A16, A17	Goes to Device Selector

*A01H is not a Unibus signal.

2.4.2 Memory Organization and Addressing Conventions

Prior to a detailed discussion of the address selection logic, it is desirable to understand memory organization and addressing conventions.

The memory is organized in 16-bit words each consisting of two 8-bit bytes. The bytes are identified as low and high as shown below.



DATA BITS D⟨15:00⟩

Each byte is addressable and has its own address location; low bytes are even numbered and high bytes are odd numbered. Words are addressed at even-numbered locations only; the high (odd) byte is automatically included.

For example, an 8K word memory has 8,192 words or 16,384 bytes; therefore, 16,384 locations are assigned. The address locations are specified as 6-digit octal numbers. The 16, 384 locations are designated 000000 through 037777 as shown in Figure 2-5.

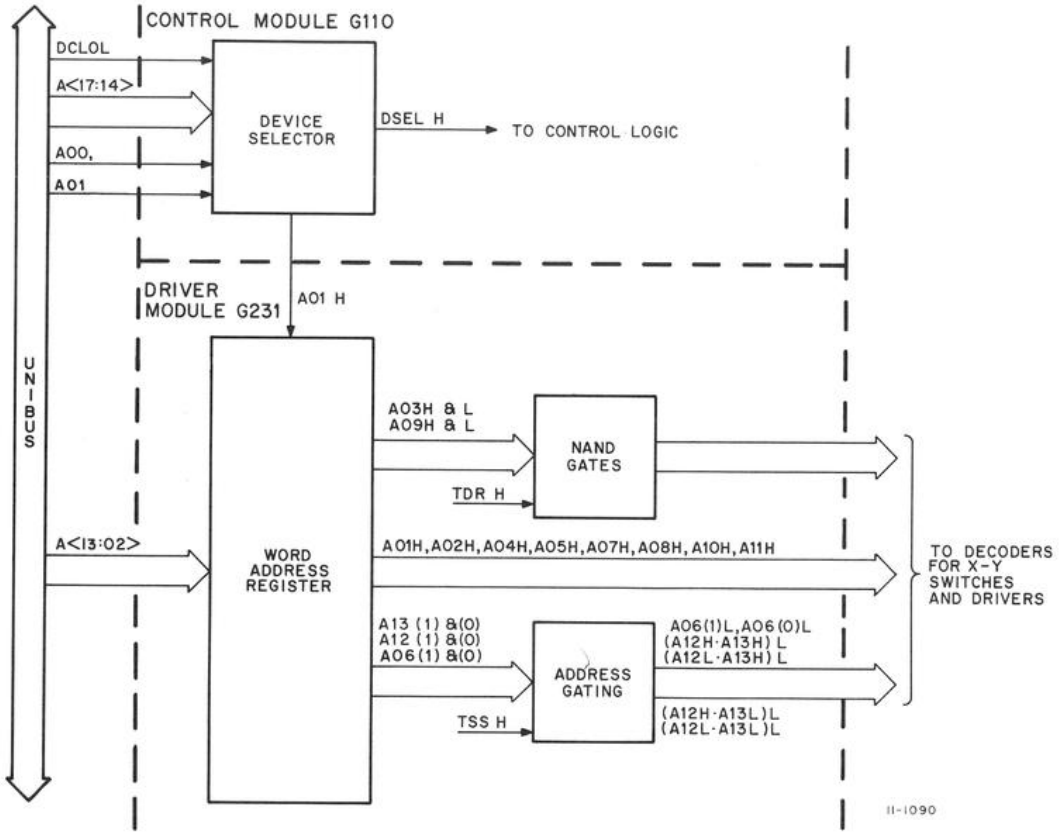


Figure 2-4 Device and Word Address Selection Logic, Block Diagram

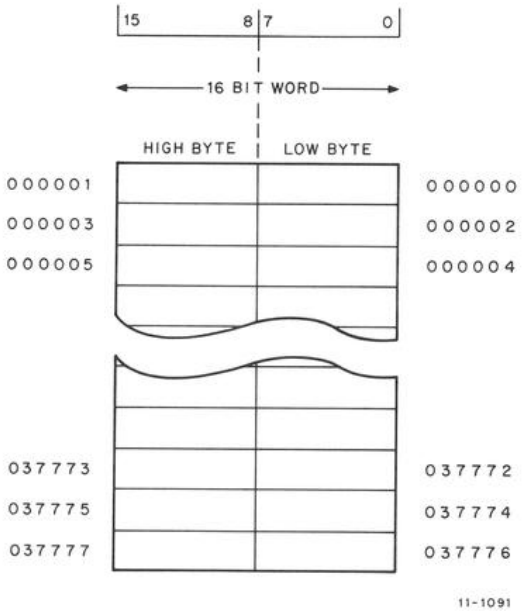


Figure 2-5 Memory Organization

The address selection logic responds to the binary equivalent of the octal address. The binary equivalent of 017772 is shown below as an example.

ADDRESS BITS A<17:00>

17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00	BIT POSITION
0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	0	1	0	BINARY
0			1			7			7			7			2			OCTAL

11-1173

Each memory bank requires its own unique device address. For example, assume that a system contains three 8K memory banks as shown in Figure 2-6. The device selector for the 8K non-interleaved memory decodes four address lines (A<17:14>). Examination of the binary states of these lines for the three memory banks shows that the changes in the states of bits A14 and A15 allow the selection of a unique combination for each bank. The combination, which is the device address, is hardware selected by jumpers in the device selector.

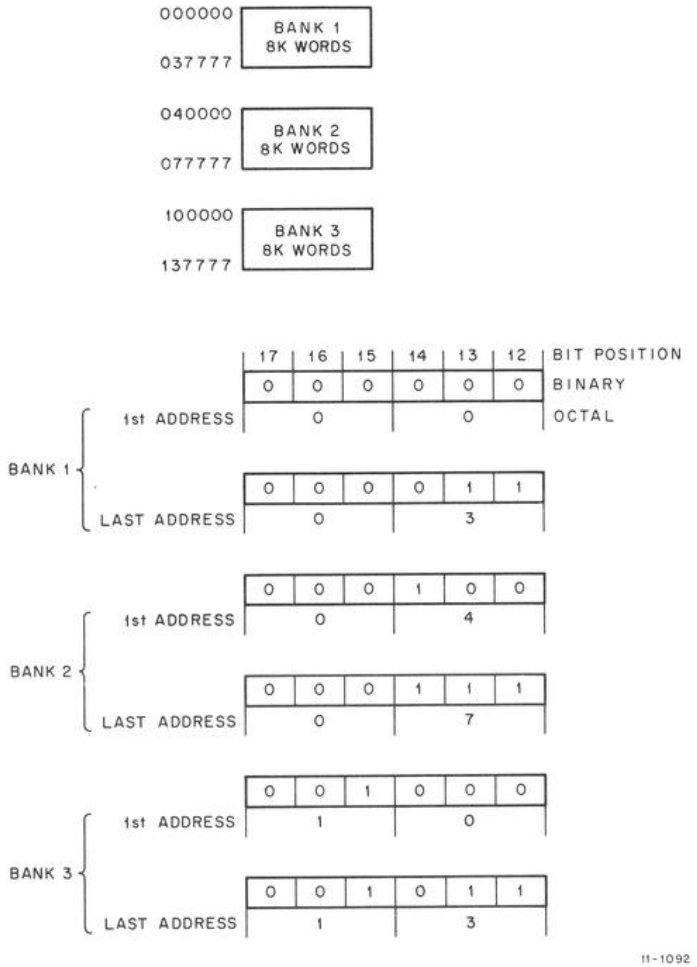


Figure 2-6 Address Assignments for Three Banks of 8K Words Each

2.4.3 Device Selector

The device selector is located on the control module; Drawing G110-0-1, sheet 2 shows a logic diagram of the device selector in the 4K configuration.

Address bits A01 and A⟨17:14⟩ are decoded in the device selector to provide the device selection signal D SEL H that is used in the control logic. Two combinations of these bits are decoded depending on the memory configuration as shown below.

Memory Configuration	Address Bits
8K Words (non-interleaved)	A ⟨17:14⟩
8K Words (interleaved)	A01 and A⟨17:15⟩

The control module is used for both 4K and 8K memories; therefore, two jumpers (W9 and W10) are provided to include or exclude address bit A13 commensurate with the memory word size. Two jumpers (J3 and J4) on the driver module (Drawing G231-0-1, sheet 2) are provided for A13 inclusion or exclusion in the word addressing logic. The same driver module is used for both memory capacities. Two jumpers (W7 and W8) in the device selection logic on the control module are used to select interleaved or non-interleaved operation of the 8K memory.

Each memory bank must have its own unique device address. Four jumpers (W2, W3, W4, and W6) in the device selector provide this capability. In Drawing G110-0-1, sheet 2, all the jumpers are shown in place and the device selector would respond only when high signals appear on the Unibus address lines A⟨17:14⟩. Some jumpers can be removed to allow the device selector to respond to a particular combination of high and low signals on these address lines.

All highs at the inputs of the 7380 Unibus receivers (E12 and E23) give lows at their outputs. Each receiver output goes to one input of a type 8242 Exclusive-NOR gate. Because the jumpers W7 and W8, only bit A01 or A14 is decoded for a given configuration. As shown, the jumpers are set for 4K and bit A14 is decoded. An additional receiver is used to sense BUS DC LO L and its output (E23 pin 14) is sent to an 8242 gate (E24 pin 5). BUS DC LO L is asserted only when the dc voltages from the power supply drop below specified limits.

The other input of the 8242 gates associated with bits A01 or A14, A13, A15, A16, and A17 can be connected to +5V or ground, depending on whether or not jumpers W2 through W6 are installed. The input is low (ground) with the jumper in; with the jumper removed, the input is high (+5V). Each 8242 gate is used as a digital comparator: its output is high only when both inputs are identical. The 8242 gates have open collectors and they are connected in common; therefore, the comparator output D SEL H is high only when all gates detect matched inputs (both lows or both highs).

An installed jumper requires a low signal at the output 7380 Unibus receiver. The 7380 is connected as an inverter so this signal is reflected as a high on the Unibus (logical 0 or asserted state for the Unibus). To configure the jumpers for a specific device address, find the binary equivalent of the assigned octal address and insert a jumper in each bit position that contains a 0. A specific jumper configuration is shown in Figure 2-7.

In the 8K non-interleaved memory configuration, jumper W9 is removed and W10 is installed. This removes bit A13 from the input of Unibus receiver E12 in G110 and replaces it with +5V via resistor R107. This receiver output (pin 14) always remains 0 so that jumper W5 must remain installed to ensure a match on pins 12 and 13 of gate E13. In the 8K interleaved memory configuration, one more change must be made. Jumpers W7 and W8 must be connected in the "X" pattern shown by dotted lines in Drawing G110-0-1, sheet 2. Bit A01 is now decoded by the device selector and bit A14 is sent via jumper W7 to the word address register as A01H. The jumper configurations for memory systems up to 128K words are shown in Figure 2-8.

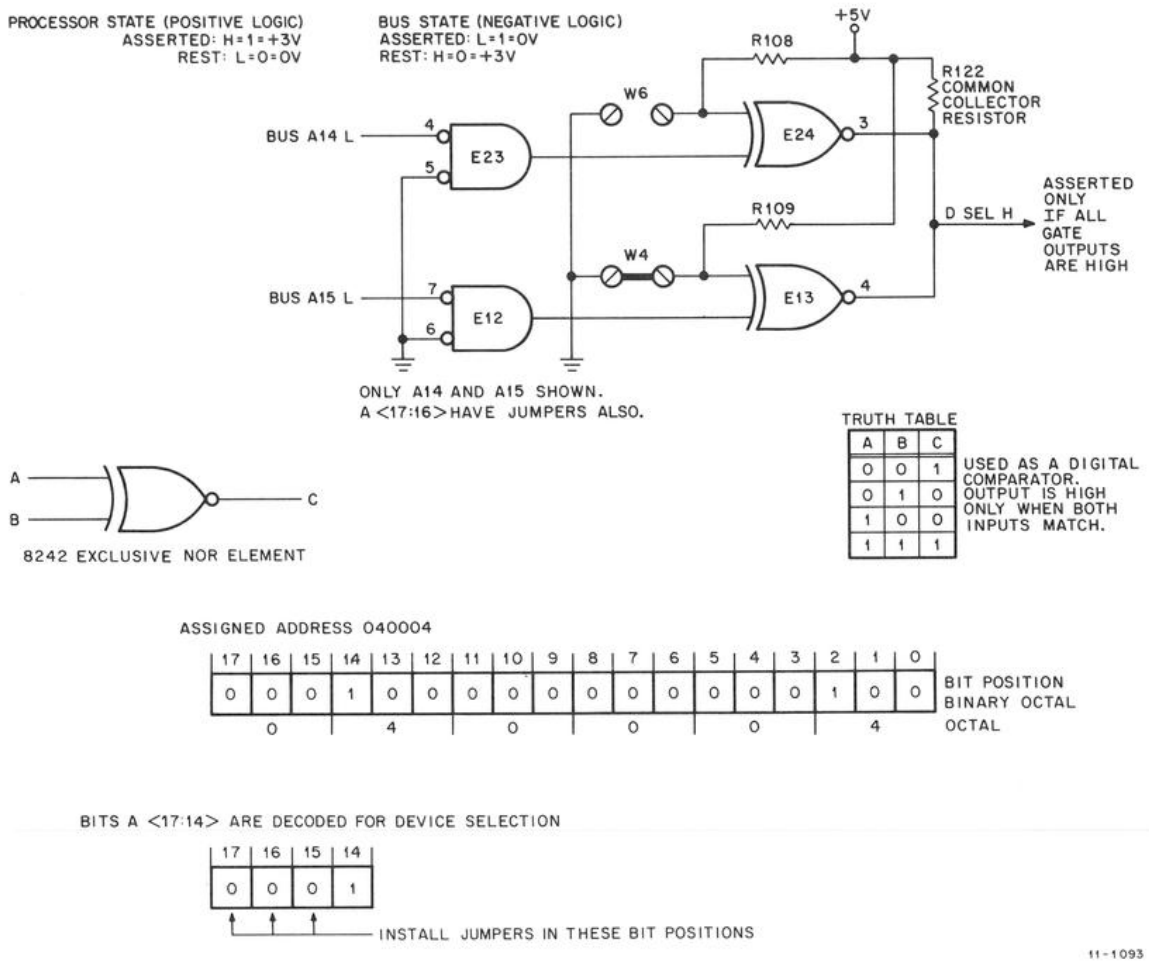


Figure 2-7 Jumper Configuration for a Specific Memory Address

2.4.4 Word Selection

Word selection requires two levels of decoding. The word address bits are placed in the 13-bit word address register; some bits from the register output are combined in a gating network. The outputs from the gating network and some outputs directly from the register are used as inputs to a group of decoders (Figure 2-4). The outputs of the decoders select the proper X and Y read/write switches and drivers.

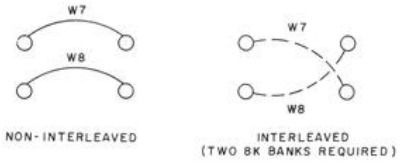
2.4.4.1 Word Address Register and Gating Logic – The word address register and gating logic are contained on the driver module. The circuit schematic is shown in drawing G231-0-1, sheet 2. The register is composed of 13 dual 74H74 D-type edge-triggered flip-flops. They are identified as E11, E12, E13, E14, E18, E19, and E20. The output (pin 3) of gate E9 provides a high signal on the present input (pin 4 or pin 10) of each flip-flop which prevents direct presetting of the flip-flop. Direct clearing of each flip-flop is prevented by a high signal on the clear input (pin 1 or pin 13) via the output (pin 2) of gate E9. The register cannot be directly cleared or preset; its output responds only to the signal at its data (D) input.

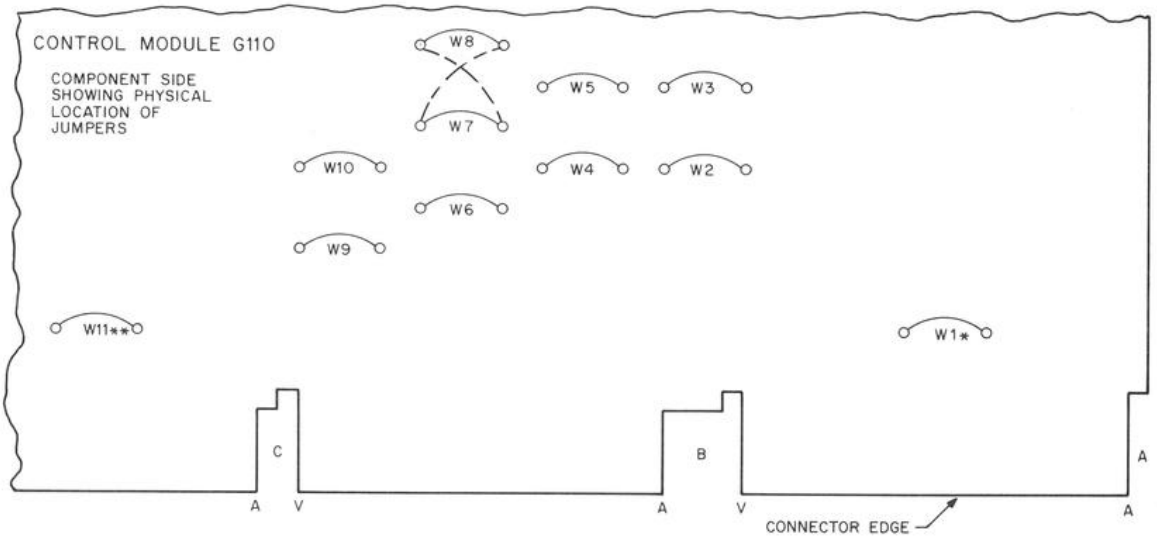
Memory Bank (words)	Machine Address (words)	Device Address Jumpers (1)			
		W6 A14 or A01 (2)	W4 A15	W3 A16	W2 A17L
0–8K	000000–037776	In	In	In	In
8–16K	040000–077776	Out	In	In	In
16–24K	100000–137776	In	Out	In	In
24–32K	140000–177776	Out	Out	In	In
32–40K	200000–237776	In	In	Out	In
40–48K	240000–277776	Out	In	Out	In
48–56K	300000–337776	In	Out	Out	In
56–64K	340000–377776	Out	Out	Out	In
64–72K	400000–437776	In	In	In	Out
72–80K	440000–477776	Out	In	In	Out
80–88K	500000–537776	In	Out	In	Out
88–96K	540000–577776	Out	Out	In	Out
96–104K	600000–637776	In	In	Out	Out
104–112K	640000–677776	Out	In	Out	Out
112–120K	700000–737776	In	Out	Out	Out
120–128K	74000–777776	Out	Out	Out	Out

(1) W5 and W10 must be installed and W9 must be removed.

(2) The memory can be interleaved as 16K only, using two adjacent contiguously addressed 8K banks. When two 8K banks are interleaved, jumpers W7 and W8 must be in the configuration shown by the dotted lines. Bit A01 goes to the device selector gate controlled by jumper W6. One 8K bank must have W6 installed and the other must have W6 removed.

When not interleaved, jumpers W7 and W8 must be in the configuration shown by the solid lines. Bit A14 goes to the device selector gate controlled by jumper W6.





*Jumper W1 is for test purposes only. It must be installed for normal operation.

**Jumper W11 should be removed for normal operation. When installed the memory responds to DATI only, regardless of state of control lines C00 and C01.

NOTE:
Jumpers W5, W7, and W8 must remain in the factory installed positions.

11-1149

Figure 2-8 Device Decoding Guide

Address bits A⟨13:02⟩ are picked off the Unibus via type 7380 quad receivers (E15, E16, and E17). The receiver outputs are sent to the corresponding flip-flop D-inputs. The 8K memory requires J4 in and J3 out.

The flip-flop (E11) associated with bit A01 receives its input from the device selector (Drawing G110-0-1, sheet 2). The input signal is A01H which is obtained from bit A01 Unibus receiver for an 8K non-interleaved memory. For an 8K interleaved memory, A01H is obtained from bit A14 Unibus receiver, and the A01 Unibus receiver output goes to the device selector.

The register flip-flops are clocked synchronously by CLK 1 H from the control logic (Drawing G110-0-1, sheet 2). Clocking occurs on the positive-going edge of CLK 1 H. The generation and timing of this clock signal is discussed in Paragraph 2.8. When the register is clocked, the outputs of flip-flops A01, A02, A04, A05, A07, A08, A10, and A11 are sent to the type 8251 X-Y line decoders on the driver module (Drawing G231-0-1, sheets 3 and 4). The outputs of flip-flops A06, A12, and A13 are combined in a group of six type 74H10 NAND gates (three E22s and three E25s) which are enabled by signal TSS H. Table 2-2 lists the states of flip-flops A06, A12, and A13 that are required to enable these gates. The outputs of flip-flops A03 and A09 are gated with TDR H in high-speed 2-input NAND gates and then applied to the decoders associated with the drivers. The six signals listed in Table 2-2 are also sent to the X-Y line decoders on the driver module.

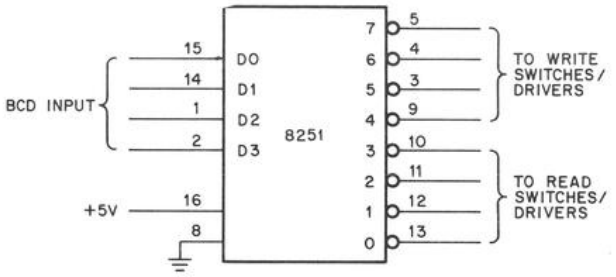
Table 2-2
Enabling Signals for Word Register Gating

Output Signals		Enabling Signals		
Gate	**Asserted Signal**	**FF A06**	**FF A12**	**FF A13**
E22 pin 12	(A06H) L	Set	X	X
E22 pin 8	A06L	Reset	X	X
E22 pin 6	(A12H · A13H) L	X	Set	Set
E25 pin 12	(A12L · A13H) L	X	Reset	Set
E25 pin 8	(A12H · A13L) L	X	Set	Reset
E25 pin 6	(A12L · A13L) L	X	Reset	Reset

TSS H is generated at the output (pin 3) of negative-input OR gate E4 during a read or write operation. During a read operation, the enabling signal is produced at NAND gate E4, pin 8 by ANDing READ H and TNAR H. During a write operation, the enabling signal is produced at NAND gate E4, pin 6 by ANDing WRITE H and TWID H. READ, TNAR, and TWID are generated by the control logic on the control module. WRITE is the complement of READ (produced by inverter E6). READ H comes from the 1 output of R/W flip-flop E13 (Drawing G110-0-1, sheet 2); READ H is produced when the flip-flop is set. When the R/W flip-flop is cleared, READ H is low and it is inverted by E6 to produce WRITE H.

2.4.4.2 X and Y Line Decoding

The basic decoding unit is a type 8251 BCD-to-Decimal Decoder. It converts a 4-bit BCD input code to a one-of-ten output; however, only eight outputs are used. Figure 2-9 shows an 8251 and associated truth table. The inputs are D0, D1, D2, and D3; they are weighted 1, 2, 4, and 8, with D0 being the least significant bit. The outputs are 0-7 and are mutually exclusive. The selected output is low and all others are high.



TRUTH TABLE

INPUTS				OUTPUTS							
D3	D2	D1	D0	0	1	2	3	4	5	6	7
0	0	0	0	0	1	1	1	1	1	1	1
0	0	0	1	1	0	1	1	1	1	1	1
0	0	1	0	1	1	0	1	1	1	1	1
0	0	1	1	1	1	1	0	1	1	1	1
0	1	0	0	1	1	1	1	0	1	1	1
0	1	0	1	1	1	1	1	1	0	1	1
0	1	1	0	1	1	1	1	1	1	0	1
0	1	1	1	1	1	1	1	1	1	1	0
1	X	X	X	1	1	1	1	1	1	1	1

X = IRRELEVANT
0 = LOW
1 = HIGH

11-1095

Figure 2-9 Type 8251 Decoder, Pin Designation and Truth Table

In the MM11-S memory, 10 decoders are used: 6 for the X-axis and 4 for the Y-axis. Each decoder controls four read/write switch pairs. Each pair is associated with a specific switch or driver. This switch matrix is combined with the stack X-Y diode matrix to allow selection of any location out of the total 8192 locations (see stack drawing DCS-H214-0-1 for interconnections).

The X and Y line switches are first differentiated as switches and drivers. The drivers are those switches that are connected to the diode end of the stack. Drivers and switches are further differentiated by function: either read or write. Another differentiation is made by polarity: negative or positive, depending on the physical connection. Read drivers and write switches are connected to the current generator outputs and are considered positive; write drivers and read switches are connected to –15V and are considered negative.

Figure 2-10 shows the decoders associated with Y line read and write switches 4-7 and Y line read and write drivers 4-7. Also refer to the truth table in Figure 2-9. In both decoders (E28 for switches and E8 for drivers), the signal to input D3 selects the block of switch pairs. This signal must be low for any output to be selected. The signal to input D2, which is READ L for all decoders, controls the selection of read or write switches/drivers.

When READ L is low, outputs 0-3 are selected; these are read switches and read drivers. When READ L is high, outputs 4-7 are selected; these are write switches and write drivers. The four combinations of the states of inputs D0 and D1 select the particular switch/driver.

The four driver decoders (E3, E8, E43, and E46 in Drawing G231-0-1, sheets 3 and 4) have a NAND gate connected to input D3. Signal TDR H is an input to each gate; therefore, the driver decoders cannot be enabled unless TDR H is high. This signal is generated on the driver module (Drawing G231-0-1, sheet 2, coordinates A-8) by ANDing TWID H and READ H or TNAR H and WRITE H.

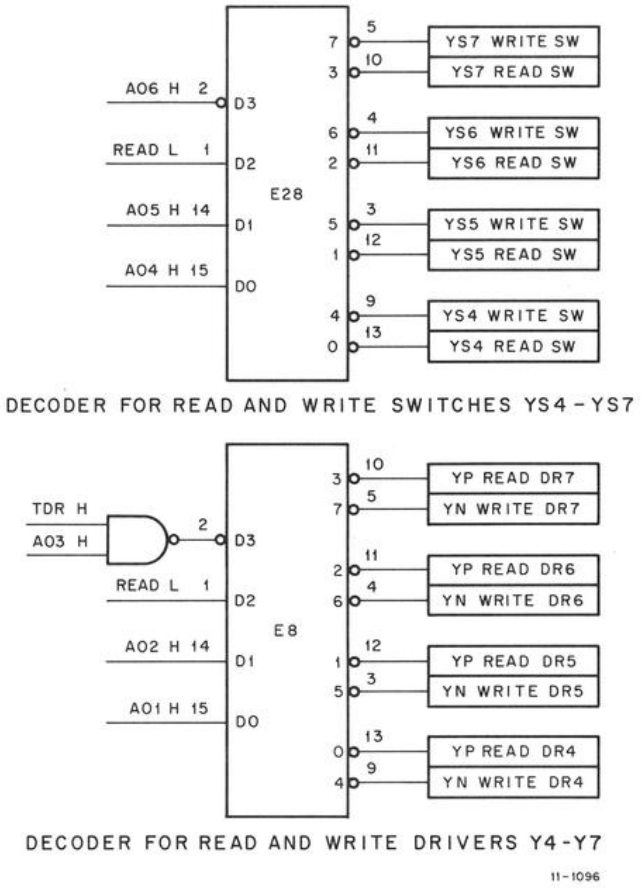


Figure 2-10 Decoding of Read/Write Switches and Drivers Y4-Y7

Each switch/driver is connected to the decoder output by means of a transformer-coupled base drive circuit. When the decoder output is at ground (low), the switch/driver is turned on; it is turned off when the decoder output is at +3.5V (high). The base drive circuit for write switch YS7 shown in Figure 2-11 is typical.

In this example, the decoder inputs have selected output 7 which is at ground. Current i_1 flows into this decoder output circuit from the +5V supply via resistor R11 and the primary winding (terminals 4 and 3) of transformer T8. The value of i_1 is determined by the value of R11 and the voltage reflected into the transformer primary (approximately 1.0V). An equal current i_2 is induced in the base-emitter circuit of write-switch E29 which is connected to the transformer secondary winding (terminals 13 and 14). This current turns on E29. All the base current for E29 is provided by this circuit; i_3 is the collector current. When the decoder is turned off, its output pull-up transistor tries to drive the turn-off current i_4 in the opposite direction. This reverse current removes the forward bias from the base of E29 and turns it off. Capacitor C30 allows the decoder to pump reverse current i_4 into the transformer primary; it also speeds up turn-on current i_1. Diode D1 prevents reverse breakdown of the base-emitter junction of E29; it also protects the decoder output.

2.4.4.3 Drivers and Switches – Drivers and switches direct the current through the X and Y lines in the proper direction as selected by the read and write operations.

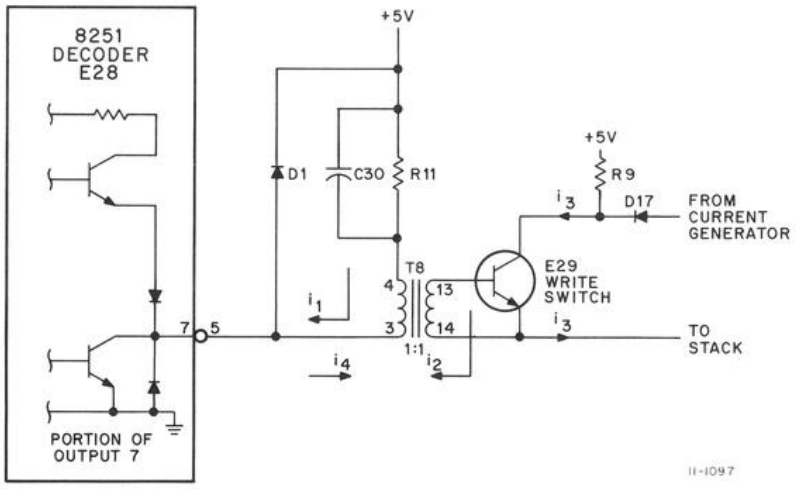


Figure 2-11 Switch or Driver Base Drive Circuit

In the MM11-L memory, 16 pairs of read/write switches and 8 pairs of read/write drivers are provided in the X-axis; 8 pairs of read/write switches and 8 pairs of read/write drivers are provided in the Y-axis. In conjunction with the stack diode matrix (Drawing H214-0-1, sheet 2), one driver and any one of 16 switches select 8 lines in the Y-axis. This allows selection of 128 lines in the X-axis and 64 lines in the Y-axis. This provides a 128 x 64 matrix that selects any location out of 8192 locations.

Figure 2-12 illustrates one-fourth of a Y selection matrix and shows the interconnection of the diodes and the lines from the switches and drivers. It shows how 4 pairs of switches and drivers are connected to select 16 locations. Refer to Drawing H213-0-1, sheet 2 for an extension of this method which uses 8 pairs of switches and drivers to select 64 locations.

Figure 2-12 shows four pairs of drivers and four pairs of switches for the Y-axis only; polarities are shown for convenience. The diodes are identified to assist in associating them with the drivers and switches. Each line from a twin diode interconnection to a read/write switch pair passes through 64 cores and represents one line on each bit mat. Assume that a write operation is to be performed and the word address decoders have selected write switch WYS00 and write driver YNWD1. The Y current generator sends current through write switch WYS00 (conventional flow) which puts a positive voltage on the anodes of diodes 03W, 02W, 01W, and 00W. The non-selected write drivers (YNWD3, YNWD2, and YNWD0) provide a positive voltage on the cathodes of their associated diodes (03W, 02W, and 00W respectively) which reverse biases them and prevents conduction. Write driver YNWD1, which has been selected, turns on and makes the cathode of diode 01W negative with respect to the anode which forward biases it. The diode conducts and allows current to flow to write driver YNWD1. A half-select current now flows through this line that links 64 cores per bit mat (1024 total for 16 mats).

Figure 2-13 is a simplified schematic of two pairs of switches and drivers interconnected with the core stack and current generator. Read/write switches YS07 and read/write drivers YD7 are used as examples. These switches and drivers are chosen for convenience. For a read or write operation, there are 64 switch/driver combinations on the Y axis and 128 on the X axis. For a read operation, decoder E8 selects positive read driver E7 via transformer T3, and decoder E28 selects negative read switch E26 via transformer T7. Both E7 and E28 are turned on when they are selected. E7 conducts and removes the reverse bias on diode D67 which allows current from the Y current generator to flow through D67, E7, the associated matrix diode, and the cores on the selected line. After passing through the cores, the current flows through E26 and R27 to the -15V line. For a write

operation, decoder E28 selects positive write switch E29 via transformer T8, and decoder E8 selects negative write drivers E10 via transformer T4. Both E29 and E10 are turned on. E29 conducts and removes the reverse bias on diode D17 which allows current from the Y current generator to flow through D17, E29, and the cores in the opposite direction. After passing through the cores, the current flows through the associated matrix diode E10, and R140 to the -15V line. Read current flow is shown as a solid line: a broken line shows write current flow.

2.4.4.4 Word Address Decoding and Selection Sequence – This paragraph takes a specific word address through the decoding and X and Y line selection sequence.

The word address is 017772 and it is assumed that a specific memory bank has been selected. The binary equivalent of the address is shown below. A read operation is to be performed.

ADDRESS BITS A<17:00>

17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00	BIT POSITION
0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	0	1	0	BINARY
0			1			7			7			7			2			OCTAL

11-1173

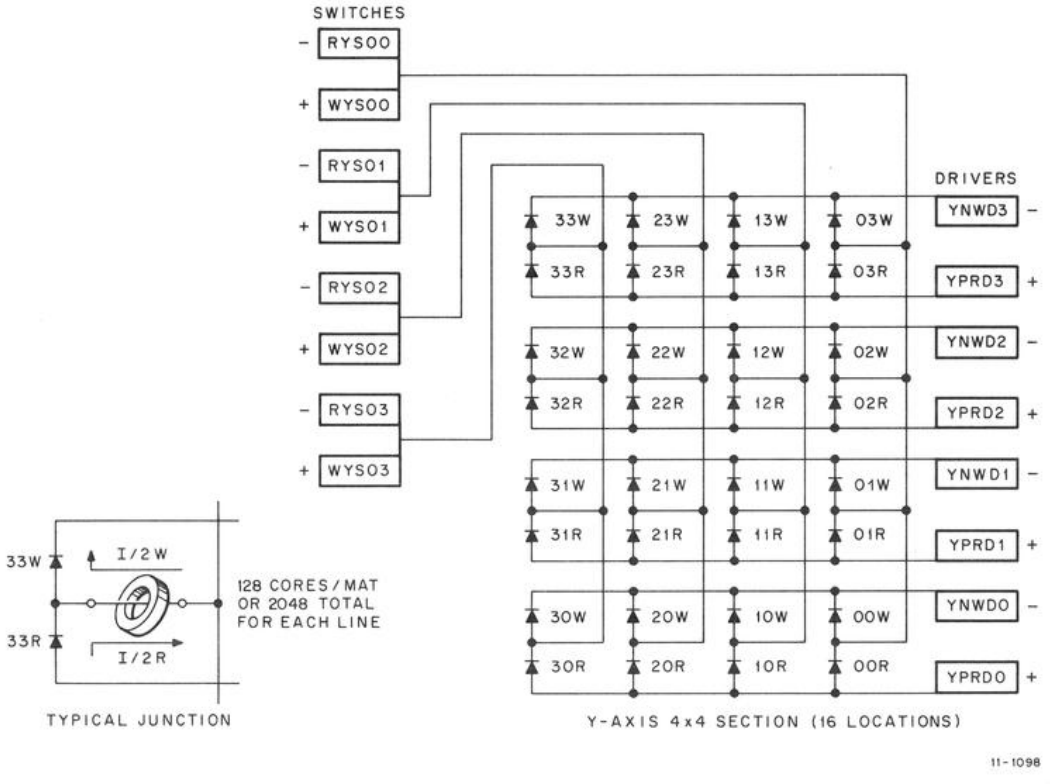


Figure 2-12 Y Line Selection Stack Diode Matrix

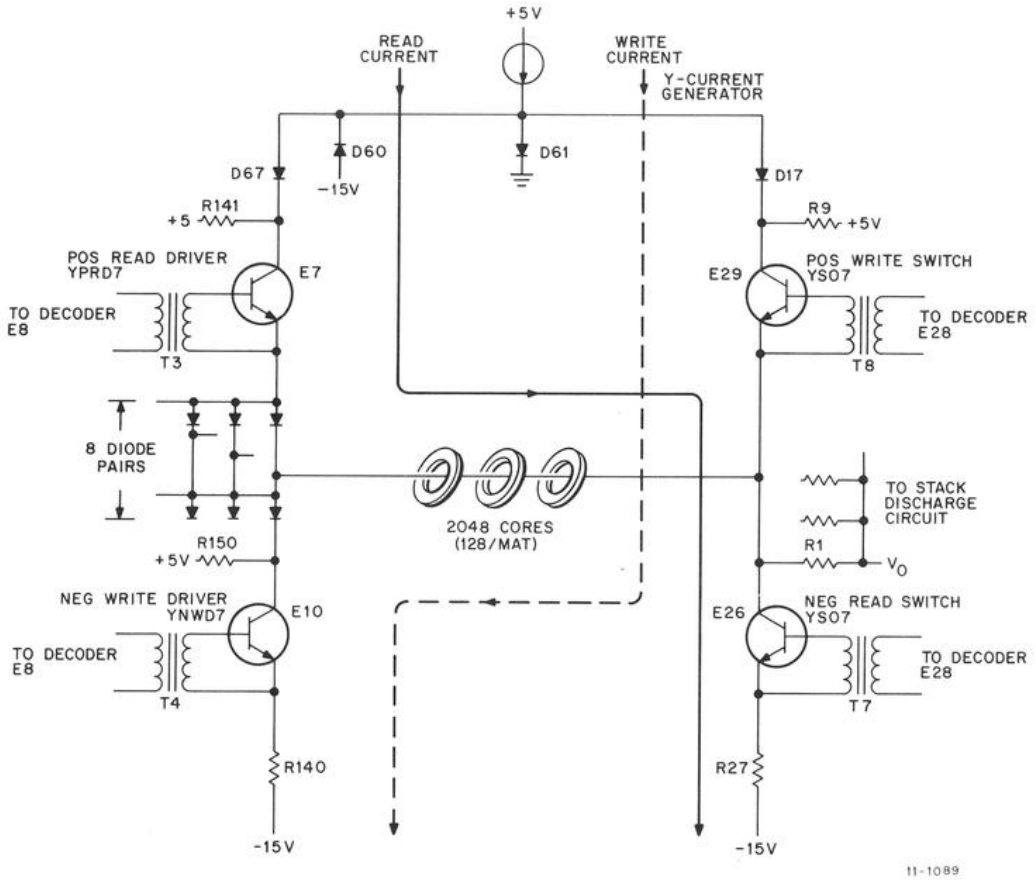


Figure 2-13 Typical Y Line Read/Write Switches and Drivers

Bits A⟨13:01⟩ are used to decode the word address. Bit A01 is sent to the device selector (Drawing G110-0-1, sheet 2) and appears at word address flip-flop E11 pin 2 as A01 H (Drawing G231-0-1, sheet 2). Bits A⟨13:01⟩ are sent to the Unibus receivers which are inputs to the associated word address flip-flops. J3 is out and J4 is in. Table 2-3 shows the state of bits A⟨13:01⟩ and the decoding signals generated by the word address flip-flops after they are clocked.

The output signals from flip-flops A06, A12, and A13 are not used directly from the flip-flops. They are sent to gating logic (E22 and E25) and are ANDed with signal TSS H. In this case, only two out of a possible six signals are generated: A06 H is low from E22 pin 12 and (A12H · A13L) L is low from E25 pin 8. These signals and the outputs from the other word address flip-flops are sent to the inputs of the type 8251 decoders to select the appropriate switches and drivers. READ L is an input to each 8251 decoder. A read operation is to be performed; therefore, READ L is low.

The decoders, switches, and drivers are shown in Drawing G231-0-1, sheets 3 and 4. Using the decoding signals in Table 2-3 and the operating characteristics of the decoders, it is possible to determine which decoders have been selected for word address 017772. A decoder is selected only when its D3 input is low. In this case, the selected decoders are E34 and E46 for the X line (Drawing G231-0-1, sheet 3), and E28 and E8 for the Y line (Drawing G231-0-1, sheet 4). READ L is low and is sent to input D2 of each decoder; it selects read drivers and

switches in this case. To verify this point, refer to the truth table and diagram in Figure 2-9. Decoder inputs D0 and D1 select the particular switch or driver as shown below.

Decoder E34 – D1 is high, D0 is high: selects output 3 (pin 10) which is read switch XS07.

Decoder E46 – D1 is high, D0 is high: selects output 3 (pin 10) which is read driver XPRD7.

Decoder E28 – D1 is high, D0 is high: selects output 3 (pin 10) which is read switch YS07.

Decoder E8 – D1 is low, D0 is high: selects output 1 (pin 12) which is read driver YPRD5.

The last step is to follow the outputs of the drivers and switches to the stack diode matrix (Drawing H213-0-1, sheet 2). For the X line, the circuit is from driver XPRD7 to diode junction E7-11, across termination 35 to switch XS07. For the Y line, the circuit is from driver YPRD5 to diode junction E4-9, across termination 15 to switch YS03. The terminations indicate the point on the stack printed circuit board where the X or Y line is soldered. Physically, the wire that is connected across the termination is strung through 64 cores per bit mat (total of 1024 cores in series for 16-bit memory).

Table 2-3
Word Address Decoding Signals

Address Bit	Unibus Receiver Input	Receiver Output	Flip-Flop State	Flip-Flop Output Signals
A01	L	H	set	A01H = H
A02	H	L	reset	A02H = L
A03	L	H	set	A03H = H, A03L = L
A04	L	H	set	A04H = H
A05	L	H	set	A05H = H
A06	L	H	set	A06H = H, A06L = L
A07	L	H	set	A07H = H
A08	L	H	set	A08H = H
A09	L	H	set	A09H = H, A09L = L
A10	L	H	set	A10H = H
A11	L	H	set	A11H = H
A12	L	H	set	A12H = H, A12L = L
A13	--	–	reset	A13H = L, A13L = H

2.5 READ/WRITE CURRENT GENERATION AND SENSING

2.5.1 Introduction

Aside from the addressing and control logic, four functional units are involved in generating current to switch the cores and detect their state. The X and Y line current generators supply the drive current (via switches and drivers); the inhibit drivers allow 0s to be written during a write operation; the sense amplifiers detect 1s during a read operation; and the memory data register (MDR) temporarily stores data to be written or data that has been read from the memory. The following paragraphs discuss each functional unit and their interrelation.

2.5.2 Read/Write Operations

The discussion of the read/write operations shows the interrelation of the current generator, inhibit drivers, sense amplifiers, and memory data register. Details of the operation of each functional unit are discussed in subsequent paragraphs. Several control signals are mentioned; however, details of their generation and timing are described in Paragraph 2.8.

For clarity, one data bit (D07) of the selected word is discussed and the text is referenced to Figure 2-14 which is a simplified block diagram. Detailed logic for the MDR, Unibus receivers and drivers, sense amplifiers, and inhibit drivers for all 16 data bits is shown in Drawings G110-0-1, sheets 3 and 4.

During a read operation, half-select currents flow in the X and Y lines for the selected word in each bit mat. These currents flow opposite to the write currents; therefore, cores in the 1 state are switched to the 0 state and cores in the 0 state are unchanged. Switching the core from the 1 state to the 0 state induces a voltage pulse in the sense winding. This pulse is detected by sense amplifier E52 as a differential voltage on input pins 6 and 7 that exceeds the threshold reference voltage. This pulse is amplified and when STROBE 0H is generated at pin 11, the output of sense amplifier E52 goes high. Just prior to the strobe signal, the control logic generates RESET 0 which clears (resets) flip-flop E54. The sense amplifier output is inverted by E56 and sent to the present input (pin 10) of MDR flip-flop E54. A low on the present input sets the flip-flop; its 1-output (pin 9) is a high and its 0-output (pin 8) is a low. The high from pin 9 of the flip-flop is sent to input pin 1 of the Unibus driver E21. The other input to this gate is the data out signal. When the control logic generates DATA OUT H, the output of E21 is low (logical 0 for memory logic and logical 1 for Unibus logic). This is the read-out of bit D07 and is sent to the requesting device via the Unibus. Timing diagrams for the sense operation are shown in Figure 2-15.

The read operation is destructive: all cores at the specified location are now 0. The data that was read must be restored by a write operation which immediately follows the read operation. Flip-flop E54 is still in the set state; therefore, its 0-output (pin 8), which is high, is sent to input pin 9 of NAND gate E53. The control logic generates the inhibit driver control signal TINH0 H which is the other input to gate E53. The gate is not asserted (pin 8 is low) and the inhibit driver is not turned on. With no inhibit current in the inhibit line to oppose the half-select Y line current, a 1 is written back into the appropriate cores.

In this example, if bit D07 is a 0 in core, it does not switch during the read operation and the output of sense amplifier E52 does not go high. Flip-flop E54 remains cleared (reset): its 1-output (pin 9) is low and its 0-output (pin 8) is high. When the control logic generates DATA OUT H, the output of Unibus driver E21 is high (logical 1 for memory logic and logical 0 for Unibus logic). The 0-output of flip-flop E54, which is high, is sent to NAND gate E53. During the subsequent write operation, TINH0 H is generated which produces a low output signal at E53 pin 8. This activates the inhibit driver which produces a current that opposes the Y line current and prevents a 1 from being written into this bit of the selected word.

The read/write operation which has been discussed is a read/restore operation (DATI). The requesting device wants to read a word from memory and, as an internal requirement, the memory must restore the word by writing it back in core. In this case, the MDR flip-flops are preset by the sense amplifier outputs when 1s are read from the core. The flip-flop outputs are used in the subsequent write (restore) operation to control the inhibit drivers. If the requesting device wants to write a word into memory (DATO), it must load the data into the MDR flip-flops. The device asserts the data on the Unibus from which it is picked off via Unibus receivers. In this example, bit D07 is sent to pin 7 of Unibus receiver E10. The bit is inverted by the receiver and sent to the D-input (pin 12) of flip-flop E54. At the start of the DATO cycle, the control logic generates LOAD 0 H which clocks the flip-flop. If the D-input is high, E54 is set and its 0-output is low. Control gate E53 is not asserted by TINH0 H and the inhibit driver is not turned on. A 1 is written into the selected core. If the D-input is low, E54 is reset and its 0-output is high. Control gate E53 is asserted by TINH0 H and the inhibit driver is turned on. A 0 is written into the selected core. Because RESET L and STROBE H are disabled in this mode, the read operation is used only to magnetically clear the cores.

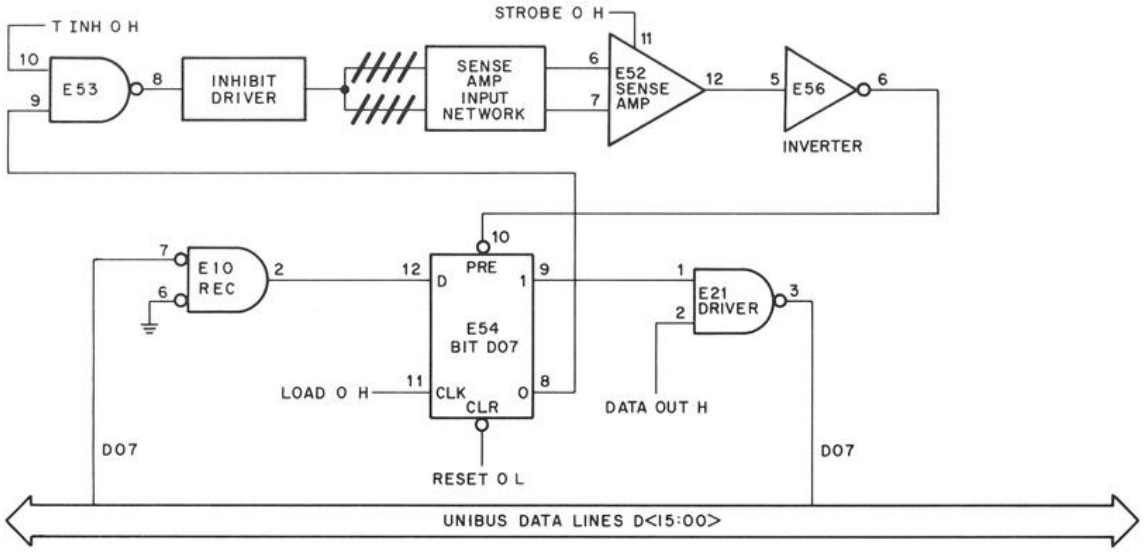


Figure 2-14 Interconnection of Unibus, Data Register, Sense Amplifier, and Inhibit Driver

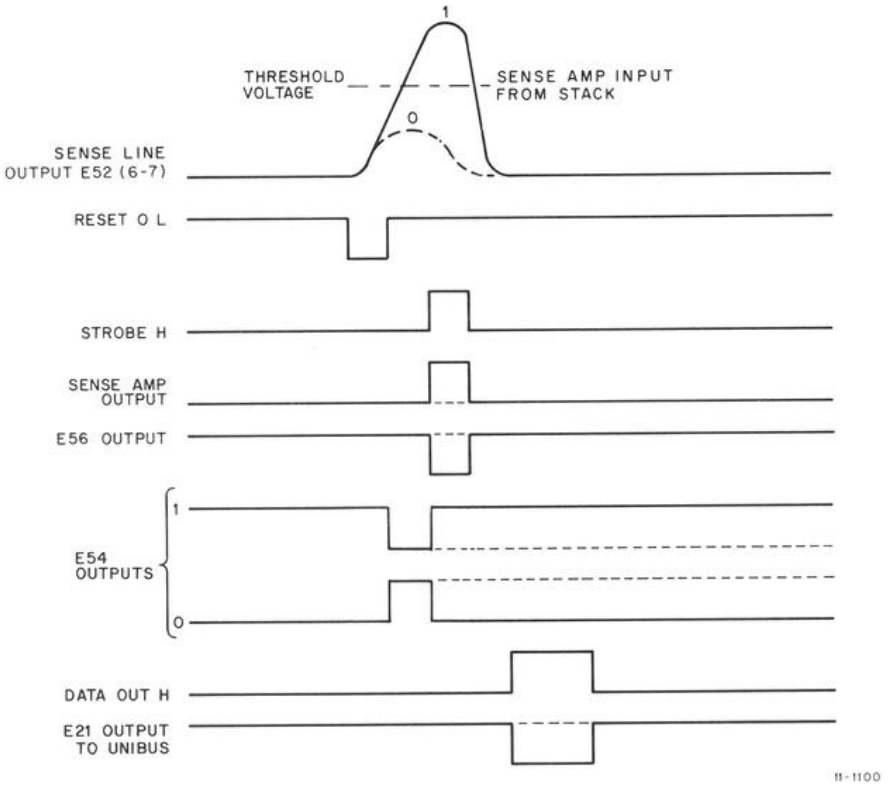


Figure 2-15 Timing Diagram For Sense Portion of a Read Operation

2.5.3 X and Y Current Generators

Two identical current generators are provided: one each for the X and Y drive lines. They generate the current pulses that are used during read and write operations to switch the cores. The current generators and associated reference voltage supply are shown in Drawing G231-0-1, sheet 2. This discussion refers to Figure 2-16 which shows the Y current generator and reference voltage supply.

Optimum core switching requires repeatable current pulses of constant amplitude with a linear rise time. The current generator and reference voltage circuit provide current pulses that meet these requirements. The amplitude of the output current pulse is determined by the reference voltage circuit; the rise time is determined by an RC circuit in the current generator; and pulse duration is determined by the length of the triggering pulse TWID H.

During the quiescent state of the current generator, input transistor Q8 is on; its collector voltage is 4.7V and is connected to the cathode of diode D62 which reverse biases it. The anode of D62 is connected to the emitter of transistor Q4 which is the output of the reference voltage circuit. In this state, D62 blocks the output from the reference voltage circuit to the current generator. With Q8 on, both output transistors Q9 and Q10 are turned off and the current generator is off.

Operation of the current generator is triggered by a high TWID H signal from the control logic. TWID H is double inverted by two E6 inverters and sent to the base of Q8 which turns it off. When Q8 is cut off, capacitor C52 starts charging. This provides base drive to output transistors Q9 and Q10 and they start to conduct. With Q8 off, its collector goes negative until it reaches the forward bias level of D62 which is the value of the reference voltage minus the voltage drop across D62. The rise time of the current pulse is determined by the time constant

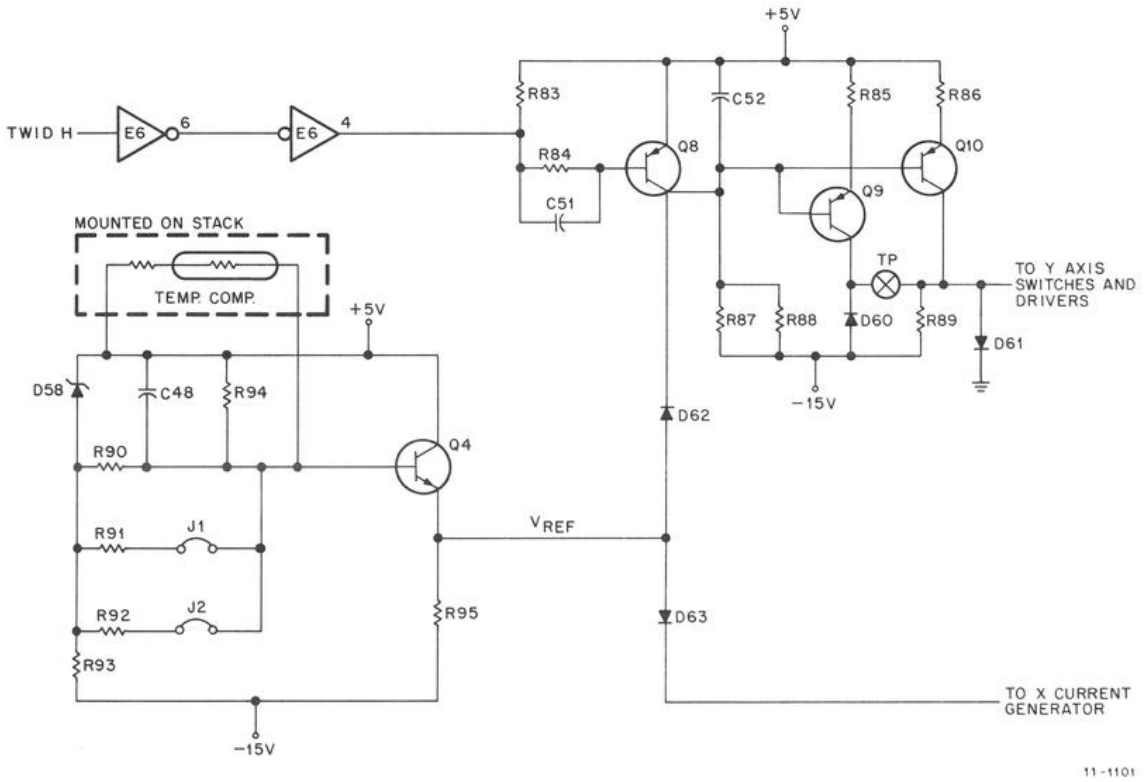


Figure 2-16 Y Current Generator and Reference Voltage Supply

of C52, R87 and R88. The amplitude of the pulse is determined by the value of the reference voltage. When TWID H goes low again, the current generator is turned off and the output pulse is terminated.

A resistor network in the base circuit of Q4 in the reference supply is used to set the amplitude of the current generator to approximately 410 mA. The total resistance of parallel network R90, R91, and R92 is changed by the configuration of jumpers J1 and J2. The amplitude of the current generator output pulse is factory set as close as possible to 410 mA at 25°C. It should not be changed in the field.

The base circuit of Q4 is temperature compensated by a resistor and thermistor that are mounted on the stack. This ensures that the amplitude of the current generator output pulse remains within specified tolerances over the temperature range of 0°C to 50°C. This temperature compensation is approximately –0.8 mA/°C.

2.5.4 Inhibit Driver

A detailed schematic of the inhibit driver for bit D07 is shown in Figure 2-17; it is typical of all 16 inhibit drivers (Drawing G110-0-1, sheets 3 and 4).

When the inhibit driver is off, none of the currents shown in the schematic are flowing. Transistor Q7 is held off by the negative voltage on its base. The output of NAND gate E53 goes low (ground) when this inhibit driver is selected. Current i_1 flows into the output circuit of E53 from the +5V supply via resistor R87 and the primary winding (terminals 15 and 16) of transformer T8. An equal current is induced in the base-emitter circuit of Q7 which is connected to the transformer secondary winding (terminals 1 and 2). This base current overcomes the reverse bias voltage and turns on Q7. Current i_1, and therefore induced-current i_2, is determined by resistor R87 and the reflected base-emitter voltage V_{be} of Q7. When Q7 is turned on, current flows from ground, through Balun transformer T7, isolation diodes D13 and D14, and the sense/inhibit winding to the common inhibit terminal (07IN). The Balun transformer balances the two inhibit half-currents. At terminal 07IN the full inhibit current flows through resistor R72 and Q7 to –15V. The value for inhibit current is calculated as follows:

$$i_{inh} \cong \frac{15V - V_{ce\ sat\ Q7} - V_{be\ diodes}}{R72 + R_{core\ mat}}$$

$$\cong \frac{15 - 0.8 - 1.2}{13 + 4.5} \cong \frac{13}{17.5} \cong 740\ mA$$

Each leg of the sense/inhibit sees half the inhibit current; i.e., approximately 370 mA. Capacitor C55 decreases the rise time of the current.

The inhibit driver is turned off when the output (pin 8) of gate E53 goes from low to high. At turn-off time, the back emf caused by the stack inductive reactance tries to drive the collector of Q7 highly positive; however, diode D43 clamps this voltage to ground. When the output of E53 goes high (approximately +3.2V), its output pull-up transistor (an integral part of the gate circuit) tries to drive the turn-off current i_4 in the opposite direction through the transformer primary winding. An equal current induced in the secondary winding removes the forward bias from the base of Q7 and turns it off. With Q7 off, all dynamic current flow ceases in the circuit and the negative voltage on the base of Q7 keeps it turned off until the output of gate E53 goes low again.

Capacitor C74 allows the gate to pump reverse current i_4 into the transformer primary; it also helps to decrease the turn-on time of Q7. Diode D59 prevents reverse breakdown of the base-emitter junction of Q7.

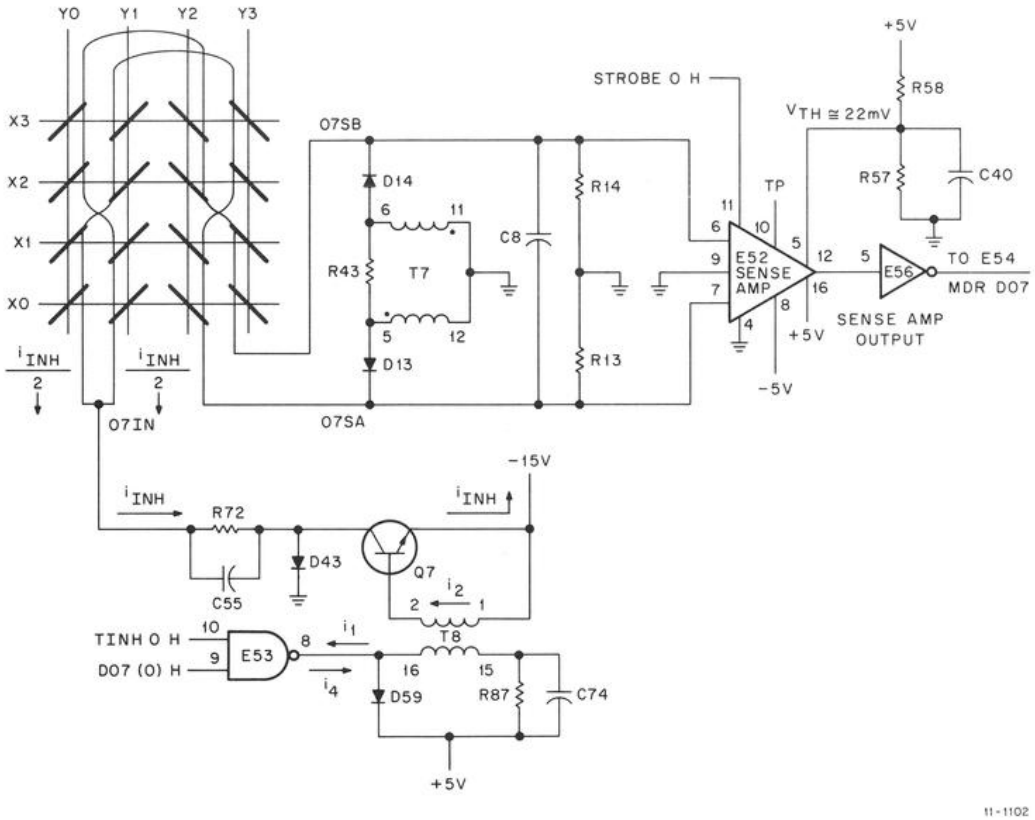


Figure 2-17 Sense Amplifier and Inhibit Driver

2.5.5 Sense Amplifier

A detailed schematic of the sense amplifier circuit for bit D07 is shown in Figure 2-17; it is typical of all 16 sense amplifier circuits (Drawing G110-0-1, sheets 3 and 4). It consists of the sense amplifier, terminating network for the sense/inhibit winding, and threshold voltage network.

The sense amplifier input (E52 pins 6 and 7) is across the sense/inhibit winding (points 07SB and 07SA). Resistors R13 and R14 are matched to terminate the sense/inhibit line in the desired impedance. Practically speaking, during the sense operation, the inhibit driver connection is an open circuit through the driver transistor Q7. The effect of the inhibit driver circuit, Balun transformer T7, and isolation diodes D13 and D14 can be ignored during the sense operation, because the diodes are reverse biased.

Sense amplifier E52 is one-half of a dual IC package (type 7528). A simplified block diagram of the package is shown in Figure 2-18. The two identical circuits are marked 1 and 2. Each consists of a preamplifier and sense amplifier. The output of the preamplifier is available as a test point to observe the amplified core signal and to facilitate accurate strobe timing. Both circuits share a reference voltage (or threshold voltage) amplifier (pins 4 and 5). In this application, pin 4 is grounded and a positive threshold voltage of approximately 20 mV is supplied. to pin 5. This voltage is obtained from the +5V supply through resistor voltage divider R57 and R58; C40 is a bypass capacitor. Operation of the sense amplifier is discussed in Paragraph 2.5.2.

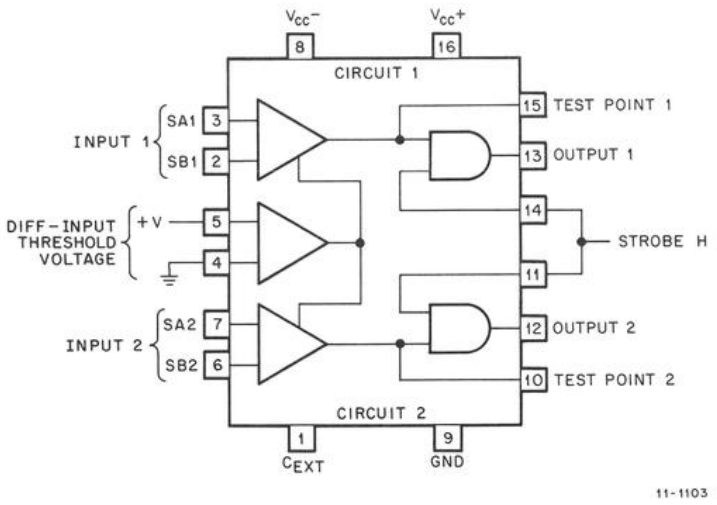


Figure 2-18 Type 7528 Dual Sense Amplifiers with Preamplifier Test Points

2.5.6 Memory Data Register

The memory data register (MDR) is a 16-bit flip-flop register that is used to store a word after it is read out of the memory, or to store a word from the Unibus prior to its being written into the memory. It is composed of eight 74H74 dual high-speed D-type flip-flops: bits D00–D07 are shown in Drawing G110-0-1, sheet 3 and are identified as E54, E57, E60, and E63; bits D08–D15 are shown in Drawing G110-0-1, sheet 4 and are identified as E42, E45, E48, and E51.

At the start of a memory operation, the MDR is cleared directly via the CLEAR input (pin 1 or pin 13) of each flip-flop; the clear signal is RESET 0 L for bits D00–D07 and RESET 1 L for bits D08–D15.

The operation of the MDR during a read/restore operation (DATI) and a write operation (DATO) is discussed in Paragraph 2.5.2.

2.6 STACK DISCHARGE CIRCUIT

The stack discharge circuit assists the stack capacitance in recovering and shortens the rise time of the stack current. It also reduces unwanted currents in the seven unselected lines associated with the selected driver.

Figure 2-19 shows the stack discharge circuit. Its output is taken from the emitter of transistor Q2 and goes to the junction of each X and Y read/write switch pair via a resistor. This common interconnection is labeled V_0. It is desired that $V_0 \simeq 0V$ (ground) during a read operation; and $V_0 \simeq -15V$ during a write operation. The effective stack capacitance associated with each line is shown as C_{stack}.

During a write operation, READ H is low; it is inverted and ANDed with TWID H at NAND gate E4. The low output (pin 11) of E4 is inverted by E6 and sent to the cathode of diode D51 which reverse biases it. The emitter of Q1 becomes more positive, overcomes the constant positive base bias, and turns on transistor Q1. When Q1 conducts, it provides base drive for Q3 which also turns on. When Q3 conducts, it reduces the base drive on Q2 and it turns off. The emitter voltage of Q2 goes to approximately –14V, which is V_0 on the switch node for the stack. Diode D57 prevents hard saturation of Q3. Diode D55 holds Q2 off. During a write operation, $V_0 = -14V$ and the stack discharge circuit is considered to be turned on (input transistor Q1 is on).

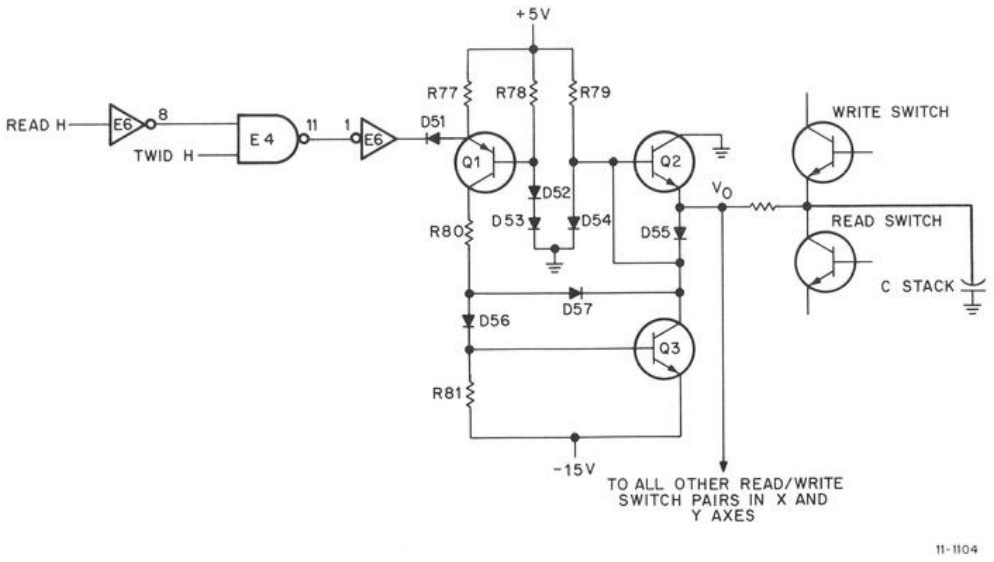


Figure 2-19 Stack Discharge Circuit

During a read operation, READ H is high; it is inverted and ANDed with TWID H at NAND gate E4. The gate is not asserted and its output (pin 11) is high. This signal is inverted by E6 and sent to the cathode of diode D51 which forward biases it. The voltage on the emitter of Q1 produced by the current through R77 is not enough to overcome the constant positive bias and Q1 is turned off. With Q1 off, Q3 looses its base drive and turns off. Now, D55 cannot hold Q2 off. As long as the stack capacitance is charged negatively, base current exists for Q2 and it remains on. The stack capacitance now charges in the positive direction until it reaches ground potential. During a read operation, $V_0 \simeq 0V$ and the stack discharge circuit is considered to be off (input transistor Q1 is off).

To see how the stack discharge circuit reduces unwanted currents on the seven unselected lines associated with the selected driver, see Figure 2-13.

During a read operation, the stack discharge circuit is off and $V_0 = 0V$. The current generator drives the read driver node of the stack towards ground; the current generator output is clamped to ground by diode D61. The anodes of the eight read diodes are at ground. The stack discharge circuit is on and the cathodes of the seven unselected diodes are also at ground which back biases them; therefore, they are off. The read switch pulls the cathode of the selected line towards –14V which forward biases it and allows conduction through the diode. Current flows only through the selected line. Reverse biasing of the diodes in the unselected lines prevents current from flowing between the unselected nodes and the selected read driver.

The stack discharge circuit performs the same task during the write operation by back biasing the anodes of the diodes in the unselected lines with –14V.

2.7 DC LO CIRCUIT

A circuit on the driver module (Drawing G231-0-1, sheet 2) opens the –15V supply line to the current generators when power is interrupted to the power supply. When power is interrupted, the +5V supply is lost and the operation of all logic is indeterminate. In this state, it is necessary to cut off the –15V supply to the X and Y line current generators to prevent them from destroying stored data. The circuit that performs the –15V cut off is called the DC LO circuit (Figure 2-20).

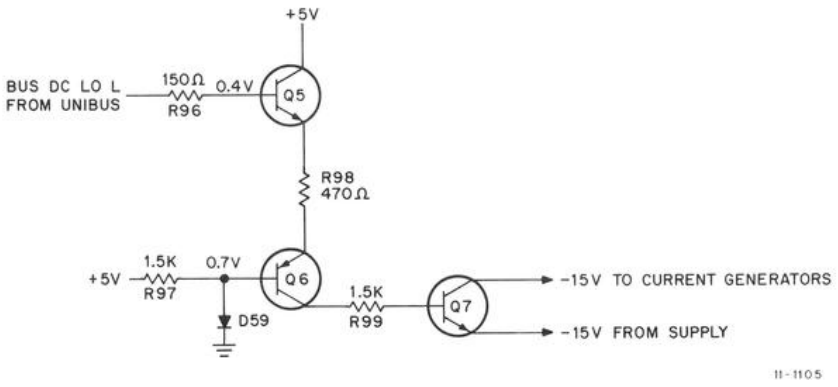


Figure 2-20 DC LO Circuit, Schematic Diagram

The –15V supply for the X and Y line current generators passes through transistor Q7 in the DC LO circuit. Q7 must be turned on for the –15V to reach the current generators.

The circuit monitors BUS DC LO L from the power supply via the Unibus. This signal is sent to the base of transistor Q5. When power is on, BUS DC LO L is high (not asserted). The voltage across R96 forward biases Q5 and it turns on which turns on Q6. The conduction through Q5 and Q6 forward biases Q7 which turns it on. The –15V flows through Q7 to the X and Y line current generators.

When power is interrupted, BUS DC LO L goes low (asserted). Q5 is now reverse biased and it turns off which turns off Q6. With Q5 and Q6 off, Q7 is also turned off which opens the –15V line to the current generators. This circuit still functions when BUS DC LO L is asserted even if the +5V supply drops to zero.

2.8 OPERATING MODE SELECTION LOGIC

When the memory is addressed by the master device, one of four bus transactions is selected. The transaction (or operation) selected is determined by the states of control bits C01 and C00 and address bit A00 as placed on the Unibus by the master device. Table 2-4 shows the states of these bits for each transaction.

The logic that decodes the mode and byte control bits is shown in Drawing G110-0-1, sheet 2; it appears at the bottom of the sheet and is identified as the byte masking logic. Bits BUS C01, BUS C00, and BUS A00 are taken from the Unibus to three E29 receivers. One input of each gate associated with C01 and C00 is connected to the output of the PROTECT LOW gate (E29 pin 3). Both inputs to this gate are tied to +5V so that its output is always low. For troubleshooting purposes, a jumper (W11) can be installed that makes the gate output high which allows only DATI operations to be performed regardless of the states of bits C01 and C00. This jumper hardwires the memory as a read-only device.

The outputs of the three E29 receivers (C01, C00, and A00) are sent to the byte masking logic to generate LOAD 0 H AND LOAD 1 H and to qualify a group of gates which are enabled by control signals to generate RESET 0 L, RESET 1 L, STROBE 0 H, STROBE 1 H, and DATA OUT H. The logic also conditions the D-input of the PAUSE flip-flop (E4 pin 12) to allow it to be set or reset. It also applies conditioning signals to the wired-AND that provides the clocking signal to the Slave Synchronization (SSYN) flip-flop. The PAUSE flip-flop and the SSYN flip-flop are part of the control logic.

Table 2-4
Selection of Bus Transactions

Transaction	Mnemonic	Mode Control		Control A00	Function
		C⟨01:00⟩	Octal		
Data In	DATI	00	0	X	Data from memory to master. Memory performs read and restore operations.
Data In, Pause	DATIP	01	1	X	Data from memory to master. Restore operation is inhibited. Must be followed by DATO or DATOB. Read operation is inhibited.
Data Out	DATO	10	2	X	Data from master to memory (words).
Data Out, High Byte	DATOB	11	3	1	Data from master to memory. High byte on data lines D⟨15:08⟩.
Data Out, Low Byte	DATOB	11	3	0	Data from master to memory. Low byte on data lines D⟨07:00⟩.

The signals generated for each bus transaction are shown in Table 2-5. The memory operational sequences are discussed in subsequent paragraphs. To avoid confusion in interpreting the transactions listed in Table 2-5, the purpose of the PAUSE flip-flop is discussed briefly. During DATIP, the PAUSE flip-flop is set during the read operation which inhibits the restore (write) operation. The DATIP must be followed by a DATO or DATOB on the same address. The DATO or DATOB that follows a DATIP is shorter than a standard DATO or DATOB because the initial read operation is eliminated. In Table 2-5, the suffix PAUSE L identifies the standard transactions; the suffix PAUSE H identifies the DATO and DATOB transactions that must follow a DATIP.

2.9 CONTROL LOGIC

2.9.1 Introduction

The control logic generates the precisely timed signals that initiate and stop the memory operations that are requested as a result of the decoding of the bus transaction. The heart of the control logic is the delay line timing circuit. For better understanding, the timing circuit, slave sync circuit, pause/write restart circuit, and strobe generating circuit are described separately. Then, each bus transaction is discussed in detail. The discussion is to detailed logic level but the signals are not traced through each component. The text is referenced to logic Drawing G110-0-1, sheet 2 and the timing diagrams in Drawing MM11-L-3.

2.9.2 Timing Circuit

The heart of the memory control logic is the timing circuit. When activated, it generates a series of precisely timed signals that control memory operation. The major component of the timing circuit is a delay line (DL1) with multiple 25-ns taps (Drawing C110-0-1, sheet 2). The delay line outputs are gated to produce the control signals. Figure 2-21 shows the timing of the delay line outputs and the timing of the control signals obtained by gating these outputs. A brief statement of the function of each control signal is included. Absolute timing is obtained from the engineering timing diagram (Drawing MM11-L-3). The discussion is referenced to Figure 2-21 and the control logic Drawing G110-0-1.

Table 2-5
Generation of Memory Operating Signals

Mode	Byte Control A00	Mode Control		State of PAUSE Flip-Flop	Signals Generated							Operational Sequence
		C01	C00		STROBE 0	STROBE 1	RESET 0	RESET 1	LOAD 0	LOAD 1	DATA OUT H	
DATI	X	0	0	Reset	X	X	X	X			X	Read-restore.
DATIP	X	0	1	Reset-Set	X	X	X	X			X	Read-pause. Restore inhibited by PAUSE flip-flop.
DATO PAUSE L	X	1	0	Reset					X	X		Clear-write.
DATO PAUSE H	X	1	0	Set					X	X		Write. Must follow DATIP.
DATOB PAUSE L	0	1	1	Reset		X		X	X			Clear-write selected byte 0. Clear-restore nonselected byte 1.
DATOB PAUSE H	0	1	1	Set		X		X	X			Write selected byte 0. Restore nonselected byte 1. Must follow DATIP.
DATOB PAUSE L	1	1	1	Reset	X		X			X		Clear-write selected byte 1. Clear-restore nonselected byte 0.
DATOB PAUSE H	1	1	1	Set	X		X			X		Write selected byte 1. Restore nonselected byte 0. Must follow DATIP.

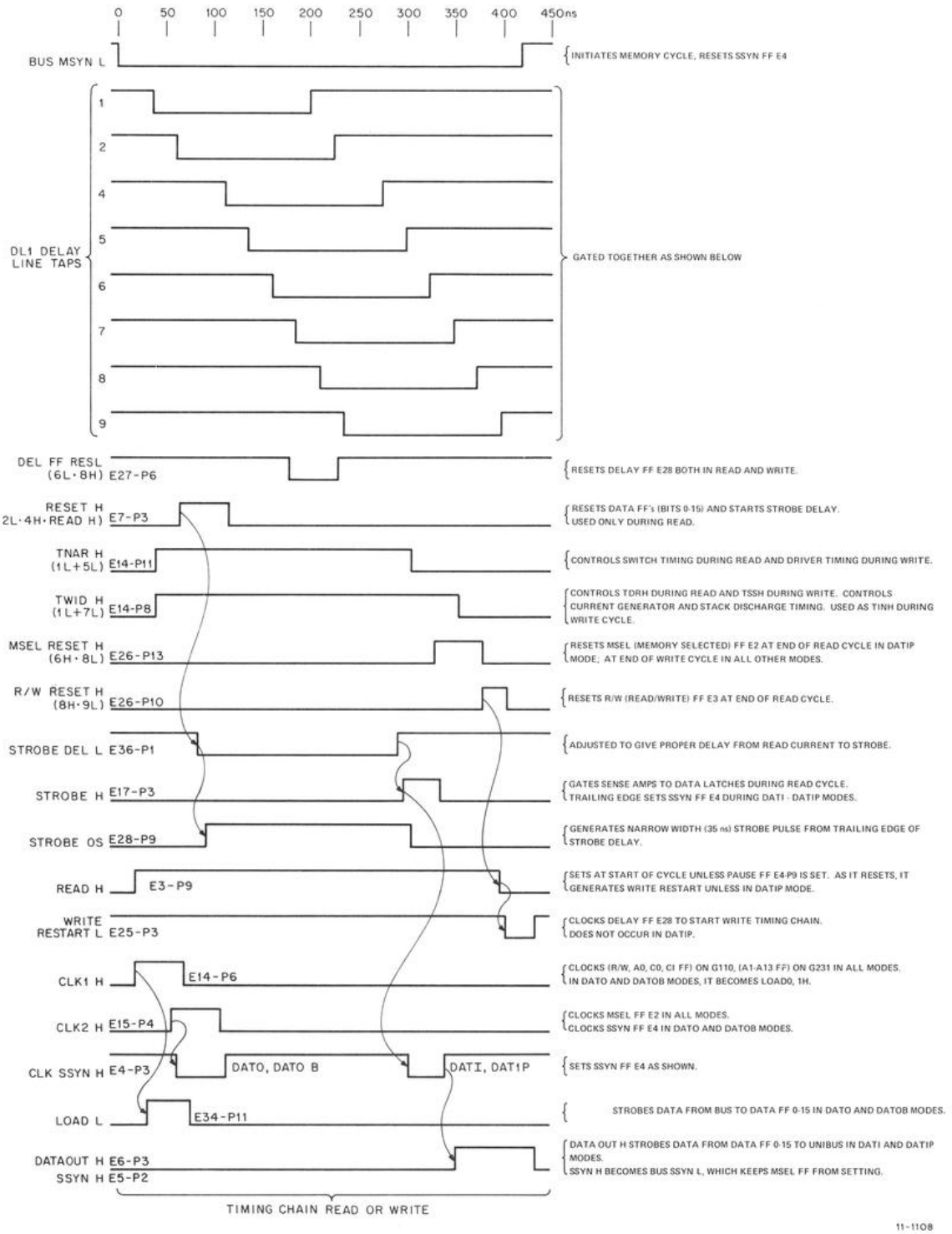


Figure 2-21 Basic Timing and Control Signal Functions

When the system is turned on, the processor asserts BUS INIT L on the Unibus. This initializing signal is sent to pins 6 and 7 of the bus receiver E7. It is inverted by E7 to produce a high which is sent to pins 9 and 10 of the memory select reset (MSEL RESET) gate E16. The output (pin 8) of E16 is a low which is used to clear (reset) MSEL flip-flop E2 via the 100 ns delay DL3. The output of E7 is also inverted by E18 to provide a low which clears read/write (R/W) flip-flop E3. The output of E7 is also inverted by E15 to provide a low which clears PAUSE flip-flop E4. The low output of E15 is double inverted by two E38 gates to clear the DEL flip-flop E28. The master places the address, mode control state, and data (if required) on the Unibus. The device address is decoded and DSEL H is generated and sent to pin 13 of E1, which is one of four input signals (pins 10, 11, 12, and 13). Pin 11 is high via the 0-output of MSEL flip-flop E2. SSYN flip-flop E4 is preset and it makes pin 10 of E1 high via its 1-output (pin 5). When the master asserts BUS MSYN L to bus receiver E23, pin 12 of E1 is high also. The output of E1 (pin 8) is a low which is sent to pin 13 of E5, pins 4 and 5 of E14, and pin 1 of delay line DL2. E14 inverts the low from E1 to start the positive CLK 1 H pulse. DL2 provides a 30-ns delay for the low signal from E1 which is inverted by E15 to start the positive CLK 2 H pulse. The output (pin 3) of DL2 is also sent to the preset input (pin 4) of MSEL flip-flop E2. This low signal directly sets E2; pin 6 goes low and is fed back to pin 10 of E1 to disable it. The output (pin 8) of E1 is now high and this signal terminates both clock pulses (CLK 1 H and CLK 2 H) via gates E14 and E15. These clock pulses are approximately 50-ns wide.

Gate E5 also inverts the low from E1 because pin 12 (WRITE RESTART L) of E5 is high. The positive transition at the output (pin 11) of E5 clocks delay (DEL) flip-flop E28 which sets it. Pin 5 of E28 is high and it is connected to pins 1 and 2 of DL1 driver gate E34. The low from the output (pin 3) of E34 is the input to delay line DL1. This signal remains low for approximately 225 ns until DEL flip-flop E28 is cleared by DELAY FF RESET L. This provides a negative pulse that propagates through the delay line and can be picked off at 25-ns intervals.

DL1 taps 2, 4, 5, 6, 7, 8, and 9 are used to generate control signals. Using Figure 2-21 as a guide, each control signal is discussed and related to the logic drawing (G110-0-1, sheet 2).

DELAY FF RESET

Tap 6L is inverted by E15 and sent to pins 3 and 5 of 3-input NAND gate E27; the third input (pin 4) is a tap 8H. The output (pin 6) of E27 is the signal that clears DEL flip-flop E28; however, it is ORed with INIT L in gate E38 (pins 9 and 10) and inverted by E38 pin 11 so that either (6L · 8H) or BUS INIT L can produce DELAY FF RESET L which clears E28 via its clear input (pin 1). This signal is generated in both read and write operations.

RESET H

Tap 2L, tape 4H, and READ H are gated to generate RESET H which triggers the strobe delay circuit and generates RESET 0 L and RESET 1 L during the read operation only. Tap 4H and READ H (high during read operation) are ANDed at pins 10 and 9 of E17. The low output of E17 is ANDed with tap 2L in gate E7. The high output (pin 3) is RESET H.

TWID H and TNAR H

The 0-output of DEL flip-flop E28 is ORed with tap 5L and tap 7L in separate gates (E14) to produce TWID H and TNAR H. Tap 5L is sent to pin 13 of E14; the other input to this gate (pin 12) is from the 0-output of DEL flip-flop E28. Tap 7L is sent to pin 10 of another E14 gate; pin 9 of this gate also is connected to the 0-output of DEL flip-flop E28. These gates are 2-input NAND gates (type 7437); however, they are shown as logically equivalent negative-input OR gates because it is desired to have them asserted high (logical 1) when TWID H or TNAR H is asserted.

At the start of a read or write cycle, just before E28 is set, TNAR and TWID are low because both inputs to each gate are high E28 is set and pins 12 and 9 of E14 go low; TNAR and TWID are both high which starts the positive TNAR and TWID pulses simultaneously. When taps 5 and 7 go low (E28 is still set), TNAR and TWID remain high. At the end of the read or write cycle, E28 is cleared (taps 5 and 7 are still low) and TNAR and TWID still remain high. When tap 5 is high again, TNAR goes low because both inputs (pins 12 and 13) of E14 are high. This terminates the positive TNAR pulse. Approximately 50-ns later, tap 7 is high again and TWID goes low which terminates the positive TWID pulse. To summarize, TNAR H and TWID H are started together by the setting of DEL flip-flop E28 before taps 5 and 7 are low; they are not affected when taps 5 and 7 go low. TNAR H and TWID H are terminated when taps 5 and 7 return high. The intervening clearing of E28 does not affect TNAR H or TWID H.

TNAR H and TWID H provide various control functions related to the operation of the switches, drivers, current generators, inhibit driver, and stack discharge circuit. At this point, the discussion digresses to follow TNAR H and TWID H through some additional logic to understand their functions. The logic is spread throughout several engineering drawings. To simplify the discussion, all the logic is shown in Figure 2-22.

TWID H is ANDed with the 0-output (pin 8) of R/W flip-flop E3 at pins 9 and 10 of gate E25. With TWID H high, E25 is asserted only when E3 is high; this occurs only during a write operation. The output (pin 8) of E25 is inverted by E14 to produce TINH 0 H and TINH 1 H.

The output of E14 is physically divided into two paths: TINH 0 H activates the inhibit drivers for bits D⟨07:00⟩ and TINH 1 H activates the inhibit drivers for bits D⟨15:08⟩. These signals do not leave the control module because the inhibit drivers are on this module also.

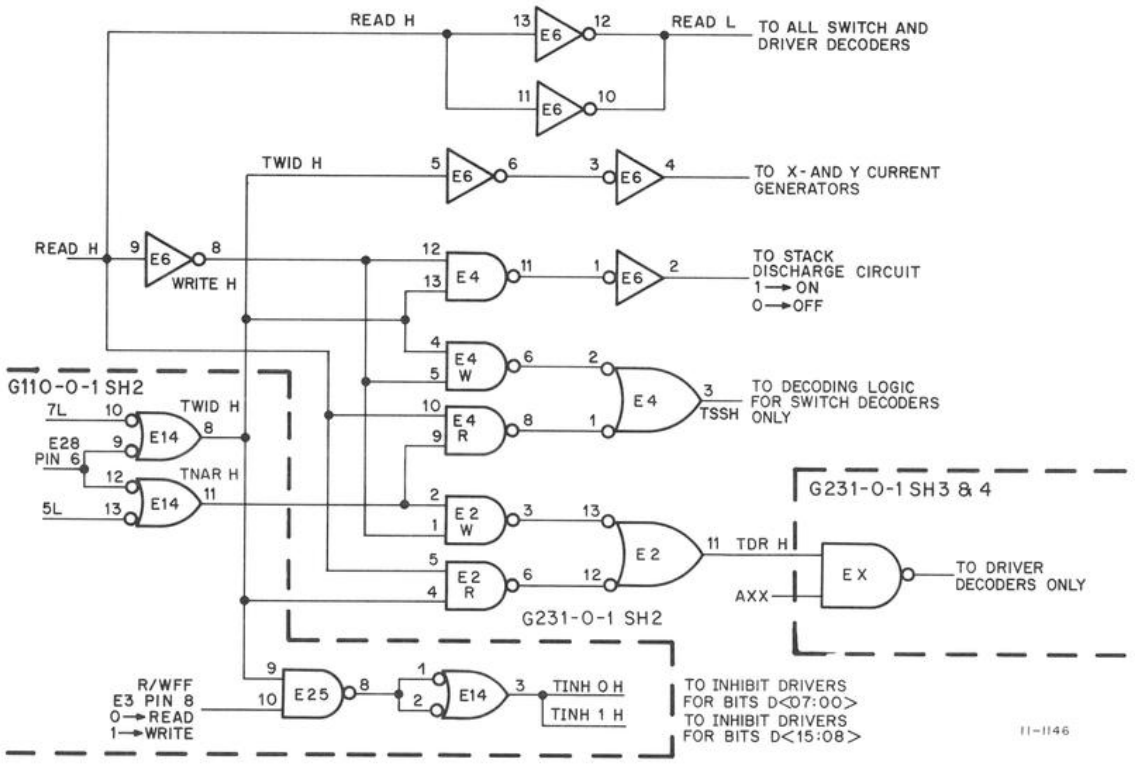


Figure 2-22 TWID H and TNAR H Control Logic

TWID H and TNAR H leave the control module (G110) and are sent to the drive module (G231). TWID H is sent to pin 4 of E2R and TNAR H is sent to pin 2 of E2W. Gates E2 and E4 are marked W and R in Figure 2-22 to show their association with write or read operations. READ H is sent from the 1-output (pin 9) of R/W flip-flop E3 on the control module to pin 9 of inverter E6 on the driver module. READ H is high during a read operation and it is low during a write operation. Assume that a read operation is selected. READ H is high at pin 9 of E6 and is sent to pin 5 of E2R to be ANDed with TWID H. This gate is asserted and its low output is sent to pin 12 of negative-input NOR gate E2 which inverts it to produce TDR H. This signal is a decoding input for the memory read/write drivers only. Gate E2W is not asserted because WRITE H, which is the inversion of READ H, is low. Therefore, TWID H controls decoding signal TDR H during a read operation. During a write operation READ H is low and WRITE H is high. TDR H is asserted via the output of gate E2W using the ANDing of WRITE H and TNAR H. Decoding signal TDR H is controlled by TNAR H during a write operation.

A similar logic network is used to control signal TSS H which enables six decoding signals that control memory read/write switches only. Gates E4W, E4R, and E4 are used; TSS H is generated at the output (pin 3) of E4. During a read operation, TNAR H controls enabling signal TSS H; TWID H controls TSS H during a write operation. TWID H controls the operation of the X and Y current generators. During read and write operations, when TWID H is high, it is double inverted by two E6 inverters to turn on both current generators.

TWID H also controls the operation of the stack discharge circuit. It is ANDed with WRITE H at pins 13 and 12 of NAND gate E4. The output (pin 11) of E4 is inverted by E6 to control the stack discharge circuit. This circuit is considered to be turned on when the output (pin 2) of E6 is high. This occurs during a write operation: TWID H and WRITE H both high.

Although not part of the timing circuit, Figure 2-22 shows READ H inverted by two E6 inverters to become READ L which is a decoding input to all type 8251 decoders for the memory switches and drivers. During a read operation, READ H is high and READ L is low which selects only read switches and drivers. Conversely, READ L is high during a write operation which selects only write switches and drivers (Paragraph 2.4.4.2).

MSEL RESET

The Memory Select (MSEL) flip-flop E2 is cleared (reset) at the end of a read operation in DATIP mode and at the end of a write operation in all other modes (DATI, DATO, and DATOB) by MSEL RESET L. This signal is generated at the output (pin 8) of gate E16. This gate is a type 74H53 2-2-2-3 input AND-OR-invert gate. Three of its four AND inputs are used to facilitate the various methods used to generate MSEL RESET L (Figure 2-23).

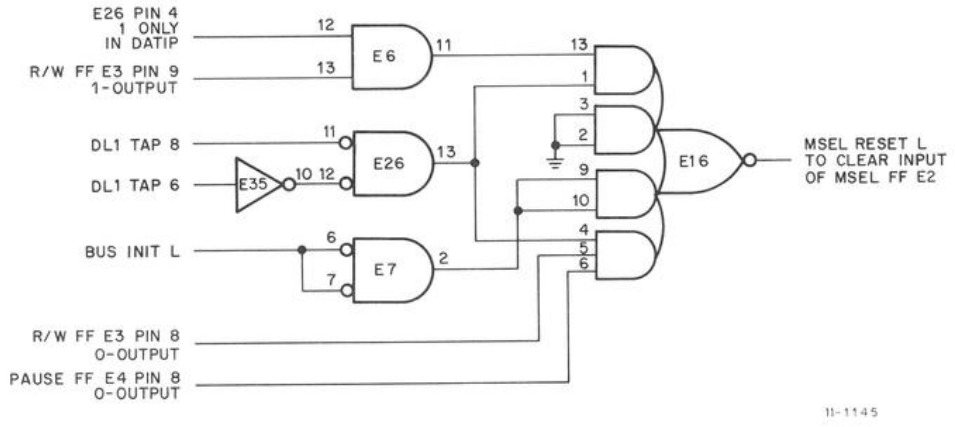


Figure 2-23 Generation of MSEL RESET L

When the system is turned on, the processor asserts BUS INIT L on the Unibus. The output of bus receiver E7 is high and is sent to pins 9 and 10 of E16 to generate MSEL RESET L at its output (pin 8). MSEL RESET L is passed through a 100-ns delay line (DL3) to the clear input (pin 1) of MSEL flip-flop E2 which directly clears (resets) it. All memory operations start with E2 cleared; however, it is set shortly (approximately 75 ns) after the processor asserts BUS MSYN L. It remains set until it is cleared by one of the following operations.

In the DATIP mode, pin 12 of AND gate E6 is high; in all other modes it is low, which disqualifies E6. A read operation is performed in DATIP so R/W flip-flop E3 is set. The 1-output of E3 is sent to pin 13 of E6. At this time pin 13 is high and a high is generated at the output (pin 11) of E6. This signal is sent to pin 13 of E16. This AND input is qualified when pin 1 is also high. This occurs when DL1 tap 6 is high and DL1 tap 8 is low. Tap 6H is inverted by E35 and sent to pin 12 of E26. Tap 8L is sent directly to the other input (pin 11). The gate is asserted and sends a high pin 1 of E16. This generates MSEL RESET L at the output (pin 8) of E16. This low signal clears MSEL flip-flop E2 at the end of the read operation (timed by 6H and 8L).

In all other modes (DATI, DATO, and DATOB), MSEL RESET L is generated at the end of the write operation. Each of the three modes starts with a read operation (except DATO or DATOB following a DATIP). The R/W flip-flop is set so its 0-output (pin 8) is low which disqualifies the 3-input (pins 4, 5, and 6) AND gate in E16. Taps 6H and 8L cannot qualify this AND input nor can they qualify the other AND input (pins 1 and 13) because the memory is not in the DATIP mode. Therefore, the read operation is completed and MSEL RESET L is not generated. The write operation is now started and the R/W flip-flop is cleared. This puts a high on input 5 of E16; input 6 is high because the PAUSE flip-flop is reset (pin 8 is a 1). When tap 6 is high and tap 8 is low, input 4 of E16 is high. This generates MSEL RESET L to clear MSEL flip-flop E2 at the end of the write operation. MSEL functions as a memory busy flip-flop.

R/W RESET

The timing for the generation of the signal to clear (reset) R/W flip-flop E3 is obtained from taps 8 and 9 of DL1. Tap 9 is sent directly to pin 8 of E26. Tap 8 is inverted by E35 and sent to pin 9 of E26. When tap 9 is low and tap 8 is high, E26 is asserted (output pin 10 is high). This signal is sometimes called R/W RESET H. It is ANDed with READ H at pins 2 and 1 of NAND gate E18 to generate R/W RESET L. When this signal is a low, it directly resets R/W flip-flop E3 via its clear input (pin 13). READ H is high when the R/W flip-flop is set because it comes from the 1-output (pin 9). The remainder of the control signals shown in Figure 2-21 are discussed in the circuit descriptions contained in Paragraph 2.9.3, Slave Sync Circuit; Paragraph 2.9.4, Pause/Write Restart Circuit; and Paragraph 2.9.5, Strobe Generating Circuit.

2.9.3 Slave Synchronization (SSYN) Circuit

Slave synchronization (SSYN) is the response of the slave device to the master, usually a response to master synchronization (MSYN). The master places address information, mode control information, and data (if a DATO or DATOB is selected) on the Unibus. It then asserts BUS MSYN L only if BUS SSYN L from the slave is cleared, which indicates that the slave can participate in a bus transaction. The slave asserts BUS SSYN L when it has data to send (DATI or DATIP) or when it has received data (DATO or DATOB). The master receives BUS SSYN L in both cases and clears BUS MSYN L.

When the slave receives the cleared BUS MSYN L it clears BUS SSYN L which frees the bus. This brief statement of the SSYN/MSYN interaction is necessary to understand the operation of the memory SSYN circuit. Details of the SSYN/MSYN interaction during all bus transactions can be found in the *PDP-11 Unibus Interface Manual*, DEC-11-HIAB-D.

The SSYN circuit is shown in Drawing G110-0-1, sheet 2; however, for clarity, only the SSYN circuit is shown in Figure 2-24 along with the appropriate timing diagram.

During a DATI or DATIP transaction, BUS SSYN L is asserted by the memory when the data is placed on the Unibus by the memory data register. During a DATO or DATOB transaction, BUS SSYN L is asserted by the memory when it takes in the data from the Unibus. At the start of each transaction, the master first places the memory address (device and word) and mode control information on the Unibus. (Data is included if the transaction is DATO or DATOB.)

For a DATI or DATIP, BUS COI L is high at pin 10 of bus receiver E29. The output (pin 14) of E29 is low and it is sent to the D-input (pin 6) of C01 latch E30 and to pin 5 of the E5 WRITE gate. BUS MSYN L has not been asserted yet so the output (pin 13) of bus receiver E23 is low. This signal is sent to pin 2 of NOR gate E26; the other input (pin 3) of this gate is always low because MSYN A L is normally not connected. The output (pin 1) of E26 is inverted by E15 to produce SSYN RESET L which sets the SSYN flip-flop E4 via its preset input (pin 4). The 0-output (pin 6) is low and is sent to both inputs of bus driver E5. The output of this gate is the slave sync signal (BUS SSYN L) and, at this point, it is not asserted. As long as BUS MSYN L is not asserted, the SSYN flip-flop is preset. Now, the master asserts BUS MSYN L which disables the preset signal to the SSYN flip-flop (SSYN RESET L is high). Clock signal CLK 1 H is generated and clocks C01 latch E30. The latch is reset and its 0-output (pin 11) is a high which is sent to pin 10 of the E5 READ gate in the wired-AND. The wired-AND output is CLK SSYN which is high. It remains high as long as both E5 NAND gate outputs are high. This occurs when at least one input of each gate is low. The output of E5 WRITE remains high because input pin 5 is held low by the output C01 receiver E29. The output of this gate is not changed when the CLK 2 H pulse appears at pin 4. The output of E5 READ remains high until STROBE H goes high, at which point, its output goes low. When STROBE H goes low again, the wired-AND output is high again. This positive transition clocks the SSYN flip-flop which now resets because its D-input is tied to ground (low). The 0-output (pin 6) of the SSYN flip-flop is a high which asserts BUS SSYN L at the output (pin 3) of bus driver E5. The master receives the asserted BUS SSYN L signal and clears BUS MSYN L. The memory receives the cleared BUS MSYN L at bus receiver E23 and generates SSYN RESET L via gates E26 and E15 to set the SSYN flip-flop. The memory is now ready for the next transaction.

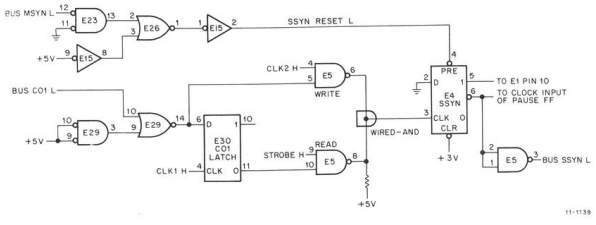
For a DATO or DATOB, the sequence is the same except that BUS C01 L is low at pin 10 of bus receiver E29. This conditions the wired-AND so that the output of E5 READ remains high. In this case, the CLK 2 H pulse generates the CLK SSYN pulse that clocks the SSYN flip-flop via E5 WRITE.

2.9.4 Pause/Write Restart Circuit

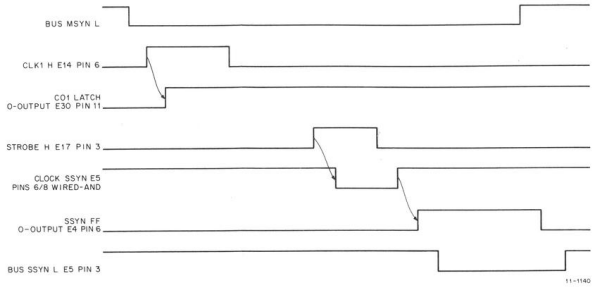
The PAUSE flip-flop is used to inhibit the restore (write) operation during a DATIP. This transaction is used to advantage when it is not necessary to restore the data after reading because the location is to have new data written into it. Eliminating the restore operation decreases the memory cycle time by approximately 50 percent. A DATIP must always be followed by a DATO or DATOB. In this case, the DATO or DATOB is shortened by eliminating the normal clear (READ) operation that is performed prior to the write operation. The location has been cleared previously by the DATIP so the DATO or DATOB performs only the write operation.

The pause/write restart circuit is shown in Drawing G110-0-1, sheet 2; however, for clarity, only the pause/write restart circuit is shown in Figure 2-25.

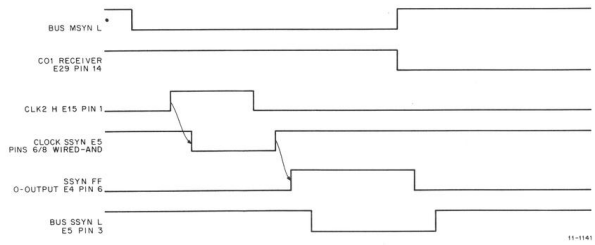
At the start of all bus transactions, the PAUSE flip-flop is reset and it remains in this state during the whole transaction except for a DATIP during which it is set during the read operation. The PAUSE flip-flop is clocked by the 0-output (pin 6) of the SSYN flip-flop when it is reset. The state (set or reset) of the PAUSE flip-flop is determined by its D-input (pin 12): D is high to set and D is low to reset. The D-input state is controlled by the Unibus mode control bits C01 and C00; only the mode control representing a DATIP provides a high to the D-input of the PAUSE flip-flop. During a DATIP, C01 is high and C00 is low at bus receivers E29 pin 10 and E29



Slave Synchronization (SSYN) Circuit



Timing Diagram for SSYN Circuit
During DATI and DATIP



Timing Diagram for SSYN Circuit
During DATO and DATOB

Figure 2-24 Slave Synchronization (SSYN)
Circuit and Timing Diagram

pin 7. These signals are inverted by the receivers and applied to the D-inputs of the C01 and C00 latches: C00 latch E30 pin 3 is high and C01 latch E30 pin 6 is low. When the latches are clocked by CLK1 H, latch C01 is reset and C00 is set. This puts a low on each input of negative-input AND gate E26 which generates a high at its output. This is the D-input to the PAUSE flip-flop. The PAUSE flip-flop is now conditioned to set when it is clocked.

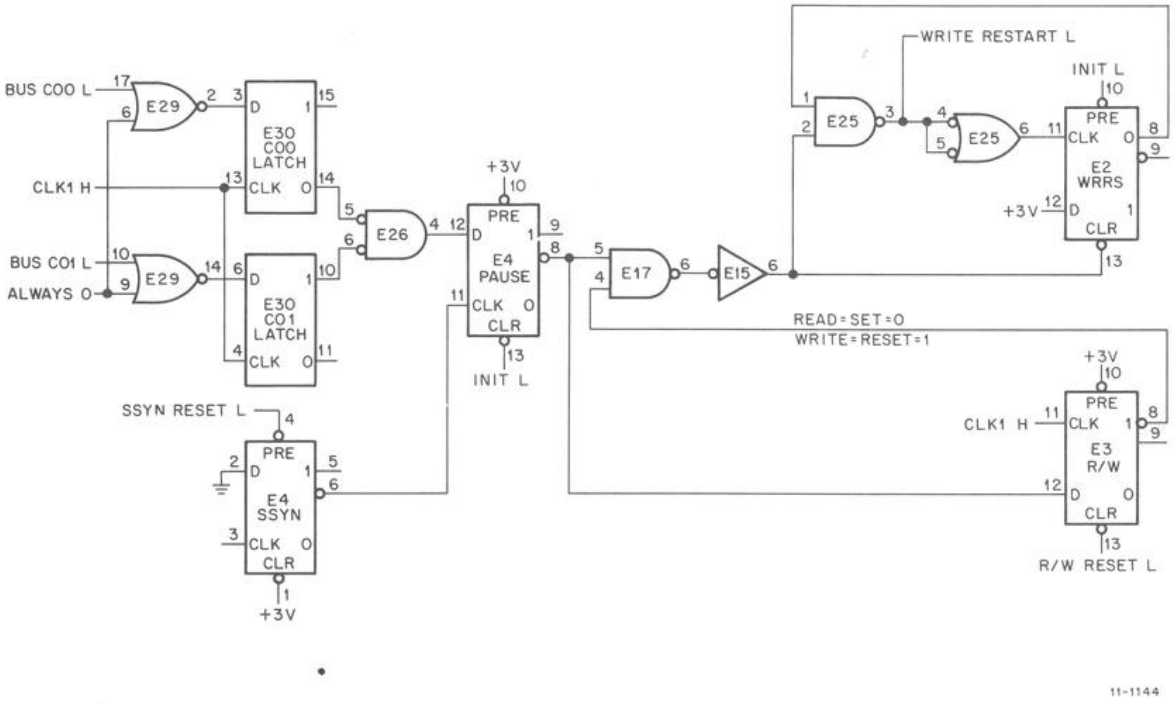


Figure 2-25 Pause/Write Restart Circuit

Going back to the start of the DATIP, the PAUSE flip-flop is reset. Its D-input is conditioned (D is high) but it has not been clocked so its 0 output (pin 8) is high. This output goes to the D-input of the read/write flip-flop (R/W E3). It is clocked early in the sequence by CLK 1 H so it is set; this permits a read operation. The 0-output (pin 8) of the R/W flip-flop is low and is sent to pin 4 of E17. The other input (pin 5) of E17 comes from the 0-output (pin 8) of the PAUSE flip-flop and it is a high at this time. The output of E17 is a high and is inverted by E15 which puts a low on the clear input of the write restart flip-flop (WRRS E2). The output of E15 also goes to input 2 of E25. The WRRS flip-flop is cleared (reset) and its 0-output (pin 8) is a high which is sent to the other input (pin 1) of E25. The output of E25 is the WRITE RESTART L signal which is produced to trigger the timing circuit and produce a write operation. It is high now, which is correct, because a read operation is being performed.

At the end of the read operation, the SSYN flip-flop is clocked which resets it. The positive transition at its 0-output (pin 6) clocks the PAUSE flip-flop which sets it and puts a low on pin 5 of E17. The timing circuit clears (resets) the R/W flip-flop which puts a high on pin 4 of E17. The output of E17 remains high which inhibits the WRITE RESTART L signal and prevents the initiation of a write operation.

For any other transaction (DATI, DATO, or DATOB) the PAUSE flip-flop is not set when it is clocked because its D-input is low. It remains reset which keeps a high on pin 5 of E17. When the R/W flip-flop is cleared, it puts a high on pin 4 of E17. Now, the output of E17 is low and is inverted by E15 and sent to pin 2 of E25. The WRRS flip-flop is reset so pin 1 of E25 is high also. The output (pin 3) of E25 goes low which generates WRITE RESTART L. This starts the formation of a low WRITE RESTART L pulse. This output is inverted by E25 pin 6 and clocks the WRRS flip-flop which sets it because its D-input is connected to +3V. Pin 8 of the WRRS now goes low and is fed to pin 1 of E25. This makes the output of E25 high again which terminates the low WRITE RESTART L pulse. This pulse triggers the timing circuit and initiates a write operation.

For a DATO or DATOB following a DATIP, the PAUSE flip-flop is reset by the SSYN flip-flop because the DATO or DATOB transaction started with the PAUSE flip-flop set previously by the DATIP.

2.9.5 Strobe Generating Circuit

The strobe generating circuit produces a narrow positive pulse (STROBE H) during the read operation to enable the STROBE 0 H and STROBE 1 H signals for the sense amplifiers.

The strobe generating circuit is shown in Drawing G110-0-1, sheet 2; however, for clarity, only the strobe generating circuit is shown in Figure 2-26 along with an appropriate timing diagram.

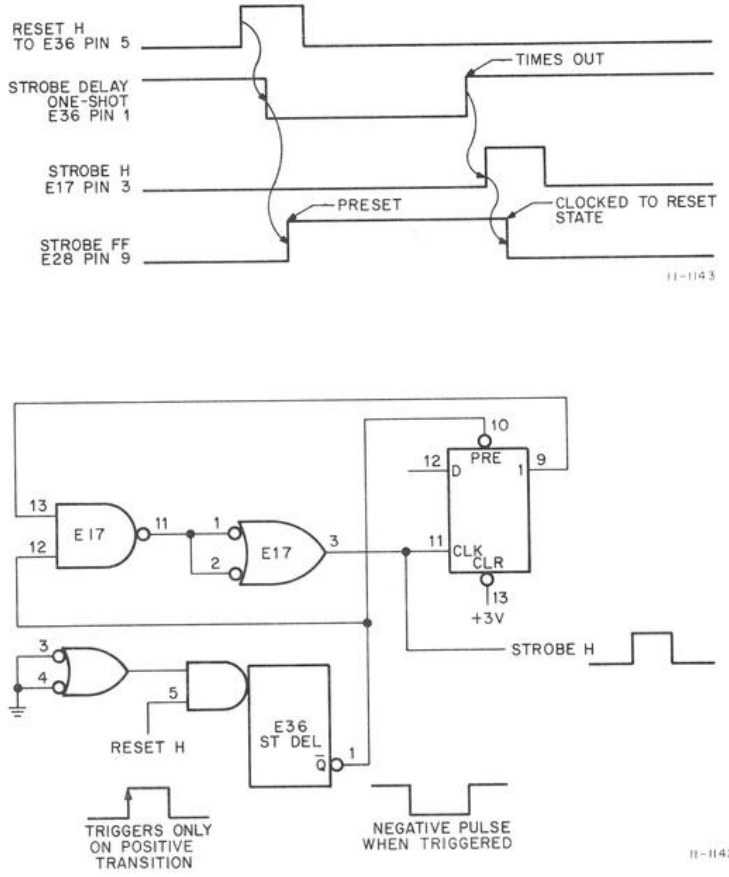


Figure 2-26 Strobe Generating Circuit and
Timing Diagram for STROBE H

During the read operation, the timing circuit generates RESET H which is a positive pulse. It is sent to pin 5 of the strobe delay one-shot (ST DEL E36). This 74121 one-shot provides complementary outputs but only the $\overline{Q}$ (negative pulse) output (pin 1) is used. Pins 3 and 4 of the ST DEL one-shot are connected to ground so that only a positive-going edge at pin 5 triggers it.

Prior to receiving the triggering signal (RESET H), the strobe generating circuit is in the quiescent state. The STROBE OS flip-flop E28 is in the reset state. (When the memory is powered up, E28 is driven to the reset state by E36 if it did not come up reset randomly.) The 1-output (pin 9) of E28 is low which is sent to pin 13 of E17. The ST DEL one-shot is inhibited so its $\overline{Q}$ output (pin 1) is high which is sent to pin 12 of E17. The output (pin 11) of E17 is high and is inverted by the next E17 gate (pin 3). This is the STROBE H signal and it is low at this time.

The timing circuit generates a positive RESET H pulse that is sent to pin 5 of E36. The positive edge of RESET H triggers E36 and its $\overline{Q}$-output (pin 1) goes to low. This is the start of a single negative pulse whose duration is determined by an external RC circuit connected to pins 10 and 11 of E36. The output of E36 directly sets STROBE OS flip-flop E28 via its preset input (pin 10). The 1-output (pin 9) of E28 goes high and is sent to pin 13 of E17. The other input to this gate (pin 12) is now low. E17 pin 11 is high and is inverted so E17 pin 3 is still low (no strobe pulse yet). When E36 times out, its output (pin 1) is high again. Pins 12 and 13 of E17 are now both high and the output (pin 11) of E17 is low. This signal is inverted and E17 pin 3 is high. This is the beginning of the STROBE H pulse. The positive transition at E17 pin 3 also clocks flip-flop E28. It is reset because its D-input is connected to ground (low). Pin 9 of E28 is now low. It is fed back to pin 13 of E17 which makes E17 pin 3 low again. This terminates the positive STROBE H pulse. The circuit is back to its quiescent state where it remains until another RESET H pulse comes along to trigger ST DEL one-shot E36.

2.9.6 Data In (DATI) Operation

The discussion of the DATI operation, as well as the DATIP, DATO, and DATOB operation, is descriptive. Signals are not traced through circuit components; rather, various events are integrated to describe a complete memory operating cycle. All the circuits involved have been discussed in detail in the preceding paragraphs of this chapter. Refer to engineering logic drawings G110-0-1, sheets 2, 3, and 4; G231-0-1, sheets 2, 3, and 4; MM11-L-3 (timing diagram); and Figure 2-27 which is a flow chart for memory operation.

In a DATI operation, the master requests that a selected memory location be read and the information transferred to the master via the Unibus. The readout is destructive because the read operation forces all cores in the selected location to 0. However, during readout, the information is temporarily stored in the memory data register (MDR) and is automatically restored to the selected location by a write operation that immediately follows the read operation.

At the start of the DATI, MSEL flip-flop is reset, DEL flip-flop is reset, R/W flip-flop is reset, PAUSE flip-flop is reset, and SSYN flip-flop is reset. The address lines and mode control lines (C01 and C00) are decoded. The master asserts BUS MSYN L and the cycle begins. CLK 1 H is generated, the DEL flip-flop is set, and the R/W flip-flop is set. Setting the DEL flip-flop initiates the timing chain via delay line DL1. The timing chain generates TWID H and TNAR H. CLK 2 H is generated at the same time and it presets the MSEL flip-flop which prevents the start of another cycle until it is reset. Signal READ H from the R/W flip-flop and signals TNAR H and TWID H go to the driver module to select the appropriate read drivers and switches; turn on the X and Y current generators; and control the stack discharge circuit. As a result of these signals, the X and Y half currents are directed to the selected memory location and all 16 cores (one per bit plane) are set to 0. Just prior to this event, the timing chain generates RESET 0 L and RESET 1 L which clear the memory data register. The timing chain generates STROBE H which sends STROBE 0 H and STROBE 1 H to the sense amplifiers. The strobe pulses are

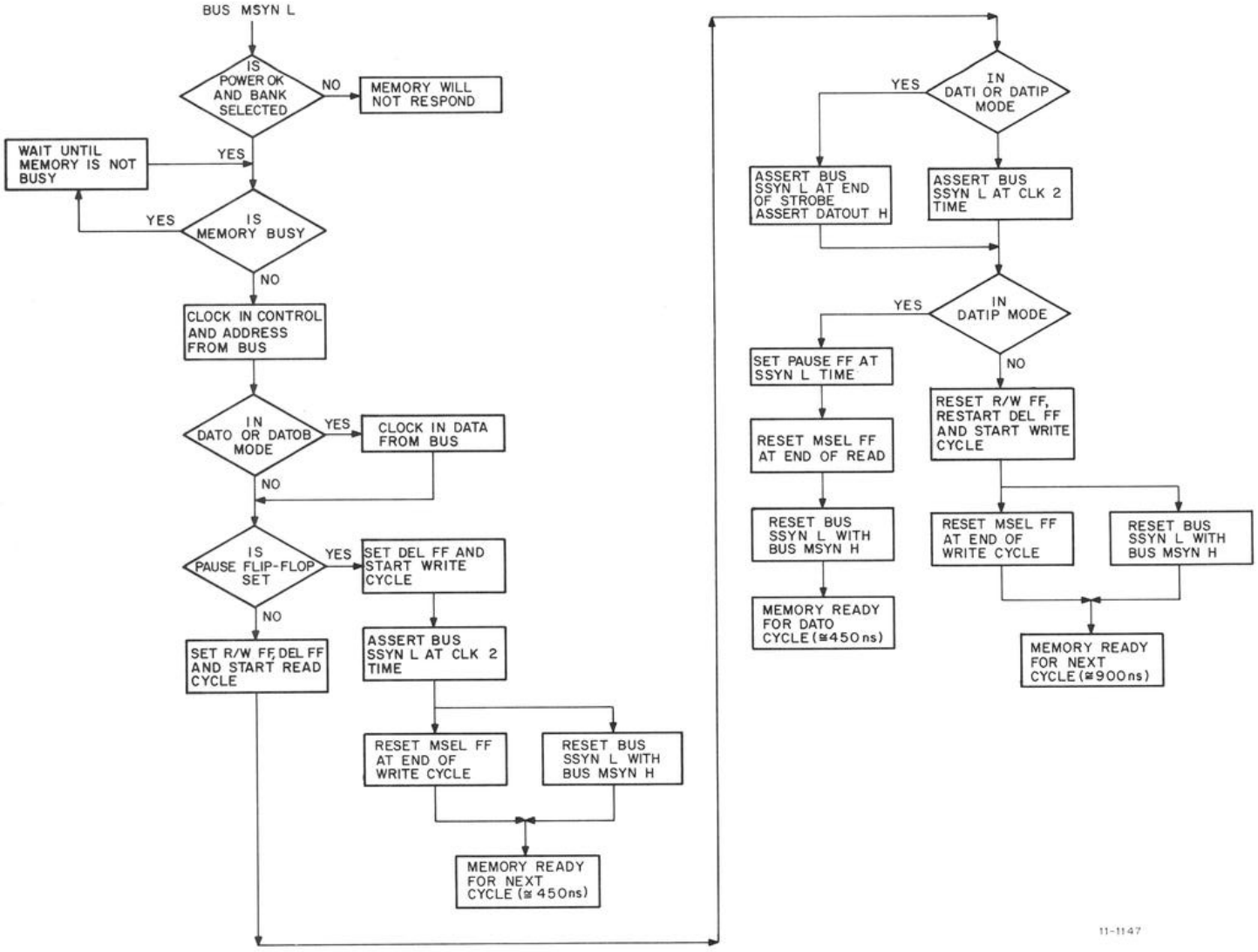


Figure 2-27 Flow Chart For Memory Operation

timed to arrive at the same time as the pulses induced in the sense/inhibit line. If a selected core was a 1, a pulse is induced in the sense/inhibit line that exceeds the sense amplifier threshold and it produces an amplified positive pulse. This output is inverted, presets its associated MDR flip-flop, and a 1 is stored in the flip-flop. STROBE H also clocks the SSYN flip-flop which resets. The SSYN flip-flop output asserts DATA OUT H and BUS SSYN L. Signal DATA OUT H gates the output of the memory data register to the Unibus. BUS SSYN L is a Unibus signal that informs the master that the memory has read the selected location and placed the data on the Unibus. The master takes the data and clears BUS MSYN L which generates SSYN RESET L to set the SSYN flip-flop. BUS SSYN L is cleared to indicate that the Unibus is free; however, another bus transaction cannot be initiated even if the master asserts BUS MSYN L because of the lockout feature of the MSEL flip-flop, which is still set. Prior to the assertion of BUS SSYN L, the timing chain generates DELAY FF RESET L which resets the DEL flip-flop and allows the TNAR H and TWID H pulses to terminate as a function of taps 5 and 7 of the delay line. The timing chain also generates R/W RESET L which resets the R/W flip-flop.

The memory now enters the write (or restore) cycle. With the R/W flip-flop and PAUSE flip-flop both reset, the pause/write restart circuit generates WRITE RESTART L which initiates another timing cycle by setting the DEL flip-flop.

The timing chain generates TWID H and TNAR H. These signals plus a low READ H signal from the R/W flip-flop go to the driver module to select the appropriate write drivers and switches, turn on the X and Y current generators, and control the stack discharge circuit. In addition, TWID H and an output from the R/W flip-flop are ANDed to generate TINH 0 H and TINH 1 H. These signals control the operation of the inhibit drivers. TINH 0 H and TINH 1 H are ANDed with the outputs of the MDR flip-flops. If a 1 is stored in the MDR flip-flop, the associated inhibit driver is not turned on and a 1 is written into this bit of the selected memory location. If a 0 is stored in the MDR flip-flop, the associated inhibit driver is turned on and produces a current that opposes the Y line current and prevents a 1 from being written into this bit. The timing chain generates DELAY FF RESET L which resets the DEL flip-flop and allows TNAR H, TWID H, and the inhibit pulses (TINH 0 H AND TINH 1 H) to terminate. The timing chain also generates MSEL RESET L which resets the MSEL flip-flop.

2.9.7 Data In Pause (DATIP) Operation

In a DATIP operation, the master requests that a selected memory location be read and the information transferred to the master via the Unibus. However, unlike the DATI, this information is not to be restored after reading; this location is to have new information written into it. The DATIP performs only a read operation; the write operation is inhibited. A DATIP must always be followed by a write transaction (either DATO or DATOB).

The read operation of a DATIP is identical to that of a DATI (Paragraph 2.9.6) until the time the SSYN flip-flop is reset (clocked by STROBE H). At this time, the SSYN flip-flop output clocks the PAUSE flip-flop which sets it because its D-input is a 1 (only during DATIP due to the state of mode control bits C01 and C00). The timing chain generates R/W RESET L which resets the R/W flip-flop. The output of the PAUSE flip-flop and R/W flip-flop prevents the pause/write restart circuit from generating WRITE RESTART L. With this signal inhibited, the write operation is not produced. The timing chain generates DELAY FF RESET L which resets the DEL flip-flop and terminates TNAR H and TWID H. The timing chain also generates MSEL RESET L which resets the MSEL flip-flop. The memory is now ready to accept another request from the master. The next cycle is forced to be a DATO or DATOB. Normally, a DATO or DATOB starts with a read operation to set all selected cores to 0 (clear) before writing new information into them. A DATO or DATOB following a DATIP has this initial clear operation eliminated because the cores have been cleared by the previous DATIP operation.

The DATO or DATOB following a DATIP starts when the master asserts BUS MSYN L. Pulse CLK 1 is generated but it does not set the R/W flip-flop because the PAUSE flip-flop is set. The master places the information to be written on the Unibus where it is picked off by bus receivers and sent to the D-input of the memory data resigter flip-flops. Decoding the mode control bits (C01 and C00) for a DATO or DATOB generates LOAD 0 H and LOAD 1 H which clock the MDR flip-flops. The outputs of the MDR flip-flops are gated with TINH 0 H and TINH 1 H to control the associated inhibit drivers to write 1s or 0s into the selected memory location. As in the write operation of a DATI, the timing chain generates TWID H and TNAR H which select the appropriate write drivers and switches, turn on the X and Y current generators, and control the stack discharge circuit. They also generate inhibit driver control signals TINH 0 H and TINH 1 H. Signal CLK 2 H clocks the SSYN flip-flop (resets it) which asserts BUS SSYN L to tell the master that the data has been taken from the Unibus. When the master clears BUS MSYN L, the SSYN flip-flop is reset which in turn resets the PAUSE flip-flop. At the end of the write operation, the timing chain generates DELAY FF RESET L and MSEL RESET L to restore the control signals to their original states.

2.9.8 Data Out (DATO) Operation

In a DATO operation, the master sends a word of 16 bits to be written into the selected memory location. The transaction starts with a read (clear) operation to set the selected cores to 0 before writing new data into them. The standard DATO consists of a read operation followed by a write operation. (As described in Paragraph 2.9.7, a DATO following a DATIP does not perform read operation.)

The read operation of a DATO is similar to a read operation of a DATI except that no RESET 0 L, RESET 1 L, STROBE 0 H, and STROBE 1 H pulses are generated. The memory data register is not cleared and the sense amplifiers are not strobed. This read operation is required only to clear the memory location by setting all the selected cores to 0; it is not necessary to readout and store the information in the MDR.

The information on the Unibus data lines is sent to the inputs of the MDR flip-flops. Decoding the mode control bits (C01 and C00) generates LOAD 0 H and LOAD 1 H which clock the MDR flip-flops. The MDR outputs (16 bits) are gated with TINH 0 H and TINH 1 H to control the associated inhibit drivers. The timing chain generates the other control signals that provide the selection of the appropriate write drivers and switches and a write operation is initiated. This write operation is the same as that described in Paragraph 2.9.7 for a DATO following a DATIP.

2.9.9 Data Out Byte (DATOB) Operation

In a DATOB operation, the master sends a byte (8 bits) to be written into the selected memory location. A high byte (bits D⟨15:08⟩) or a low byte (bits D⟨07:00⟩) can be selected. Byte selection is made by the state of address bit A00. A DATOB is the same as a DATO except that the selected and non-selected bits are handled differently.

Assume that the low byte (bits D⟨07:00⟩) is selected (A00=0). Neither RESET 0 L or STROBE 0 H are generated for the selected byte because new data is to be written into bits D⟨07:00⟩ (low byte). LOAD 0 H is generated so that the data on Unibus bits D⟨07:00⟩ can be written into the selected byte location.

The non-selected byte (bits D⟨15:08⟩) is to be restored so RESET 1 L and STROBE 1 H are generated; this strobes the byte into the MDR for restoration during the write operation. Restoration is necessary because this byte does not receive new data. LOAD 1 H is not generated; therefore, any data on Unibus bits D⟨15:08⟩ has no effect on the non-selected byte.

When the DATOB is complete, the selected byte contains new data and the non-selected byte remains unchanged.

A DATOB operation following a DATIP is the same, except that the read portion is eliminated.

CHAPTER 3
MAINTENANCE

3.1 INTRODUCTION

This chapter discusses the preventive and corrective maintenance procedures that apply to the MM11-L memory. A major point in the maintenance philosophy of this manual is that the user understand the normal operation of the memory as described in Chapter 2. This knowledge, plus the maintenance information included in this chapter, will aid the user in isolating and correcting malfunctions.

3.2 PREVENTIVE MAINTENANCE

Preventive maintenance consists of specific tasks performed at intervals to detect conditions that could lead to subsequent performance deterioration or malfunction. The following tasks are considered preventive maintenance items.

a. Visual inspection of modules for broken wires, broken connectors, or other obvious defects.

b. +5V and −15V checks: both must be within ±3 percent tolerance.

c. X and Y current generator check (Paragraph 3.2.2).

The two pieces of test equipment recommended for checking and troubleshooting the memory are the Tektronix 453 dual trace oscilloscope or equivalent, and the Honeywell 33R Digital Voltmeter or equivalent with 0.5 percent accuracy.

3.2.1 Initial Procedures

Before attempting to check, adjust, or troubleshoot the memory, perform the following steps.

NOTE
All tests and adjustments must be performed in an ambient temperature range of 20°C to 30°C (68°F to 86°F).

1. Verify that all modules are properly and securely installed.

CAUTION
Make sure all power is off before installing or removing modules.

2. Visually check modules and backplane for broken wires, connectors, or other obvious defects.

3. Verify that power buses are not shorted together.

(continued on next page)

4. Turn on primary power and check that both the –15V and +5V powers are present and within tolerances (±3 percent).

5. Start the system. The memory should operate without errors. If not, check the output of the current generator (Paragraph 3.2.2). If the memory still does not operate properly, a malfunction has occurred. Proceed with corrective maintenance (Paragraph 3.3).

3.2.2 Checking Output of Current Generators

The amplitude of the current pulse from each current generator (X and Y) is factory set at 410 ±5 mA. It is not adjustable in the field.

The X and Y current generators are located on the Driver Module (G231). Each output has a current loop on its output line for attaching a test probe. Loop J5 is for the Y generator and loop J6 is for the X generator (Drawing G231-0-1, sheet 2). The amplitude of each READ current pulse should be 410 ±5 mA. At the time of measurement, –15V and +5V power must be within the specified tolerance of ±3 percent.

3.3 CORRECTIVE MAINTENANCE

This paragraph describes the strobe delay adjustment which is a specific corrective maintenance procedure. It also includes three aids for performing corrective maintenance: a troubleshooting chart, waveforms for the sense inhibit circuits, and waveforms for the drive circuits.

3.3.1 Strobe Delay Check and Adjustment

CAUTION

Strobe delay is factory adjusted and should be adjusted only when one of the three modules is replaced. It is a critical adjustment and must be done carefully.

The strobe must be set while cycling worst case patterns. The proper setting is mid-way between the two end points where the memory starts to error as strobe time is moved from earliest to latest. As the strobe time is varied, allow adequate time to cycle completely through the worst case pattern at each strobe position. Figure 3-1 shows the strobe pulse waveform and the READ pulse waveform and the points at which they are picked off for display.

3.3.2 Corrective Maintenance Aids

Figure 3-2 is a troubleshooting chart arranged as a 2-axis grid that identifies faults versus cause location. Figure 3-3 illustrates the sense/inhibit waveforms and Figure 3-4 illustrates the drive waveforms; both figures include schematics to indicate the points in the circuit where the waveforms occur. In addition to nominal waveforms, dotted lines are used to indicate waveforms that appear if specific components are faulty.

3.4 PROGRAMMING TESTS

Certain DEC programs can be used to test various memory operations as an aid to troubleshooting. The purpose of each of these memory-related test programs, as well as the program abstract, is given in the following paragraphs. Each program contains instructions for use.

3.4.1 Address Test Up (MAINDEC-11-DZMMA)

The purpose of the Address Test Up program is to demonstrate that the selected memory area is capable of basic read and write operations when address propagation is upward through memory.

This test program writes the address of each memory location (within the test limits) into itself and then increments through memory until the address corresponding to the high limit is reached. After this location has been written, the memory enters the read cycle. The read cycle starts with the high limit location and reads and compares each word location, decrementing down to the low limit location. The program halts on an error.

This program checks that all addresses are selectable and can also be used to isolate bad switches, wiring errors, or address selection errors. It will also find double selection errors when two bus addresses select the same core address.

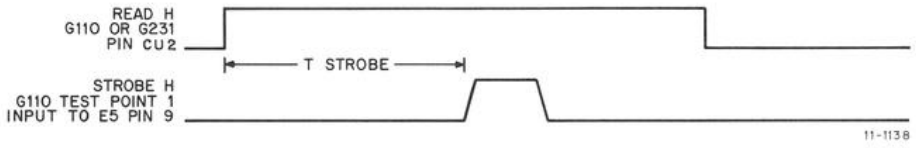


Figure 3-1 Strobe Pulse Waveform

3.4.2 Address Test Down (MAINDEC-11-DZMMB)

The purpose of the Address Test Down program is to demonstrate that the selected memory area is capable of basic read and write operations when address propagation is downward through memory. It is a companion test to the Address Test Up program (Paragraph 3.4.1).

This test program writes the address of each location into itself, downward through memory. After writing down, the program reads and checks back up through the memory test area. The program halts on an error.

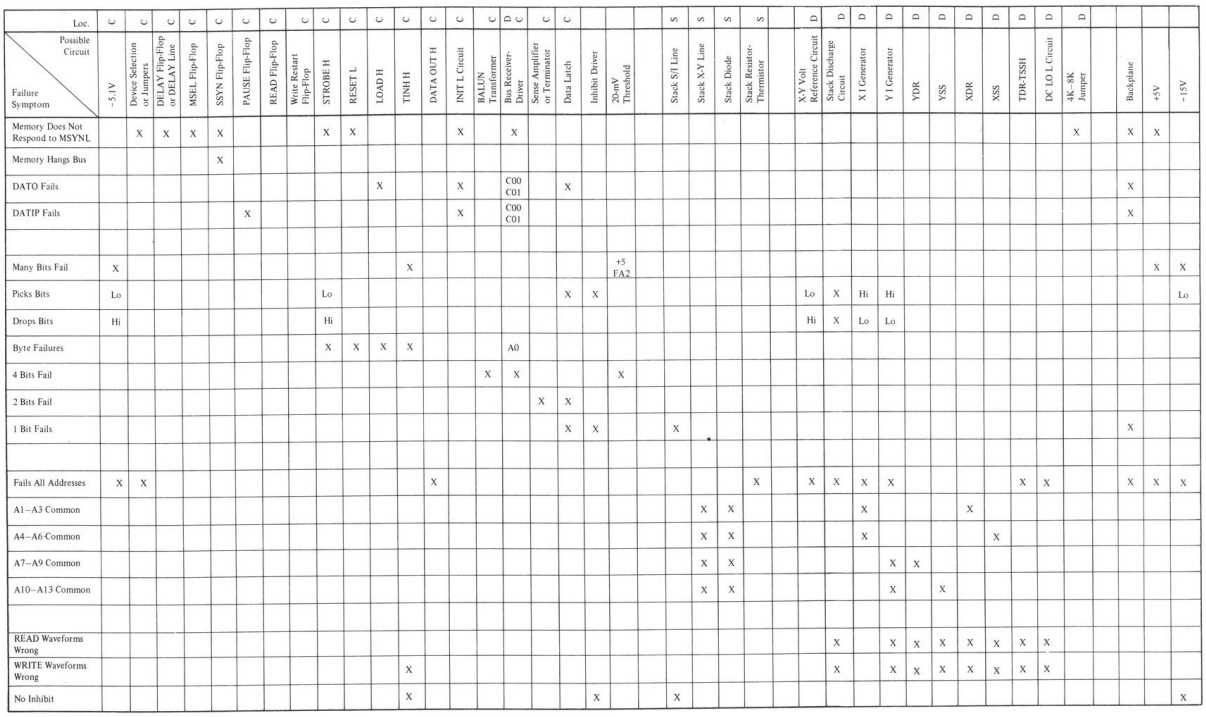
The Address Test Down program resides in the high portion of core memory. It does not check memory below address 100, as these locations are reserved for trap and vector locations. The program verifies that all modules can perform their basic functions, checks that all addresses are selectable, and can also be used to isolate faulty switches, wiring errors, or address selection errors.

3.4.3 No Dual Address Test (MAINDEC-11-DZMMC)

The purpose of the No Dual Address Test program is to check the unique selection of each memory address tested.

This test is divided into two parts. The first portion of the test fills the test field with 1s and writes 0s into the first test location. This is followed by a read check from this location. The program then checks each field location to ensure that there are no variations from the 1s configuration. Upon completion of this test, the test location pointer is incremented. The next location is then write-read exercised with 0s and the test field rechecked for any change in content. When the selected test field has been tested in this mode, the program sets a flag and the second portion of this mode, the program sets a flag and the second portion of the test is begun. The program fills the test field with 0s and the field is then tested with a write-read exercised with 1s.

This program checks for faulty switches or wiring errors, checks the complete address selection scheme, and checks all 16 bits in the data field for 1s and 0s operation.

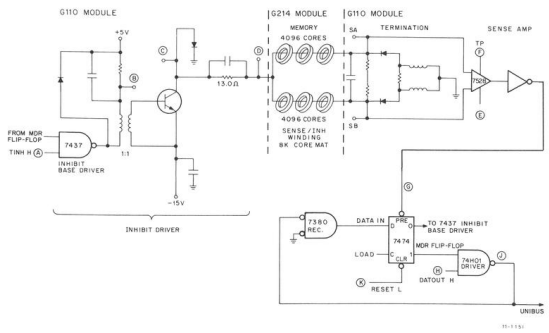


Loc.	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	S	S	S	S	D	D	D	D	D	D	D	D	D	D	D	D				
Possible Circuit / Failure Symptom	−5.1V	Device Selection or Jumpers	DELAY Flip-Flop or DELAY Line	MSEL Flip-Flop	SSYN Flip-Flop	PAUSE Flip-Flop	READ Flip-Flop	Write Restart Flip-Flop	STROBE H	RESET L	LOAD H	TIMH H	DATA OUT H	INT L Circuit	BALUN Transformer	Bus Receiver-Driver	Sense Amplifier or Terminator	Data Latch	Inhibit Driver	20mV Threshold		Stack S/I Line	Stack X-Y Line	Stack Diode	Stack Resistor-Thermistor		X-Y Volt Reference Circuit	Stack Discharge Circuit	X I Generator	Y I Generator	YDR	YSS	XDR	XSS	TDR-TSSH	DC LO L Circuit	4K–8K Jumper		Backplane	+5V	−15V
Memory Does Not Respond to MSYNL		X	X	X	X				X	X				X		X																				X		X	X	
Memory Hangs Bus					X																																				
DATO Fails											X			X		C00 C01		X																						X		
DATIP Fails						X								X		C00 C01																								X		
Many Bits Fail	X											X								+5 FA2																				X	X
Picks Bits	Lo								Lo									X	X								Lo	X	Hi	Hi											Lo
Drops Bits	Hi								Hi																		Hi	X	Lo	Lo											
Byte Failures									X	X	X	X				A0																									
4 Bits Fail															X	X				X																					
2 Bits Fail																	X	X																							
1 Bit Fails																		X	X			X																	X		
Fails All Addresses	X	X											X												X		X	X	X	X					X	X			X	X	X
A1–A3 Common																							X	X					X			X									
A4–A6 Common																							X	X					X				X								
A7–A9 Common																							X	X						X	X										
A10–A13 Common																							X	X						X		X									
READ Waveforms Wrong																												X		X	X	X	X	X	X	X	X				
WRITE Waveforms Wrong												X																X		X	X	X	X	X	X	X	X				
No Inhibit												X							X			X																			X

Location { C = G110 Sense Control; S = Stack; D = G231 Driver }

X = Indicates Circuit Not Operable
Lo = Measured Parameter Too Low or Early
Hi = Measured Parameter Too High or Late

Figure 3-2 Troubleshooting Chart



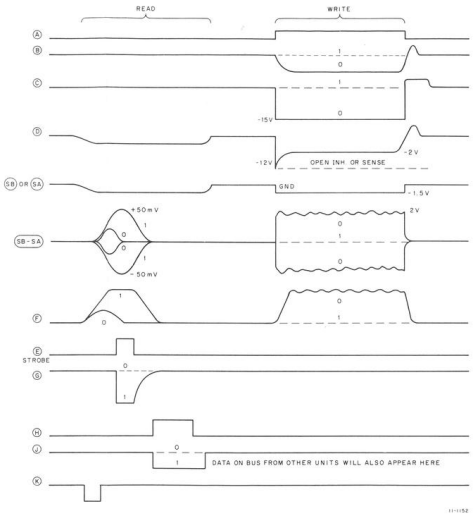
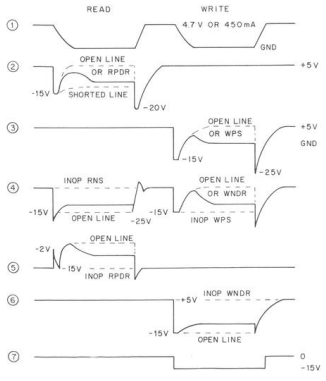


Figure 3-3 MM11-L Sense/Inhibit Waveforms



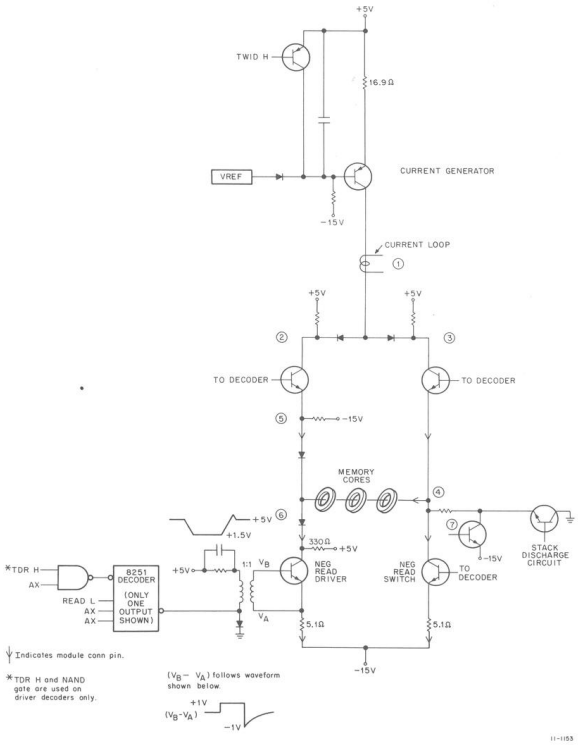


Figure 3-4 Drive Waveforms

3.4.4 Basic Memory Patterns Test (MAINDEC-11-DZMMD)

The Basic Memory Patterns Test program has two main purposes:

a. Verify that the selected memory test field is capable of writing and reading fixed data patterns.

b. Verify that the memory plane is properly strung.

This test program writes a specific pattern throughout a given memory zone, then reads the pattern back and compares it with the original for correctness. If the pattern read fails to compare correctly with the original, the program initiates a call to the error subroutine. After completely checking the pattern, the program continues on to the next pattern test.

3.4.5 0–124K Memory Exerciser (MAINDEC-11-DZQMB)

The purpose of the 0–124K Memory Exerciser is to verify that each memory address is unique and that it can be reliably written into and read. It is a combination of an address test and worst case noise test. The program tests contiguous memory addresses from 000000 to 757776. The KT11-C or KT11-D Memory Management option must be installed in order to run the program. Execution time is approximately one minute per each 4K of memory.

This test program is designed to produce the greatest amount of plane noise possible during memory read and write cycles. The noise parameters are affected by a number of factors. The noise generated is distributed across the core plane algebraically and adds to the normal dynamic noise present on the sense lines. This can cause misreading of data (within the plane) that is in the low (1) or high (0) category. The sense windings of the most memories are such that worst case patterns can be caused by alternately writing –1 and 0 data configurations throughout memory. Under these conditions, worst case noise is generated by performing a read, write, complement, read, write, complement, operation at each location. The test is repeated after complementing all of the pattern data stored in the memory test zone, so that all cores are tested worst case as both 1s and 0s. The pattern, or its complement, is written into the memory test zone as determined by the exclusive-OR between address bits 3 and 9.

If the program indicates an error, use the troubleshooting chart as a guide to locate the fault.

APPENDIX A
MM11-LP PARITY MEMORY

A.1 INTRODUCTION

This appendix contains a description of the theory and operation of the MM11-LP Parity Memory and the M7259 Parity Controller. Inasmuch as the MM11-LP is similar in operation to the MM11-L memory, which is described in the main body of this manual, only those areas of operation which are unique to the MM11-LP are covered in this appendix.

A.2 DESCRIPTION

The MM11-LP Parity Memory comprises three modules: a G109 Control Module, a G231 Drive Module, and an H215 18-bit Stack Module. Additionally, one M7259 Parity Controller Module (Figures A-1 and A-2) is required for each 24K words of memory (three MM11-LPs). Bits 16 and 17 are the parity bits for the low order and high order bytes, respectively. These bits are the property of the parity controller and are not accessible via the PA or PB Unibus lines. On parity generation (DATO), both the low order and high order bytes are coded for odd parity; thus, for every byte containing an even number of 1s, a 1 is written into its respective parity bit location.

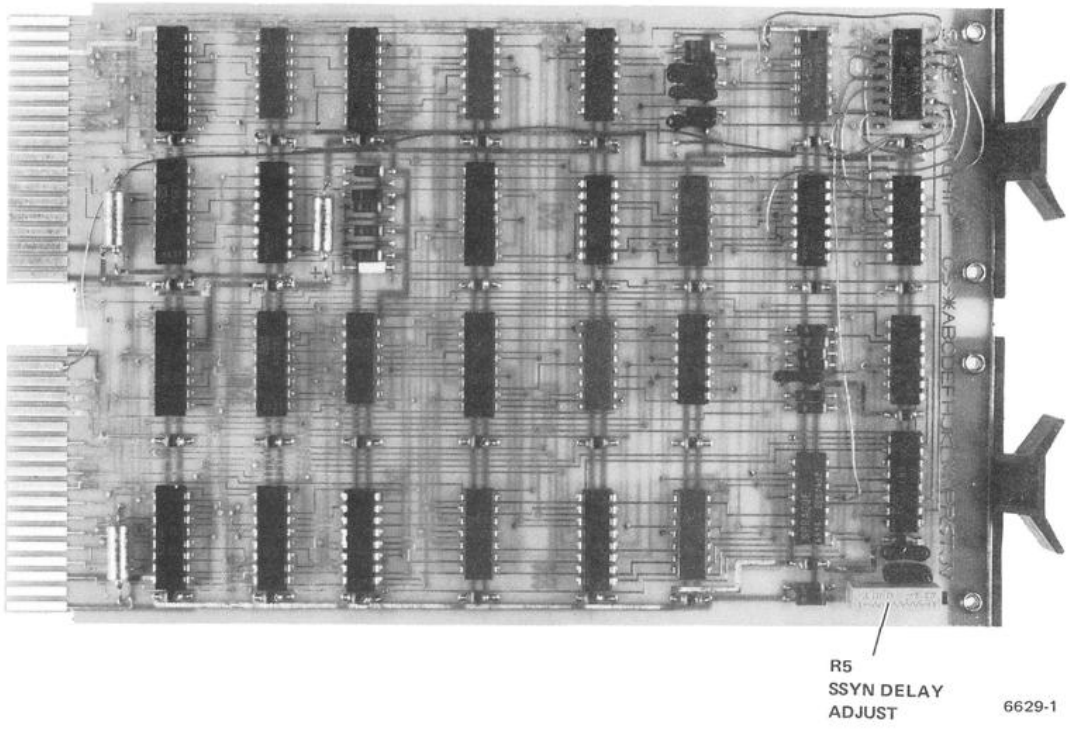


Figure A-1 Component Side of M7259 Parity Controller Module, Etch Rev C, CS Rev D

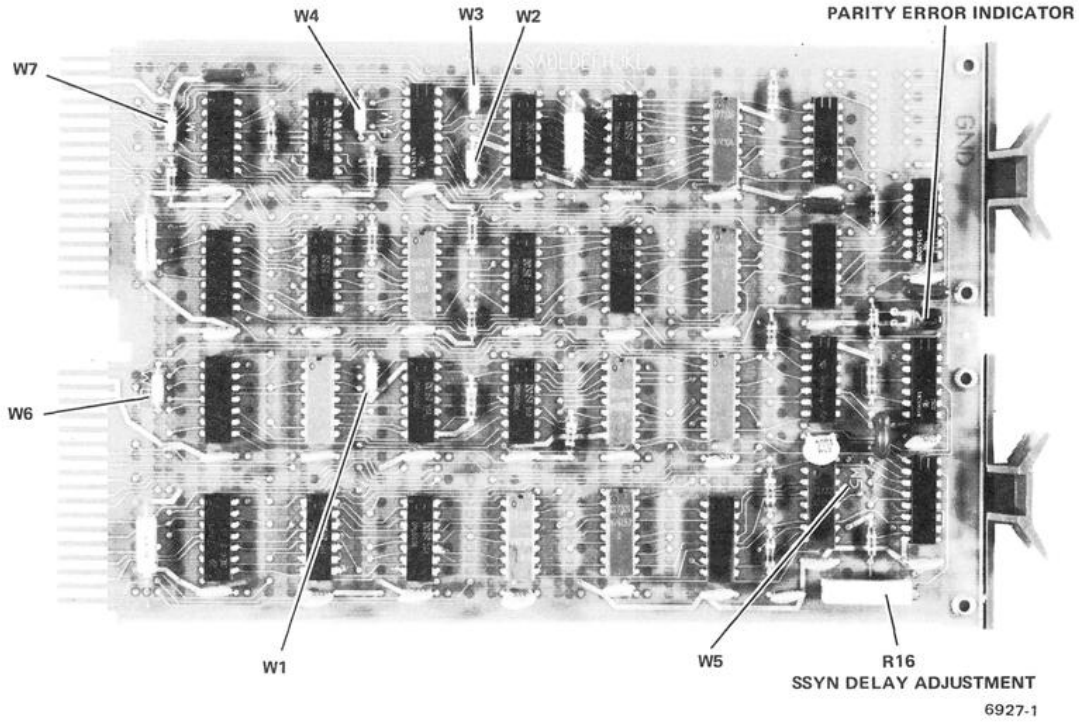


Figure A-2 Component Side of M7259 Parity Controller Module, Etch Rev D, CS Rev E

For parity checking (DATI or DATIP), each byte plus its corresponding parity bit is checked for an odd number of 1s. An error condition exists if the sum of 1s is even. If a parity error is detected during a DATIP cycle, the bad data which caused the parity error is saved and written back into core.

The M7259 Parity Controller Module performs all parity generation and checking functions.

A.3 SPECIFICATIONS

The specifications of the MM11-LP are given in Table A-1. The specifications of the M7259 Parity Controller are given in Table A-2.

Table A-1

MM11-LP Specifications

Type: Magnetic core, read/write, coincident current random access

Organization: Planar, 3D, 3-wire

Capacity: 8192 (8K) 18-bit words

Access time and Cycle time:

Bus Mode	Access Time		Cycle Time		Selection of Alternate Memory*	
	A	B	A	B	A	B
DATI	400 ns	525 ns	900 ns	900 ns	550 ns	675 ns
DATIP	400 ns	525 ns	450 ns	525 ns	550 ns	675 ns
DATO-DATOB (Pause L)	200 ns	200 ns	900 ns	900 ns	350 ns	350 ns
DATO-DATOB (Pause H)	200 ns	200 ns	450 ns	450 ns	350 ns	350 ns

A = Parity error indication not enabled
B = Parity error indication enabled
* Minimum time during which the Unibus is available to select next interleaved memory

X-Y Current Margins: ±6% @ 0°C, ±7% @ 25°C, ±6% @ 50°C

Strobe Pulse Margins: ±30 ns @ 0°C, ±40 ns @ 25°C, ±30 ns @ 50°C

Voltage Requirements: +5V ±5% with less than 0.05V p-p ripple
−15V ±5% with less than 0.05V p-p ripple

Average Current Requirements: Standby: +5V; 1.8A
−15V; 0.6A

Memory Active: +5V; 3.6A
−15V; 6.5A

Power Dissipation:
G109 Control Module: ≃ 70W
G231 Drive Module: ≃ 40W
H215 Stack Module: ≃ 20W
Total at maximum repetition rate: ≃ 130W

Environment:
Ambient Temperature: 0°C to 50°C (32°F to 122°F)
Relative Humidity: 0 to 90% (non-condensing)

Table A-2
M7259 Parity Controller Specifications

Voltage Requirements:	+5V ±5% with less than 0.05V p-p ripple
Current Requirements:	1.2A
Power Dissipation:	6W
Environment:	Ambient Temperature: 0°C to 50°C (32°F to 122°F) Relative Humidity: 0 to 90% (non-condensing)

A.4 FUNCTIONAL DESCRIPTION

The MM11-LP memory is a read/write, random access, coincident current, magnetic core parity memory with a cycle time of 900 ns and an access time of 525 ns maximum. It is organized in a 3D, 3-wire planar configuration. Word length is 18 bits, 2 of which are the parity bits, and the memory capacity is 8192 (8K) words.

The operation of the MM11-LP memory is identical to that of the MM11-L memory except for the parity generation and checking functions. In order to implement this option, an 18-bit stack module (H215) is used, bits 17 and 16 being the parity bits, and an additional parity controller module is required. The controller is a dual height module (M7259) which plugs into the memory system backplane; it contains all the logic used to generate and check parity, and a control and status register (CSR). A schematic diagram of the parity controller is shown on engineering drawing D-CS-M7259. Odd parity is used: if the number of 1s in a given byte is even, then a 1 will be written into the respective parity bit location. The use of odd parity allows detection of a memory failure of all 0s, which is a more probable failure mode than all 1s.

Error indication can be disabled or enabled under program control. If parity error indication is enabled, a parity error will cause the processor to enter a trap service routine through vector address 114. The error action is fully described in Paragraph A.5. On parity generation (DATO), both the low order (D00 to D07) and the high order (D08 to D15) bytes are coded. The Unibus data is applied through buffers to the inputs of E4 and E13 on the M7259. The outputs of these ICs will be high if their respective inputs contain an odd number of 1s, and thus cause the PA or PB parity bits to be set. The PA bit is the parity bit for the high order byte and the PB bit is the parity bit for the low order byte. The BUS C1 L signal to the M7259 parity controller indicates whether parity is to be generated or checked.

For parity checking (DATI or DATIP), the same two ICs which were used for generation are used; in this case, however, a low output indicates a parity error. During the memory read cycle, the signal SSYN INT BUS L is sent to the parity controller to indicate that memory data is present on the Unibus. This signal initiates a 105 ns timing sequence (PC2 SSYN DLY L) to allow for worst case propagation delays of data through the memory data drivers, parity controller data receivers, and the parity tree and checking logic.

At the trailing edge of PC2 SSYN DLY L, if each byte and its respective pairty bit contain an odd number of 1s, parity is confirmed as being good, and PC2 PARITY ERROR H is low. This condition permits SSYN to be sent to the bus master as an indication that data is available and valid. If a parity error is detected, however, PC2 PARITY ERROR H is asserted, causing flip-flop PC2 PARITY ERROR to set. This flip-flop, when set, enables BUS PB (parity error indication to the bus master if CSR0=1), sets CSR15 (parity error bit in CSR), and triggers PC2 PARITY ERROR DLY which in turn enables BUS SSYN to the bus master. The BUS PB signal indicates to the bus master that a parity error has occurred during the current DATI or DATIP cycle.

If CSR0 is not set, the above sequence is abbreviated and SSYN INT BUS directly becomes BUS SSYN as parity is being checked.

A.4.1 DATIP Cycle

Since the restore portion of the memory cycle is skipped during a DATIP operation, provisions must be made to save bad data in core in the event of a parity error during DATIP. The operation of the parity controller checking and timing sequence is the same as during a DATI operation, except that if PC2 PARITY ERROR DLY is generated, it will cause a 400 ns pulse, DATIP CLR PAUSE L, to be generated. This signal causes the memory to restore the bad data, and also eliminates the requirement for the write cycle which would otherwise have to follow.

A.4.2 DATO Cycle

During a normal DATO cycle (i.e., a DATO which does not follow a DATIP), parity is being generated during the read portion of the memory cycle. The Unibus data along with the proper parity bits are transferred into a data register on the G109. SSYN is then returned to the bus master via the parity controller to indicate that data has been strobed from the bus. Data is transferred from the data register to core during the write cycle.

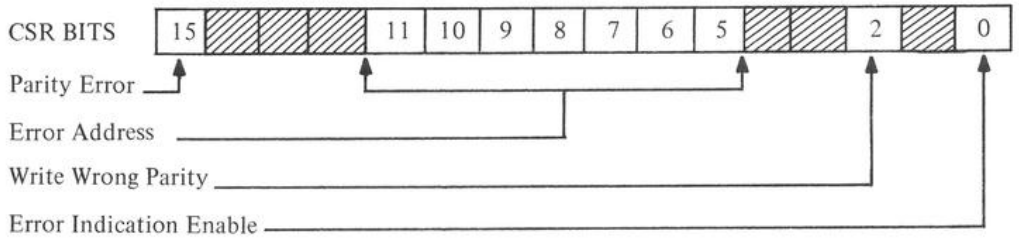
If the DATO follows a DATIP, the sequence is altered. During the DATIP, the memory location will have been cleared and a pause flag set. When the DATO occurs, the read cycle will be skipped, and the write cycle begun immediately. The data and parity bits are transferred from their respective buses as the beginning of the write cycle, at which time SSYN is generated.

The DATOB cycle is similar to the DATO except that during the DATOB, data is written in byte form rather than as a full word. The non-selected byte is simply restored along with the new data in the selected byte plus the parity bits.

A.5 PROGRAMMING

A.5.1 Control and Status Register (CSR)

The CSR is located on the M7259 parity controller. There is one CSR per 24K of memory. Transfer of a 16-bit control word from the processor to the CSR establishes the operating conditions of the MF11-LP. The data format of the CSR is shown below:



NOTES: 1. All bits are read/write.
2. All bits except the error address bits are cleared by INIT.

Bit	Name	Description
15	PARITY ERROR	Set when a parity error occurs regardless of whether any other response is enabled.
11–5	ERROR ADDRESS	Contains the highest order address bits of the most recent location causing a parity error.

Bit	Name	Description
2	WRITE WRONG PARITY	Causes the controller to generate incorrect parity on write cycles (DATO + DATOB), forcing a parity error on the next DATI or DATIP cycle. This bit is intended for use as a diagnostic aid.
0	ERROR INDICATION ENABLE	Enables error indications to the bus master when set.

A.6 INTERFACE SPECIFICATIONS

A.6.1 Bus Loading

An MF11-LP represents two bus loads; one for the MM11-LP 8K Parity Memory Module set, and the other for M7259 Parity Controller. Each additional MM11-LP 8K module set adds one bus load. Therefore the MF11-LP expanded to 24K would represent four bus loads.

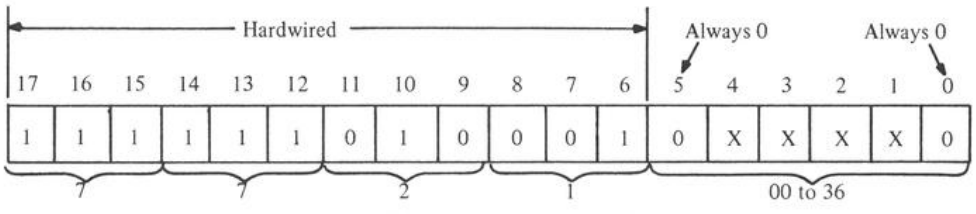
A.6.2 Internal Bus

The internal bus [Figure 1-4 (c)] is the communication path between the M7259 Parity Controller and the G109 Control Module. It comprises the following signals:

Name	Function
SSYN INT BUS L	Signal the parity controller when data is available on the Unibus to begin parity checking sequence.
PB INT BUS L (D17)	A bi-directional path which carries the generated parity bit to memory on DATO cycles and from memory to the controller on DATI cycles. This is the parity bit for the high order byte (D15 → D08).
PA INT BUS L (D16)	Same as PB INT BUS L except that it is the parity bit for the low order byte (D07 → D00).
DATIP CLR PAUSE L	Clears the PAUSE flip-flop in the G109 Control Module if a parity error occurs on a DATIP cycle.
DATIP CLR PAUSE (1) L	Not used with the MM11-LP.

A.6.3 CSR Address Selection

The address of the CSR is hardwired in the range of 772100 to 772136. Jumpers W1 through W4 (refer to Figures A1 and A2 for jumper locations) determine the discrete address.



X = Bit values selected by Jumpers W4 – W1

CSR ADDRESS

Table A-3 shows the CSR addresses for all possible memory starting addresses and their jumper configurations. For example, if the lowest address memory responds to is 28K, the jumpers are cut for address 722110. If the lowest address memory responds to is 32K, the jumpers are also cut for address 772110. This is because the CSR addresses are assigned on a basis of 8K of memory. Thus, there are 16 unique addresses in the table.

Table A-3 relates the Bus address lines to the two different configurations of jumper designations. On newer modules (M7259 etch revision D, CS revision E) the jumper designations have been changed to conform with the address line numbering (W1 – A01, W2 – A02, etc.). On the earlier version of the board (M7259 etch revision C, CS revision D), the numbering of the jumpers is in the reverse order of the numbering of the bus address lines. (Refer to drawing D-BD-M7259 to assist with address selection.)

Table A-3
M7259 Parity Controller CSR Address Jumper Selection

CSR Jumpers Etch Rev C, CS Rev D		W1	W2	W3	W4
CSR Jumpers Etch Rev D, CS Rev E		W4	W3	W2	W1
Bus Address Line		A04	A03	A02	A01
Lower Memory Boundary	CSR Address				
0	772100	X	X	X	X
4K	772102	X	X	X	O
8K	772102	X	X	X	O
12K	772104	X	X	O	X
16K	772104	X	X	O	X
20K	772106	X	X	O	O
24K	772106	X	X	O	O
28K	772110	X	O	X	X
32K	772110	X	O	X	X
36K	772112	X	O	X	O
40K	772112	X	O	X	O
44K	772114	X	O	O	X
48K	772114	X	O	O	X
52K	772116	X	O	O	O
56K	772116	X	O	O	O
60K	772120	O	X	X	X
64K	772120	O	X	X	X
68K	772122	O	X	X	O
72K	772122	O	X	X	O
76K	772124	O	X	O	X
80K	772124	O	X	O	X
84K	772126	O	X	O	O
88K	772126	O	X	O	O
92K	772130	O	O	X	X
96K	772130	O	O	X	X
100K	772132	O	O	X	O
104K	772132	O	O	X	O
108K	772134	O	O	O	X
112K	772134	O	O	O	X
116K	772136	O	O	O	O
120K	772136	O	O	O	O

O = Jumper Removed X = Jumper Installed

A.6.4 Interleaving

Interleaving of memories can be accomplished as described in Paragraph 2.4.4.1. However, with parity checking optimum fault isolation in the event of a parity error can be realized only if the memories are interleaved as shown on drawing D-BD-M7259.

A.7 ADJUSTMENT PROCEDURES

This section contains the adjustment procedures pertaining to the M7259 Parity Controller.

A.7.1 PCL SSYN DLY L Adjustment Procedure

This adjustment sets a 125 ns delay from the leading edge of SSYN INT BUS L to allow sufficient settling time for the parity checking logic. Too long a delay will result in increased cycle time and access time. The waveshapes should be as shown in Figure A-3. Adjust R5 (Figure A-1) on the Etch Rev C M7259, or R16 (Figure A-2) on the Etch Rev D M7259 to obtain the required delay.

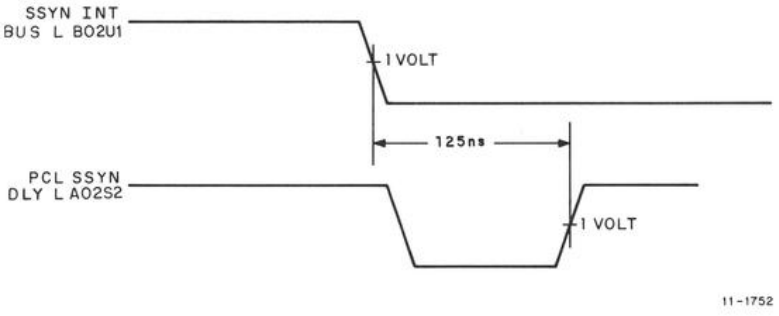


Figure A-3 SSYN DLY L Timing Relationship

A.7.2 Miscellaneous Jumpers W6 and W7

Jumper W7, when removed, will cause the memory controller to hang the Unibus if a memory parity error occurs. Jumper W6 is potentially useful to alter SSYN timing. Normal operation is with W6 installed. There will normally be no occasion to alter the configuration of these jumpers in the field, unless the M7259 is to be used with a memory system other than an MF11-LP.

A.8 PROGRAMMING TESTS

The diagnostic programs listed in Paragraph 3.4 can be used to test various memory operations and as an aid to troubleshooting. Additionally, the following test program is intended for use with the parity memory option.

A.8.1 Parity Memory Test Program (MAINDEC-11-DZMFA)

The parity memory test program has four main purposes:

a. Verify that the parity memory register control logic is operating properly.

b. Verify that the memory is capable of being written into and read from with parity checking enabled.

c. Verify that the detection logic is capable of detecting a parity error.

d. Provide worst case noise test for the parity bit memory planes.

The program is divided into two parts: the first part provides a map showing the locations of parity memory; the second part tests the mapped locations.

APPENDIX B
INTEGRATED CIRCUIT DESCRIPTIONS

B.1 INTRODUCTION

This appendix contains descriptions of the integrated circuits (ICs) depicted by boxes on the MM11-S, MF11-L, and MF11-LP engineering drawings. Those ICs whose functions are readily apparent from the input and output labels, or are described elsewhere in this manual, are not included. The ICs described are listed below.

Type	Function
7485	4-Bit Magnitude Comparator
74157	Quad 2-to-1 Line Multiplexer
74174	Hex D-Type Flip-Flop
74175	Quadruple D-Type Flip-Flop
8266	Quad 2-to-1 Line Multiplexer
82S62	9-Bit Parity Generator and Checker

The descriptions of these ICs include logic diagrams, pin numbers, and truth tables.

B.2 TYPE 7485 4-BIT MAGNITUDE COMPARATOR

This IC performs magnitude comparisons of straight BCD codes. Three fully decoded decisions about two 4-bit words are provided on the output pins. In the M7259 module, this IC performs part of the address decoding. The four LSBs of the address bits are applied to the A inputs; the B inputs are determined by jumpers W1 through W4. Only the A=B output is used.

7485 Truth Table

A=B Input	Comparison Inputs				A=B Output
	A3,B3	A2,B2	A1,B1	A0,B0	
H	A3>B3	X	X	X	L
H	A3<B3	X	X	X	L
H	A3=B3	A2>B2	X	X	L
H	A3=B3	A2<B2	X	X	L
H	A3=B3	A2=B2	A1>B1	X	L
H	A3=B3	A2=B2	A1<B1	X	L
H	A3=B3	A2=B2	A1=B1	X	L
H	A3=B3	A2=B2	A1=B1	A0>B0	L
H	A3=B3	A2=B2	A1=B1	A0<B0	L
H	A3=B3	A2=B2	A1=B1	A0=B0	H
L	X	X	X	X	L

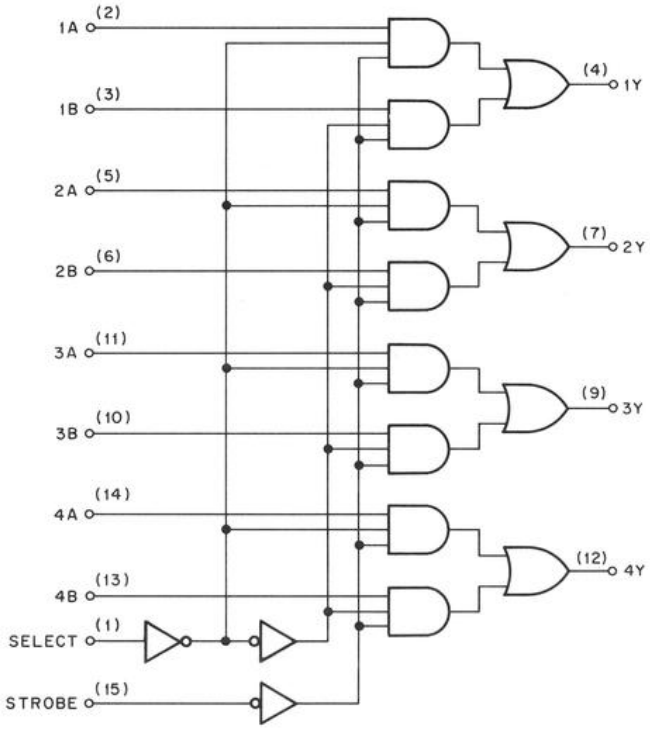
NOTE: A>B and A<B inputs L

B.3 TYPE 74157 QUAD 2-TO-1 LINE MULTIPLEXER

This IC provides selection of either of two 4-bit words. The inputs and outputs are buffered and a strobe input is also provided. The logic schematic and truth table for this device are shown below.

74157 Truth Table

Inputs				Output
Strobe	Select	A	B	Y
H	X	X	X	L
L	L	L	X	L
L	L	H	X	H
L	H	X	L	L
L	H	X	H	H



NOTES:
1. Numbers in parentheses denote pin numbers
2. Pin 16 = V_{CC}
3. Pin 8 = Gnd

11-1755

B.4 TYPES 74174 AND 74175 HEX/QUAD D-TYPE FLIP-FLOPS

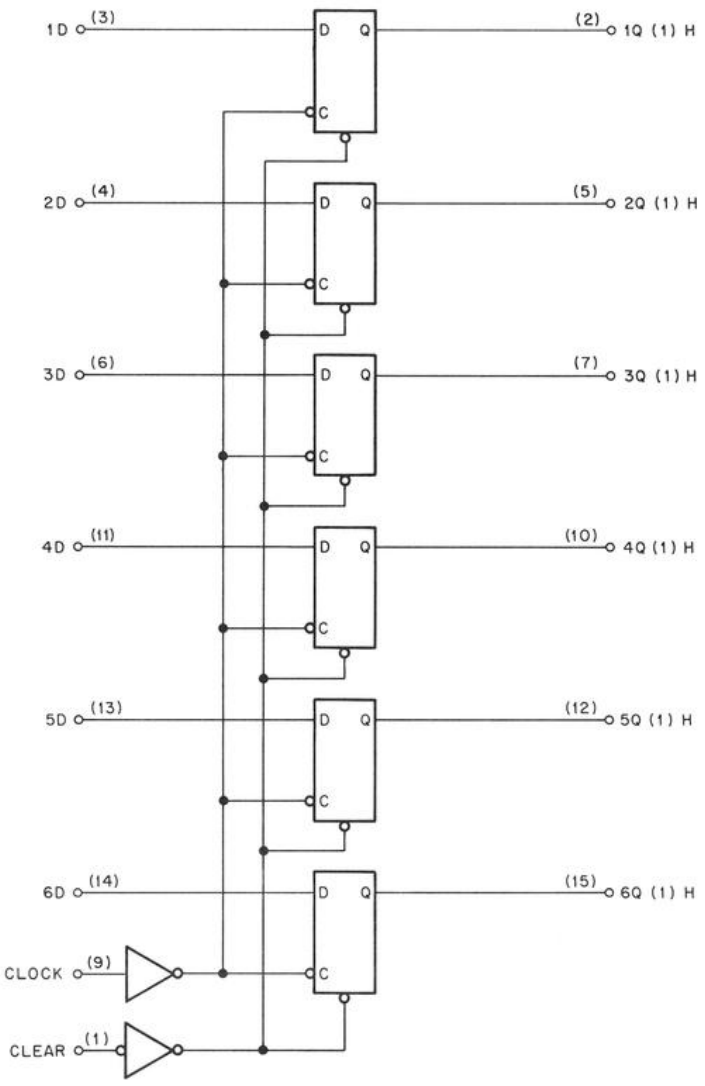
The type 74174 ICs contain six D-type flip-flops with single-rail outputs. The type 74175 ICs contain four D-type flip-flops with double-rail outputs. Both types have direct clear inputs and are triggered by the positive-going edge of an external clock pulse. Information on the D inputs which meets the timing requirements is transferred to the Q outputs at the leading edge of the positive clock pulse. Since the clock triggering occurs at a particular voltage, it is not directly related to the transition time of the clock pulse. With the clock input steady at either the high level or the low level, the D input signal has no effect on the output.

Logic diagrams and function tables for both types are given below.

Function Table
(Each Flip-Flop)

Inputs			Outputs	
Clear	Clock	D	Q	$\overline{Q}$*
L	X	X	H	L
H	↑	H	H	L
H	↑	L	L	H
H	L	X	Q_0	$\overline{Q}_0$

* 74175 only.
↑ = Transition from low state to high state.
Q_0 = Previous state of Q before the indicated steady state conditions were established.

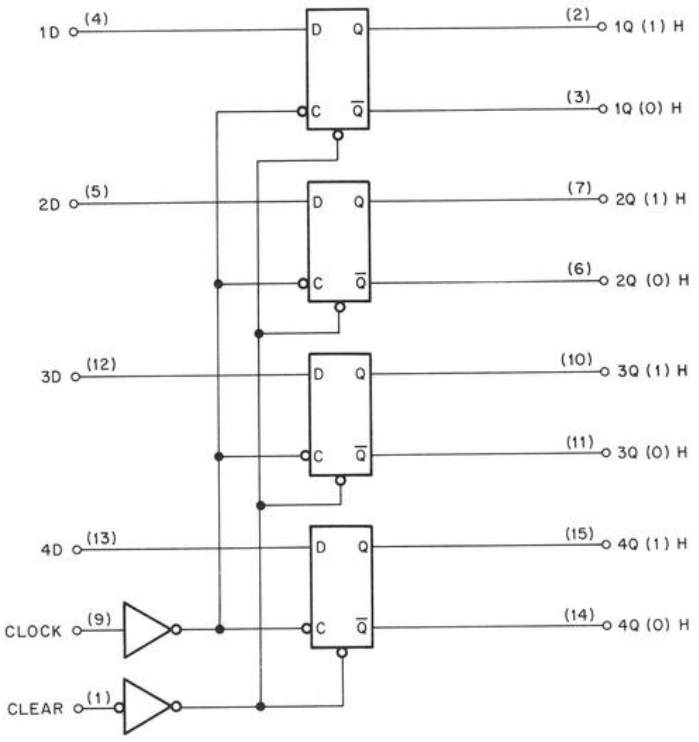


NOTES:

1. Numbers in parentheses denote pin numbers.
2. Pin 16 = V_{CC}
3. Pin 8 = GND

11-1754

74174 Schematic



NOTES:

1. Numbers in parentheses denote pin numbers.
2. Pin 16 = V_{CC}
3. Pin 8 = GND

11-1756

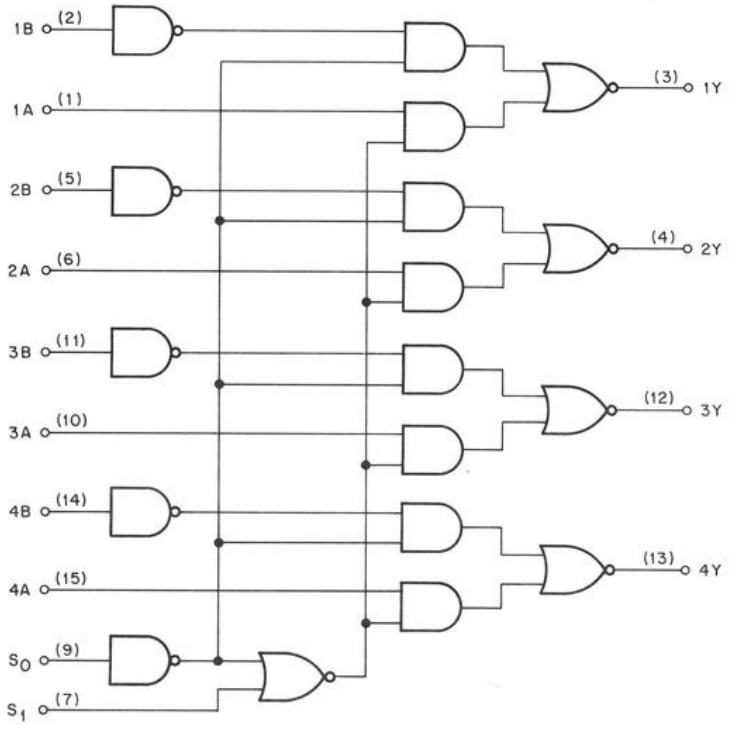
74175 Schematic

B.5 TYPE 8266 QUAD 2-TO-1 LINE MULTIPLEXER

This IC provides selection of either of two 4-bit words. Data applied to the A inputs is inverted, so that its complement appears at the output. Selection is made via two control lines, S_0 and S_1. The selection is controlled by the input at S_0 while S_1 is held low. With S_0 and S_1 both high, the outputs are also high regardless of the inputs. The logic diagram and truth table are given below.

8266 Truth Table

Inputs				Output
S_0	S_1	A	B	Y
L	L	X	L	L
L	L	X	H	H
L	H	X	L	L
L	H	X	H	H
H	L	L	X	H
H	L	H	X	L
H	H	X	X	H

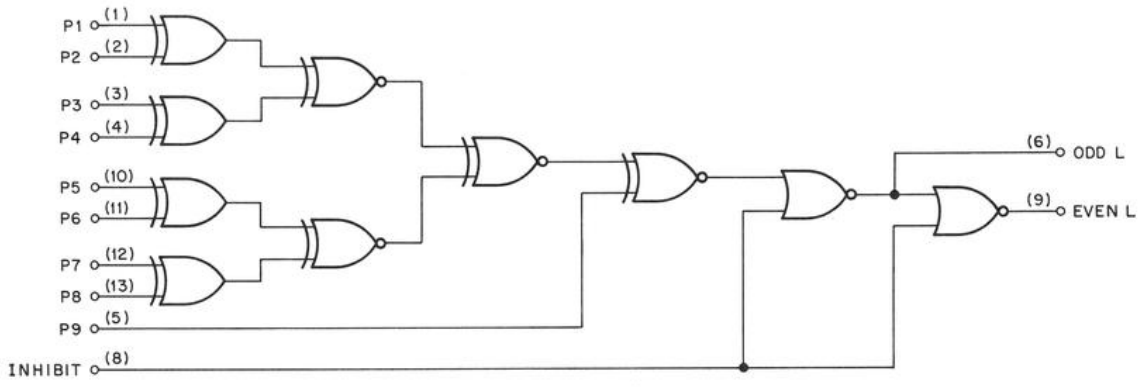


NOTES:
1. Numbers in parentheses denote pin numbers.
2. Pin 16 = V_{CC}
3. Pin 8 = GND

11-1757

B.6 TYPE 82S62 9-BIT PARITY GENERATOR AND CHECKER

This IC is a Schottky clamped, high speed parity tree used for both parity generation and checking. Two outputs are provided for either odd or even parity. An inhibit input is also provided, which disables both outputs; a high on the inhibit input causes both outputs to be forced low. The schematic diagram is shown below.



NOTES:
1. Pin 14 = V_{CC}
2. Pin 7 = GND

11-1758

MM11-S, MF11-L, and MF11-LP
CORE MEMORY SYSTEMS
EK-MM11S-TM-004

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