

WEEK 2 PDP11/40

TIME	MON	TUES	WED	THURS	FRI
0900	INTRO TO μ PROGRAM DEVICE	KD11 FLOWS	KD11 FLOWS & DISPLAY RULES	LOGIC ANALYSIS	LOGIC ANALYSIS
1000	SUB COMMANDS AND BLOCK DIAGRAM USAGE			POWER UP POWER DWN	DATA XFER BR SEQ
1100	↓	MICRO BRANCHING	KD11 CONSOLE OPERATIONS	STACK OVFW ODA ERROR	NPR SEQ
1200	L	U	N	C	H
1300	U WORD FORMAT & CLOCK CKT ANALYZE	KD11 FLOWS & SINGLE CLOCKING K11L	KD11 FLOWS SERVICE & TRAPS	PROBLEM ISOLATION & EACK PLANE	MM-11 MEMORY
1400	↓	↓	↓	↓	↓
1500	MUX ^s & GPR ADRS SWITCH	LAB	LAB	TROUBLE SHOOTING LAB	↓
1600	INTRO TO KD11 FLOWS	↓	↓	↓	↓
1700	↓	↓	↓	↓	REVIEW & COURSE CRITIQUE

CORRECTION SHEET

1- CHANGE DOPØ7 (SHEET 8) FLOWS FROM DISPLAY D TO DISPLAY R [SE]

2.- ADD THE TERM BUT Ø6 TO CON19 (SHEET 11) FLOWS

3 - REVISE MCDULE UTILIZATION KM11A BASIC = FL OPTION E1

4 - BA MAX LOW ORDER INPUTS ARE REVERSED

5 -

6 -

7 -

8 -

9 -

10 -

11 -

12 -

13 -

14 -

15 -

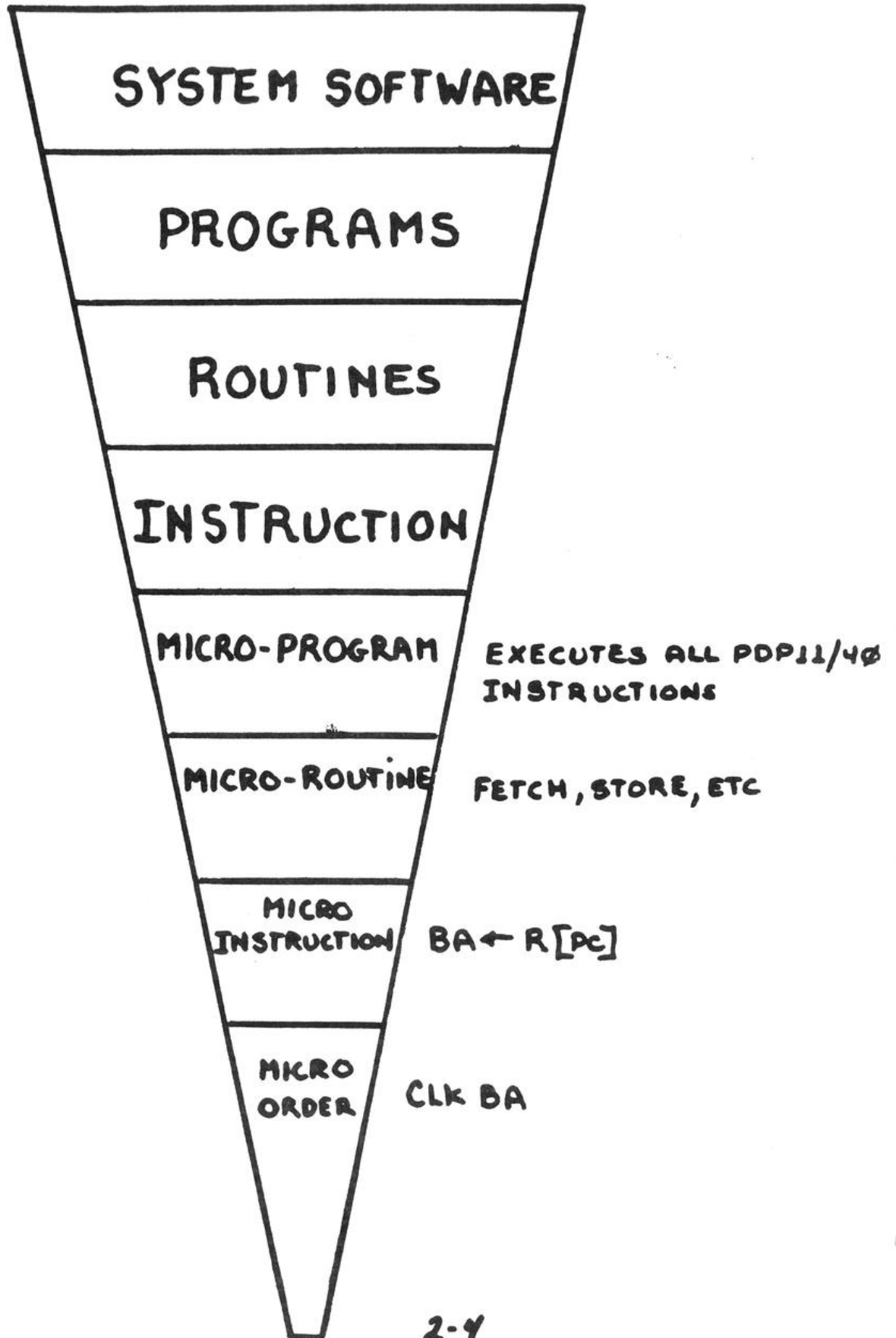
16 -

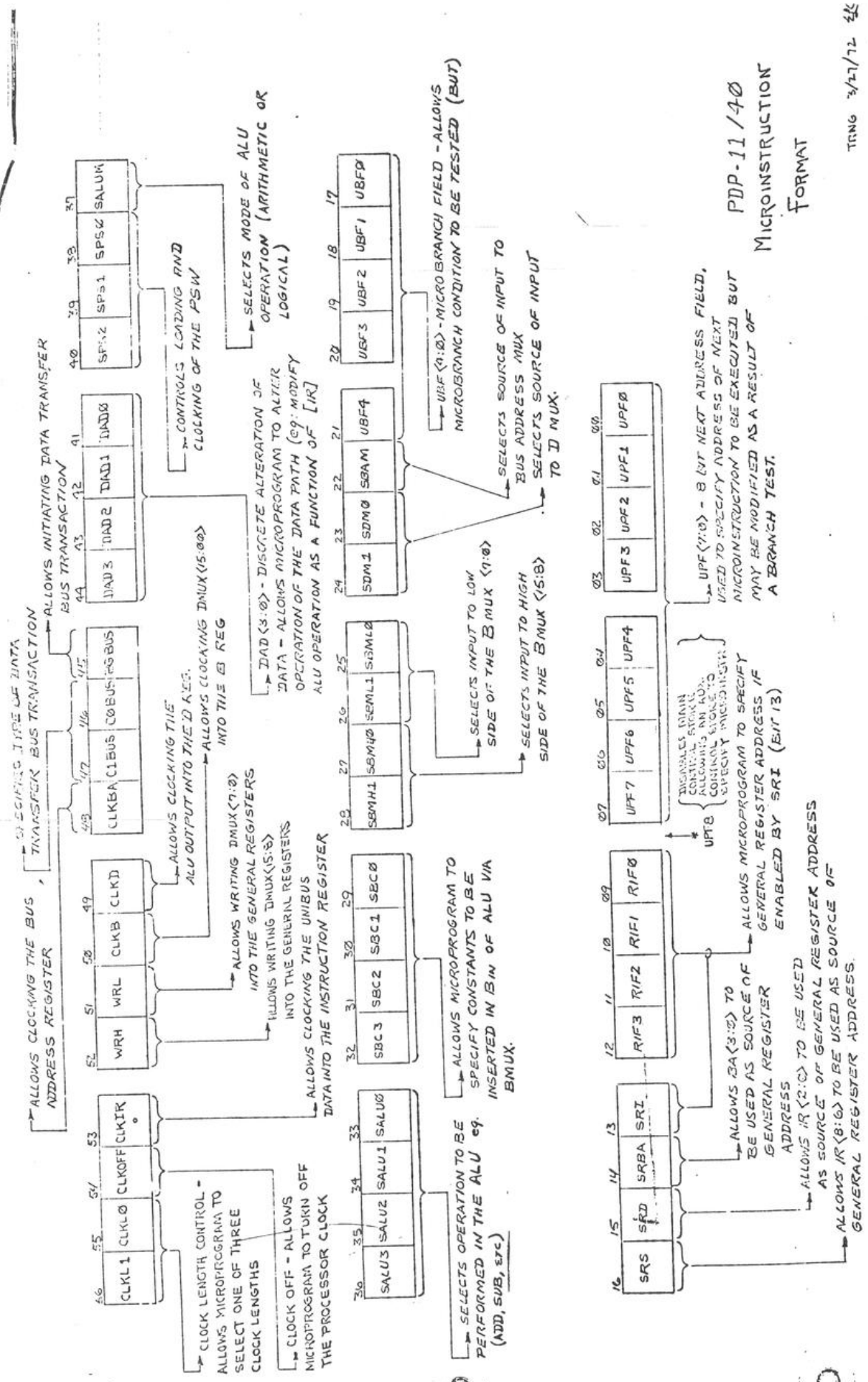
17 -

18 -

DAY I

MICRO-PROGRAM
INTRODUCTION.





PDP-11/40
MICROINSTRUCTION
FORMAT

TRNG 3/27/72 44

SUB-COMMAND EXAMPLES

USING THE KD-11 BLOCK DIAGRAM AND
THE SUB COMMAND LIST, WRITE THE SUB-COMMAND
SETS REQUIRED TO IMPLEMENT THE FOLLOWING

1. $BA \leftarrow \text{UNJ BUS DATA}$

2. $R[6] \leftarrow R[6] \text{ MINUS } 2$

ANSWER TO SUB-COMMAND EXAMPLES (2-8)

1. BA ← UNI-BUS DATA

"CLKL1"

DMUX <15:00> ← BUS D <15:00>

(P1)

B <15:00> ← DMUX <15:00>

CLKL2

BMUX <15:00> ← B <15:00>

BIN <15:00> ← BMUX <15:00>

A_{IN} = ∅

C_{IN} = ∅

ALUOUT = BIN + A_{IN} + C_{IN}

BAMUX <15:00> ← ALUOUT <15:00>

(P2)

BA <15:00> ← BAMUX <15:00>

2. R[6] ← R[6] MINUS 2

"CLKL3"

RIF <3:∅> ← 6

RA <3:∅> ← RIF <3:0>

READ ← 1

A_{IN} <15:00> ← R <15:00>

C_{IN} = ∅

B_{CON} <15:00> ← 2

BMUX <15:00> ← B_{CON} <15:00>

B_{IN} <15:00> ← BMUX <15:00>

ALUOUT = A_{IN} MINUS B

(P2)

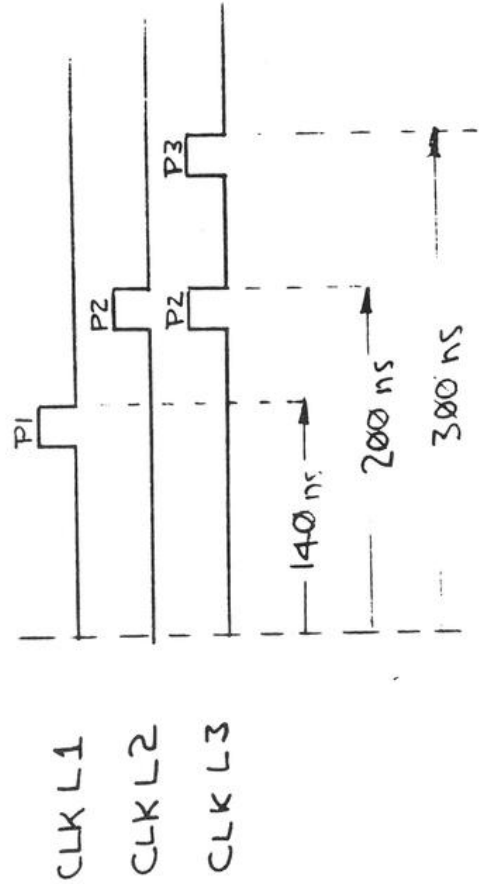
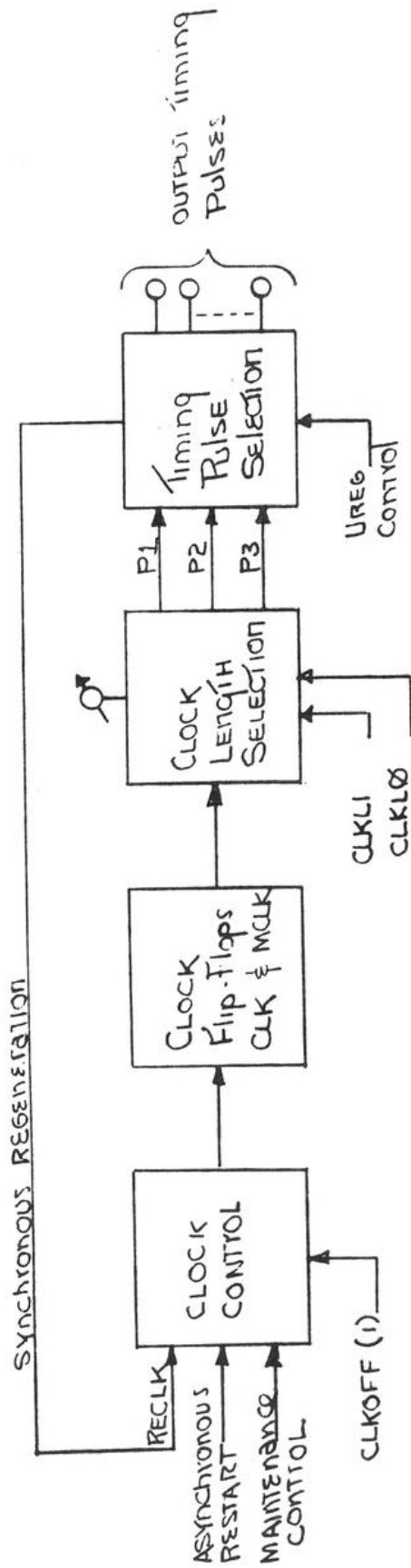
D <15:00> ← ALUOUT <15:00>

DMUX <15:00> ← D <15:00>

R <15:00> ← DMUX <15:00>

(P3)

WRITE ← 1



K111A
PROCESSOR CLOCK
Block Diagram

BASIC TIMING

PURPOSE:

USED TO GATE INFORMATION INTO REGISTERS AND TO STEP THE MICRO-PROGRAM THRU ITS SEQUENCES:

SELECTION OF CLOCK LENGTH:

THERE ARE THREE UNIQUE CLOCK LENGTHS THAT MAY BE SELECTED BY THE MICRO-PROGRAM. EACH MICRO-WORD WILL SELECT ONE OF THE FOLLOWING CLOCK LENGTHS DEPENDING ON WHAT THAT MICRO-WORD IS TRYING TO DO. THE MICRO-WORD WILL ALWAYS SELECT THE SHORTEST CLOCK LENGTH THAT WILL ACCOMPLISH THE TASK SPECIFIED IN THAT MICRO-WORD.

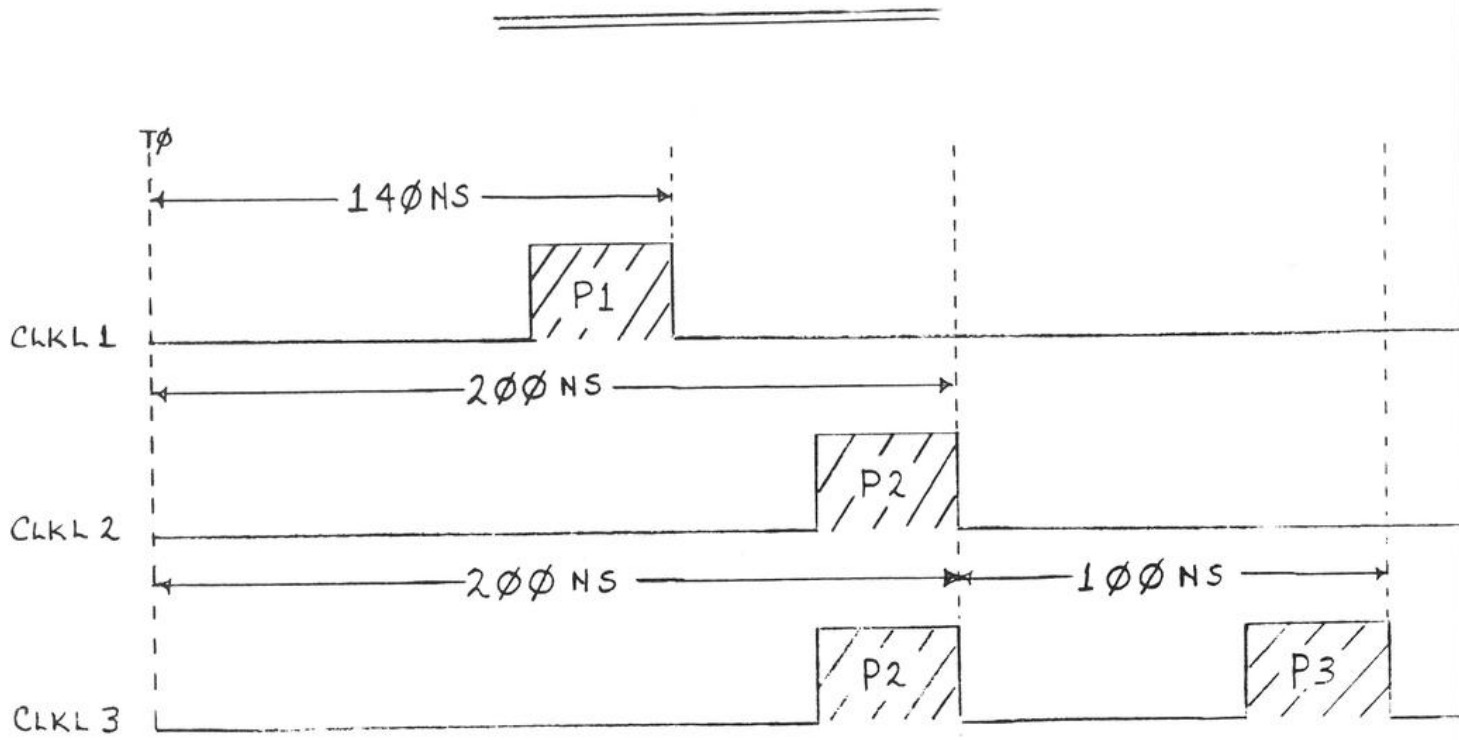
RECYCLING THE CLOCK:

THE CLOCK WILL AUTO-MATICALLY RESTART ITSELF ON THE TRAILING EDGE OF THE LAST CLOCK PULSE PERMITTED IN THE PRECEDING CLOCK CYCLE. RESTART IS ASSUMED UNLESS THE MICRO-WORD CHOOSES TO STOP THE CLOCK (IE DATA BUS CYCLE)

GENERAL RULES FOR CHOOSING CLOCK LENGTHS:

SINCE THE MICRO-PROGRAM CAN BE STEPPED ALONG BY THE PRESENCE OF ANY OF THE THREE CLOCK LENGTHS, THE ONLY FACTOR IN SELECTING CLOCK LENGTHS IS WHICH REGISTER IS INVOLVED IN THIS MICRO-WORD EXECUTION. CERTAIN REGISTERS REQUIRE PARTICULAR CLOCK LENGTHS TO BECOME ACTIVE. THE FOLLOWING IS THE REQUIRED CLOCK LENGTH THAT WILL ACTIVATE THE REGISTERS.

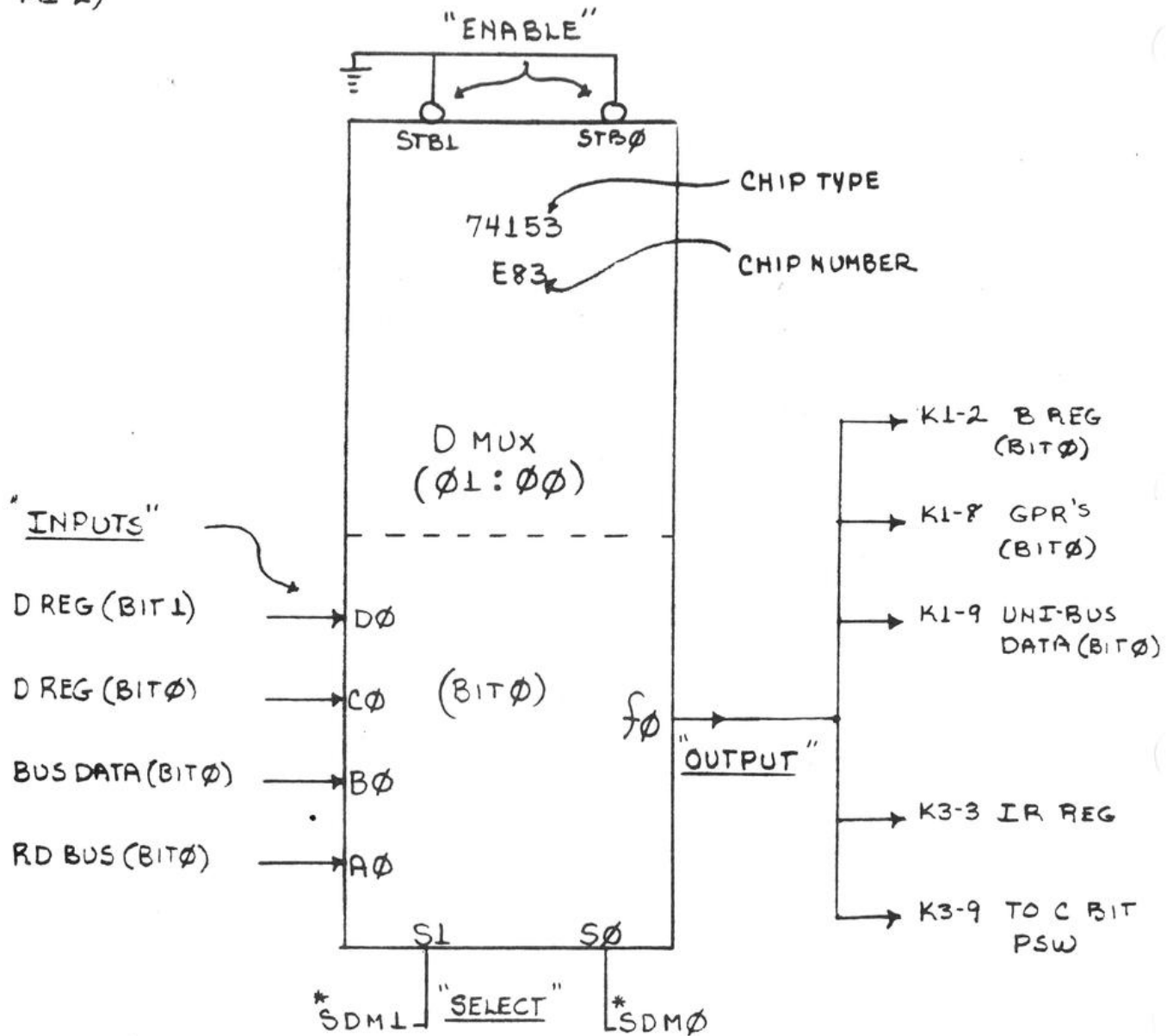
LOADING BA REG	CLKL 1 OR CLKL 2
LOADING D REG	CLKL 2
LOADING GPR REG	CLKL 1 OR CLKL 3
LOADING IREG AND BREG	CLKL 1 OR CLKL 3



NOTE: WHENEVER CLKL3 IS SPECIFIED BY MICRO-WORD P2 AND P3 ARE BOTH AVAILABLE AT CLOCK OUTPUT.

D MULTIPLEXOR

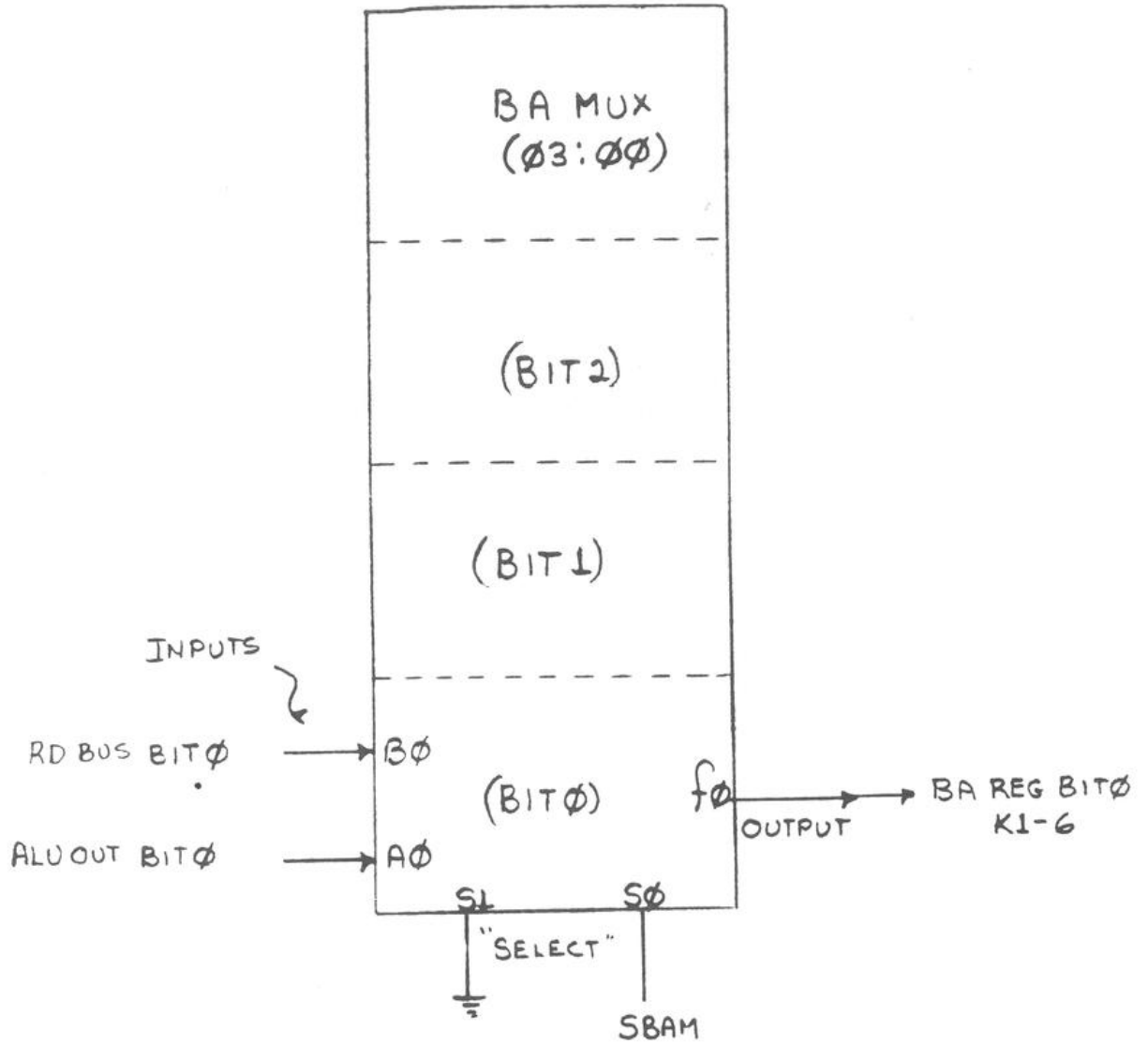
(SHEET K1-2)



S1	S \emptyset	OUTPUT
\emptyset	\emptyset	RD BUS BIT \emptyset
\emptyset	1	BUS DATA BIT \emptyset
1	\emptyset	D REG BIT \emptyset
1	1	D REG BIT 1

* SDM1/SDM \emptyset = SELECT D MUX BITS FROM MICRO-WORD

BA MULTIPLEXOR (SHEET KI-2)

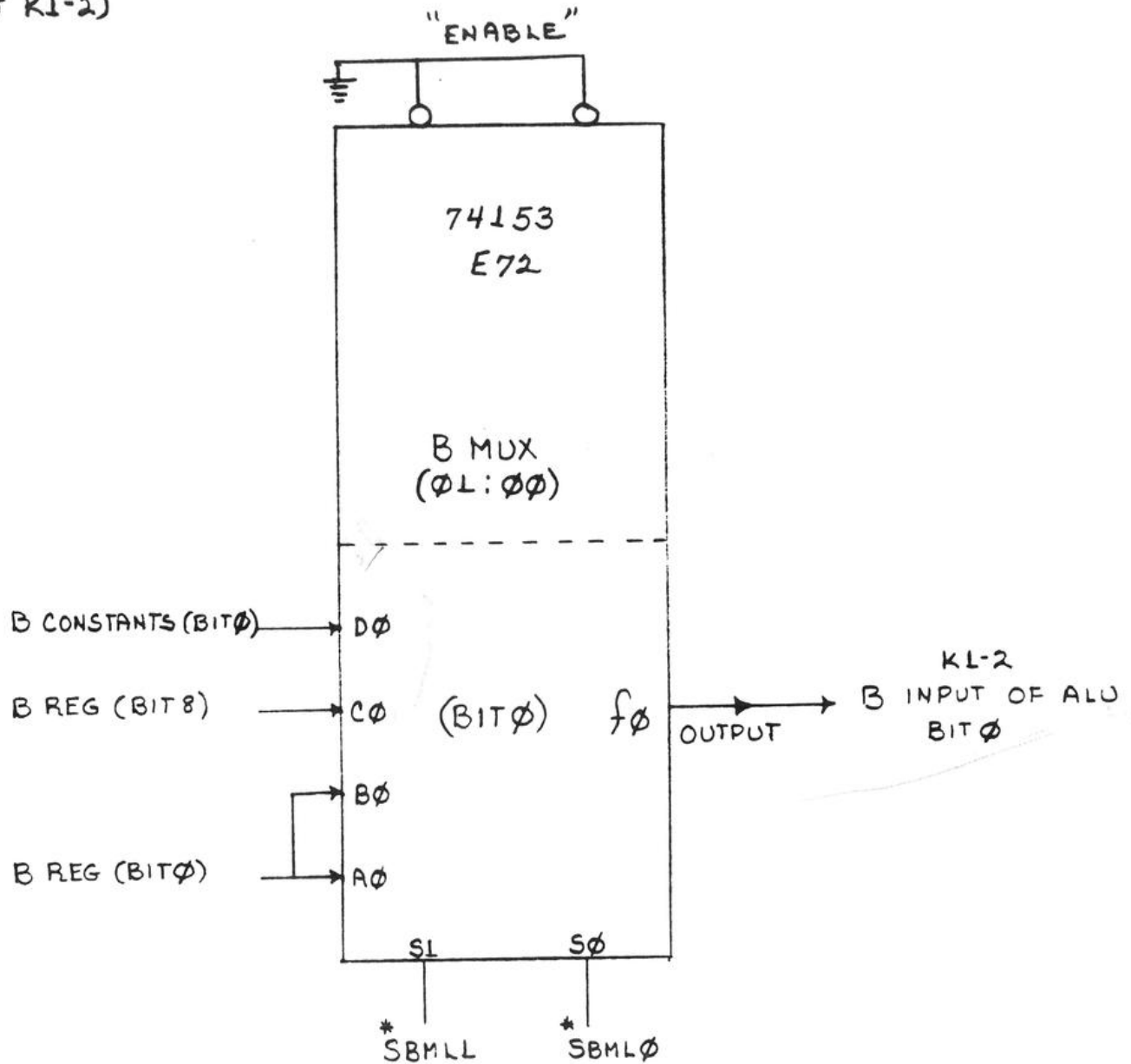


SBAM	OUTPUT
0	ALU OUT
1	RD BUS

NOTE: THIS MULTIPLEXOR
HAS NO ENABLE

B MULTIPLEXOR

(SHEET K1-2)

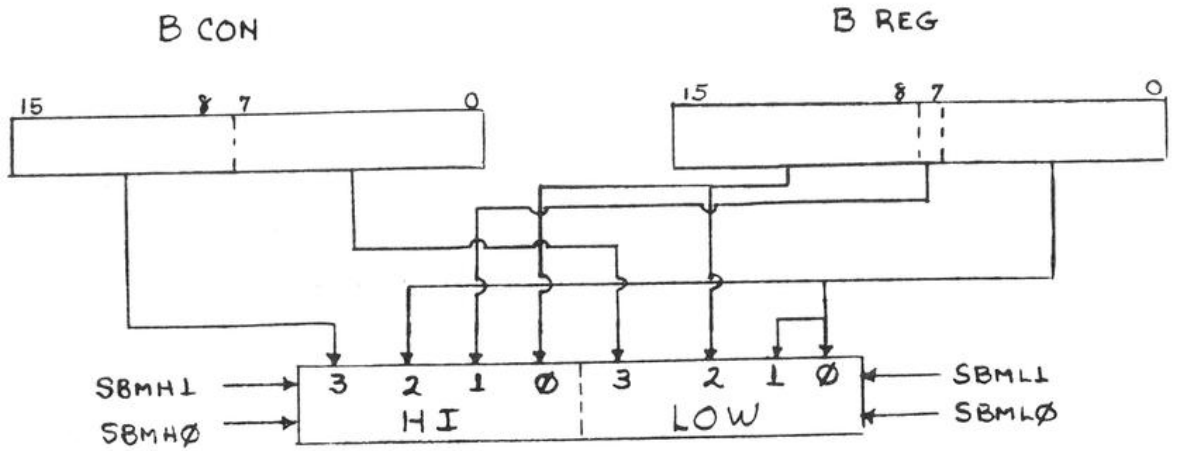


$S1$	$S\phi$	OUTPUT
ϕ	ϕ	B REG BIT ϕ
ϕ	1	B REG BIT ϕ
1	ϕ	B REG BIT 8
1	1	B CONSTANT BIT ϕ

* SBMLL/SBML ϕ : SELECT B MUX LO BYTE FROM MICRO-WORD

SBMH1/SBMH ϕ ARE USED TO CONTROL INPUTS TO B MUX BITS 8 → 15 SEE SHEET K1-4

B MUX



	SBMHI	SBMH0	SBMLI	SBML0	
SBM 00	0	0	0	0	= B REG TO ALU
SBM 02	0	0	1	0	= DUPLICATE UPPER BYTE
SBM 05	0	1	0	1	= SIGN EXTEND
SBM 10	1	0	0	0	= DUPLICATE LOW BYTE
SBM 12	1	0	1	0	= SWAP BYTES
SBM 17	1	1	1	1	= B CON TO ALU

4. ROM LOCATION $\Phi\Phi6$ SPECIFIES THAT THE _____ REGISTER SHALL BE DISPLAYED IN THE DATA LIGHTS OF THE CONSOLE. (REFER TO UNWORD TABLES)

- A- IR REGISTER
- B- D REGISTER
- C- GPR R-14
- D- GPR R-13

5. WHICH OF THE BELOW ROM LOCATIONS SPECIFIES CLOCK LENGTH 3, DATA, CLOCK OFF

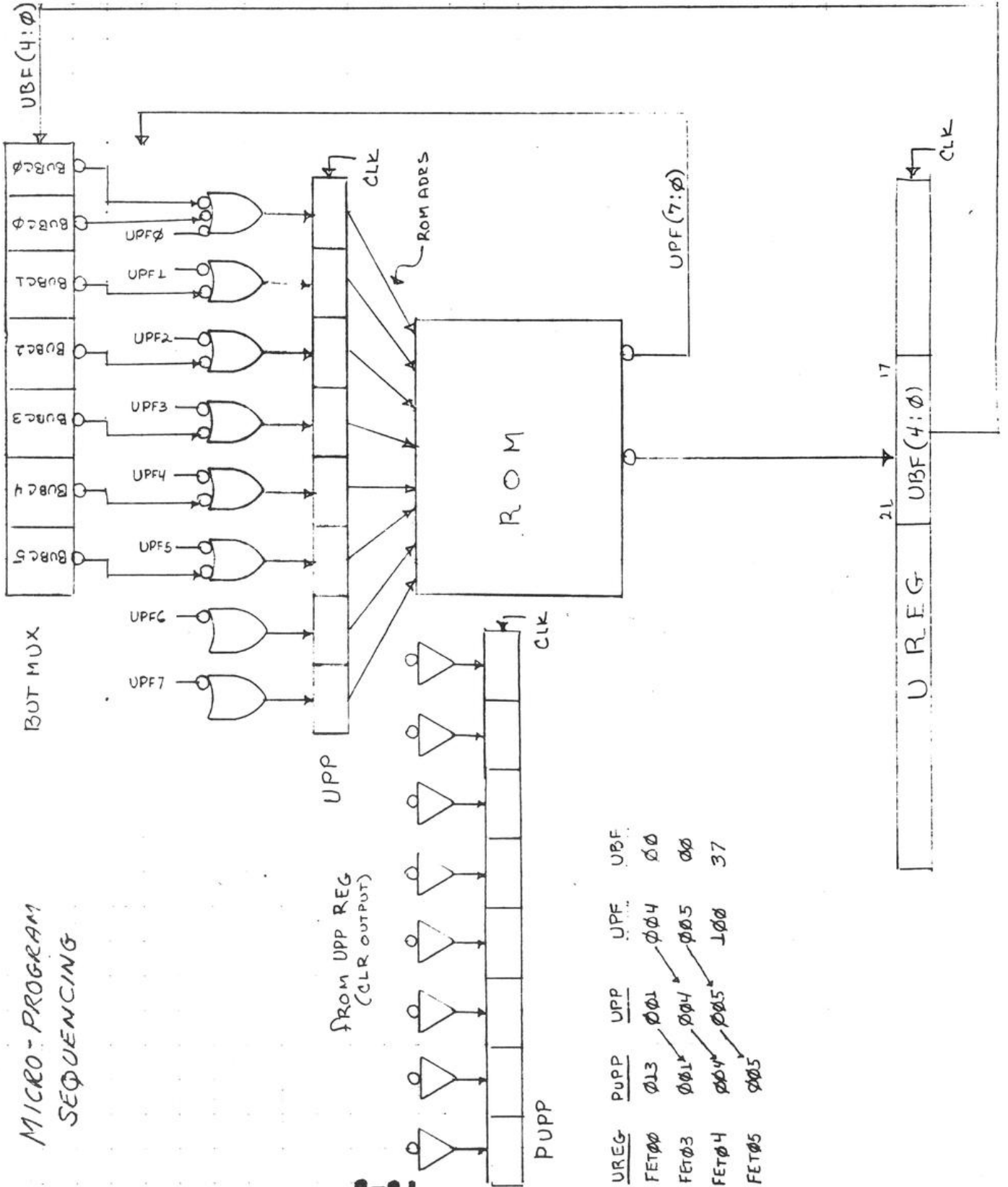
- A. $3\Phi6$
- B. 15Φ
- C. $\Phi4\Phi$
- D. $1\Phi1$

6. REFER TO OUTPUT OF THE CLOCK ON K4-2. THE SIGNAL PART P END H IS ACTIVE ON

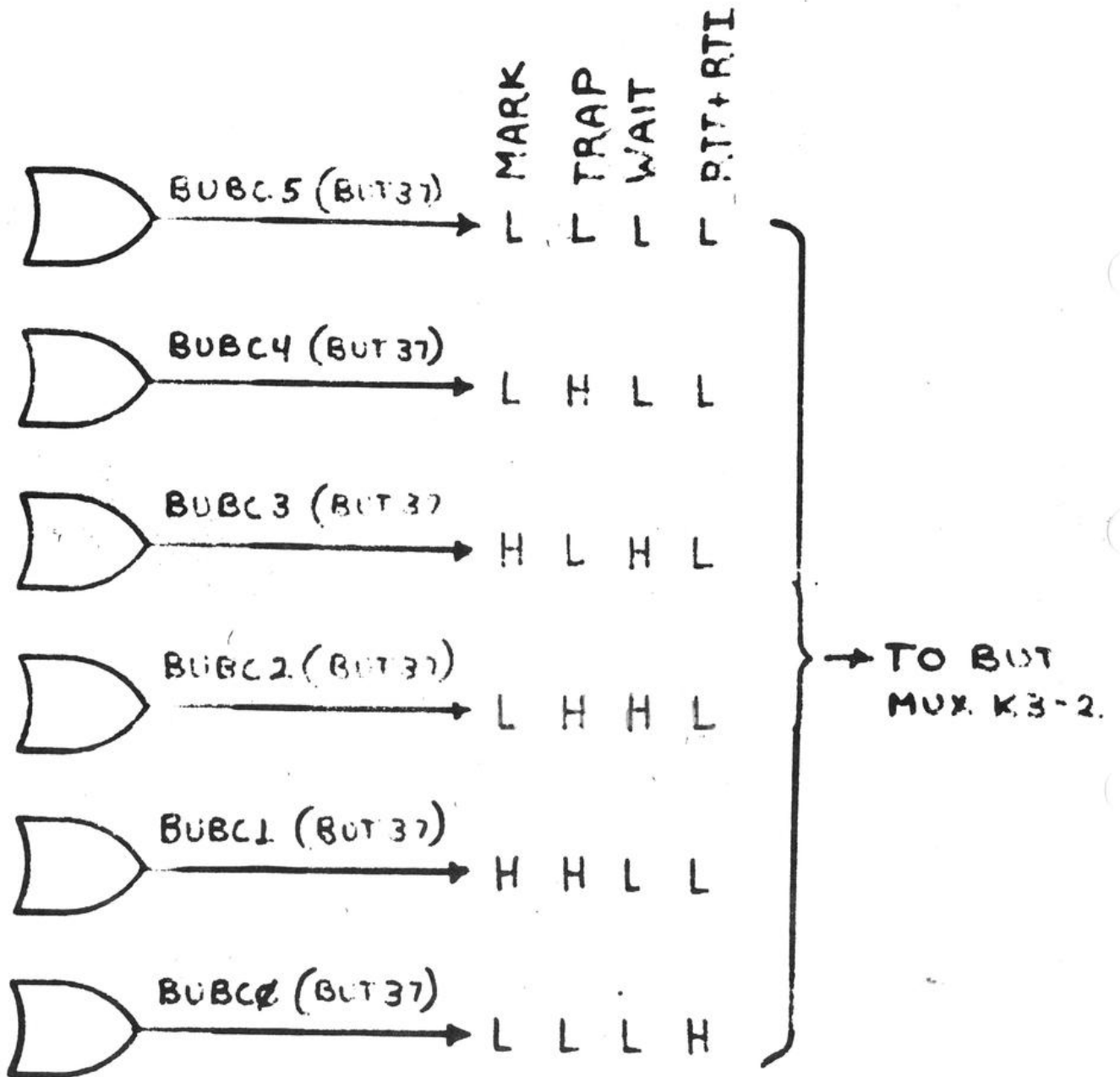
- A. $P1+P2+P3$
- B. $P1+P3$
- C. $P2+P3$
- D. $P1+P2$

DAY 2

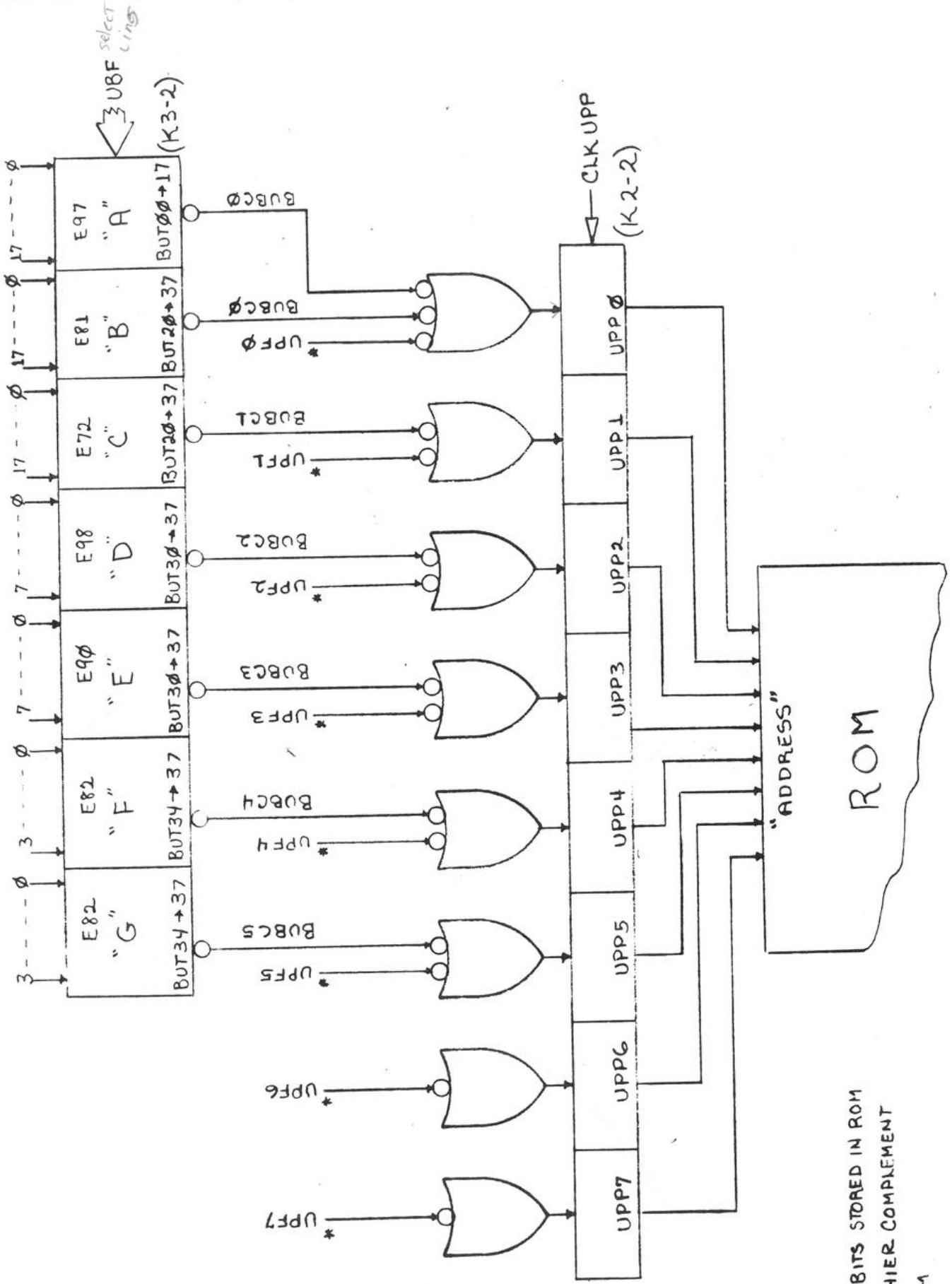
MICRO-PROGRAM SEQUENCING



OUT PUT OF IR
 DECODE TO CONTROL
 BUT MUX [K3-5]



MICRO-BRANCHING

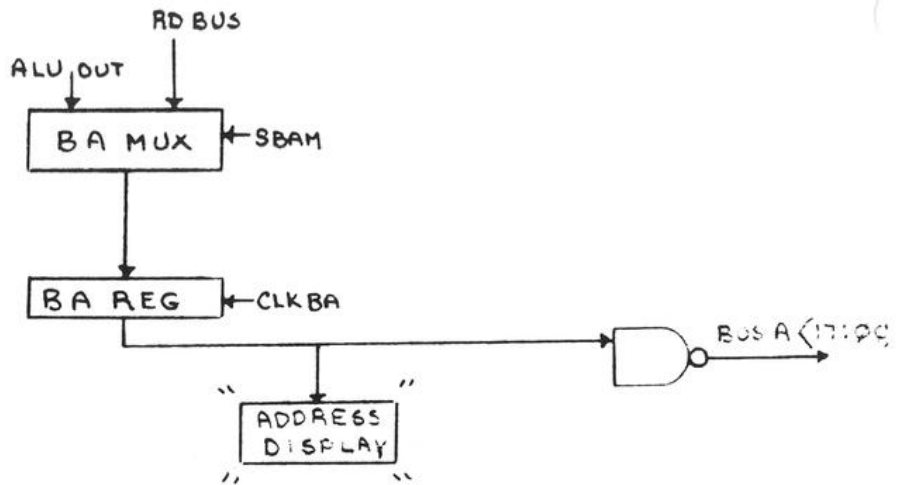


* NOTE:
UPF BITS STORED IN ROM
IN THEIR COMPLEMENT
FORM

DAY 3

SINGLE CLOCK DISPLAY RULES

ADDRESS DISPLAY

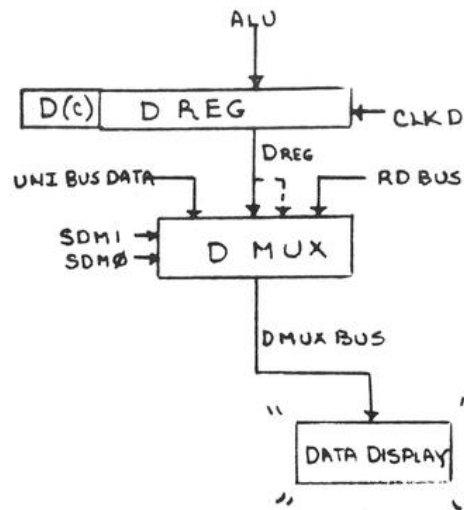


SINCE ADDRESS DISPLAY LIGHTS ARE FED DIRECTLY BY CONTENTS OF BA REG YOU NEED ONLY DETERMINE THE CONTENTS OF BA REG.

RULE:

IF MICRO-WORD SPECIFIES $BA \leftarrow X$, YOU WILL NOT SEE X IN BA NOR WILL X BE DISPLAYED IN THE ADDRESS LIGHTS UNTIL THE NEXT CLOCK PULSE. THE ADDRESS LIGHTS WILL DISPLAY THE CONTENTS OF BA REG ESTABLISHED IN THE LAST MICRO-WORD THAT ALTERED THE CONTENTS OF BA REG.

DATA DISPLAY



THE DATA DISPLAY LIGHTS ARE DRIVEN BY THE OUTPUT OF THE D MUX. SINCE THE D MUX CAN BE SELECTED TO OUTPUT FROM ONE OF FOUR INPUTS, THE MICRO-WORD FLOWS WILL INDICATE WHICH INPUT LINE IS BEING DISPLAYED. THE DATA DISPLAY SOURCE IS INDICATED IN THE SMALL BOX, UPPER RIGHT OF EACH MICRO-WORD OF THE FLOWS.

RULES:

IF THE DATA DISPLAY INDICATOR, IN THE MICRO-WORD, SPECIFIES UNI-BUS DATA OR ANY OF THE 16 GPRS, THAT DATA WILL BE DISPLAYED IN THAT MICRO-WORD.

IF THE DATA DISPLAY INDICATOR, IN THE MICRO-WORD, SPECIFIES DISPLAY D AND THAT MICRO-WORD ALSO SPECIFIES $D \leftarrow X$, X WILL NOT BE SEEN IN D NOR WILL IT BE DISPLAYED UNTIL THE NEXT CLOCK PULSE. THE DATA LIGHTS WILL DISPLAY THE VALUE IN D ESTABLISHED IN THE LAST MICRO-WORD THAT ALTERED THE CONTENTS OF D.

KM-11 DISPLAY

IF THE MICRO-WORD SPECIFIES DATI OR DATO, MSYN LIGHT ON THE KM11 MAINTENENCE MODULE WILL NOT LIGHT UNTIL NEXT CLOCK PULSE. YOU WILL NOTE THAT SSYN ON MAINTENENCE MODULE SHOULD ALSO BE LIGHTED WHEN MSYN IS ON.

BUBC1 & BUBCØ
TRANSLATOR (K3-7)

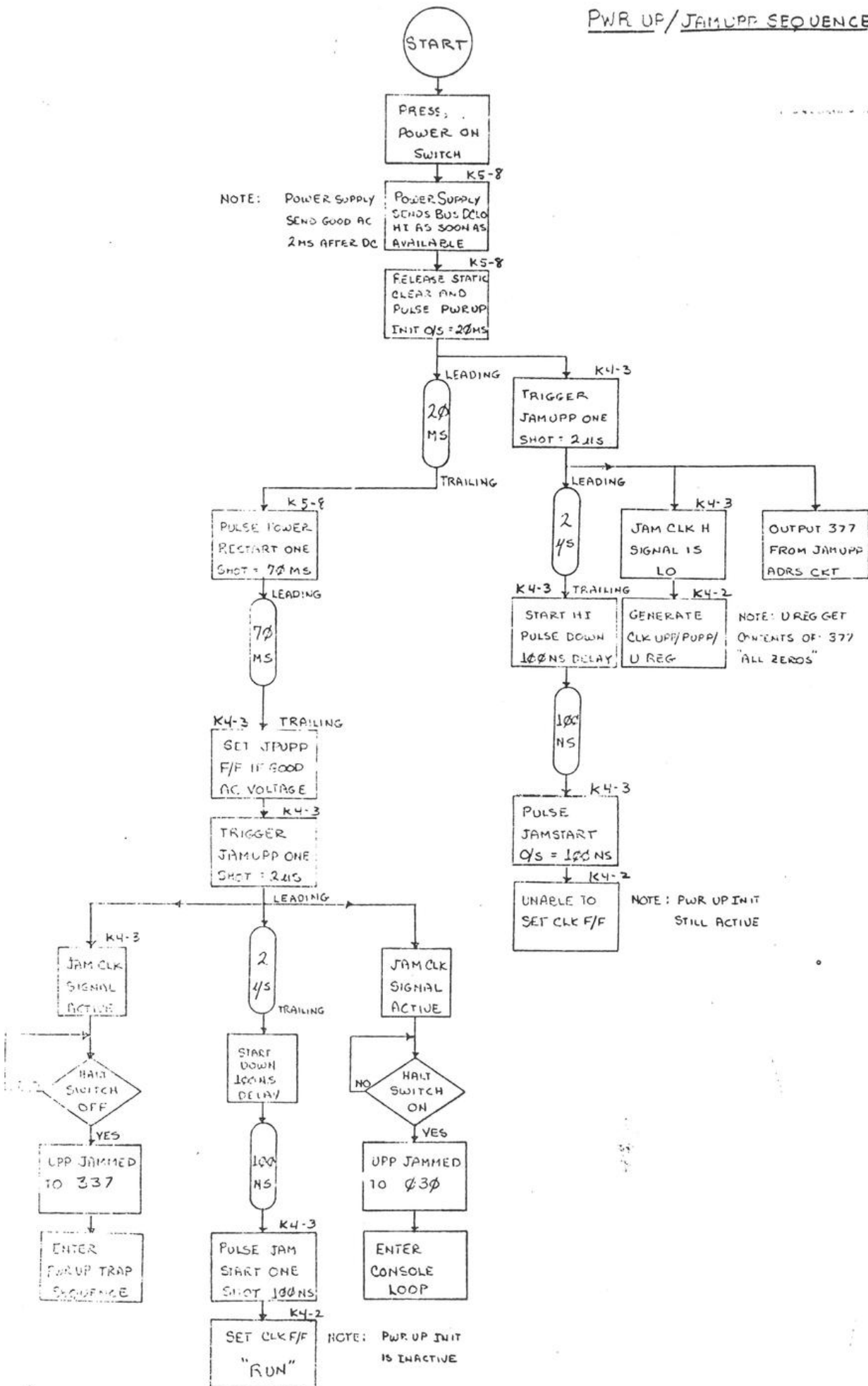
(FOR USE IN SERVICE FLOW)

CONDITION	BUBC1 (BUT26)	BUBCØ (BUT26)	BASE ADDR	BRANCH ADDR
BERR PS(T) OVFLW PWRDWN	Lo	Lo	Ø1Ø	Ø1Ø TRAP A
CBR	Lo	Hi	Ø1Ø	Ø11 CONSOLE B
BR+WAIT	Hi	Lo	Ø1Ø	Ø12 SERØ6
No RøST	Hi	Hi	Ø1Ø	Ø13 FETCH A

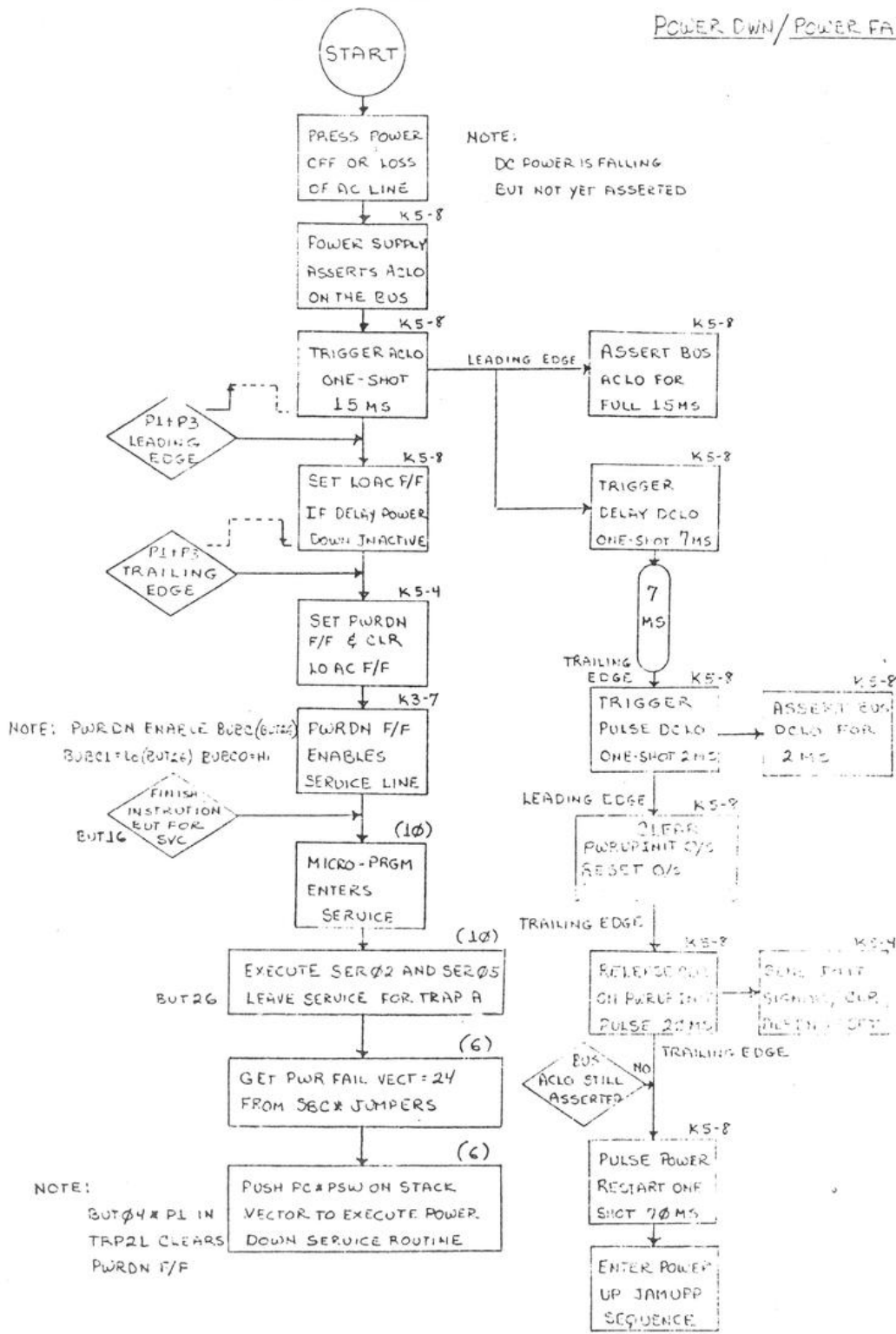
CONDITION	BUBC1 (BUT25)	BUBCØ (BUT25)	BASE ADDR	BRANCH ADDR
BR	Lo	Lo	Ø14	Ø14 SERØ9
WAIT	Hi	Hi	Ø14	Ø17 SERVICE C
No RøST	Hi	Lo	Ø14	Ø16 FETCH C

DAY 4

PWR UP/JAMUPP SEQUENCE

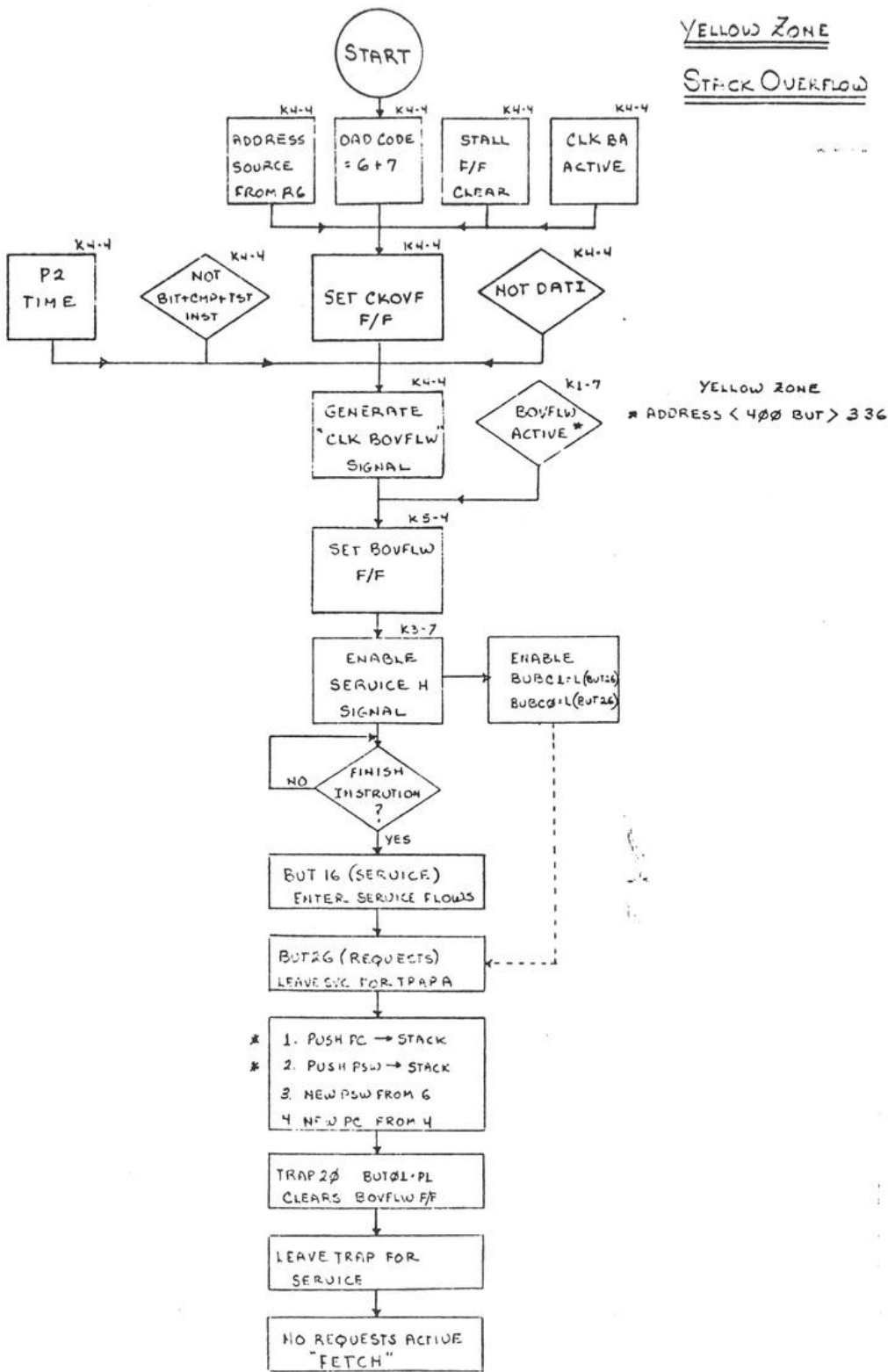


POWER DWN/POWER FAIL



YELLOW ZONE

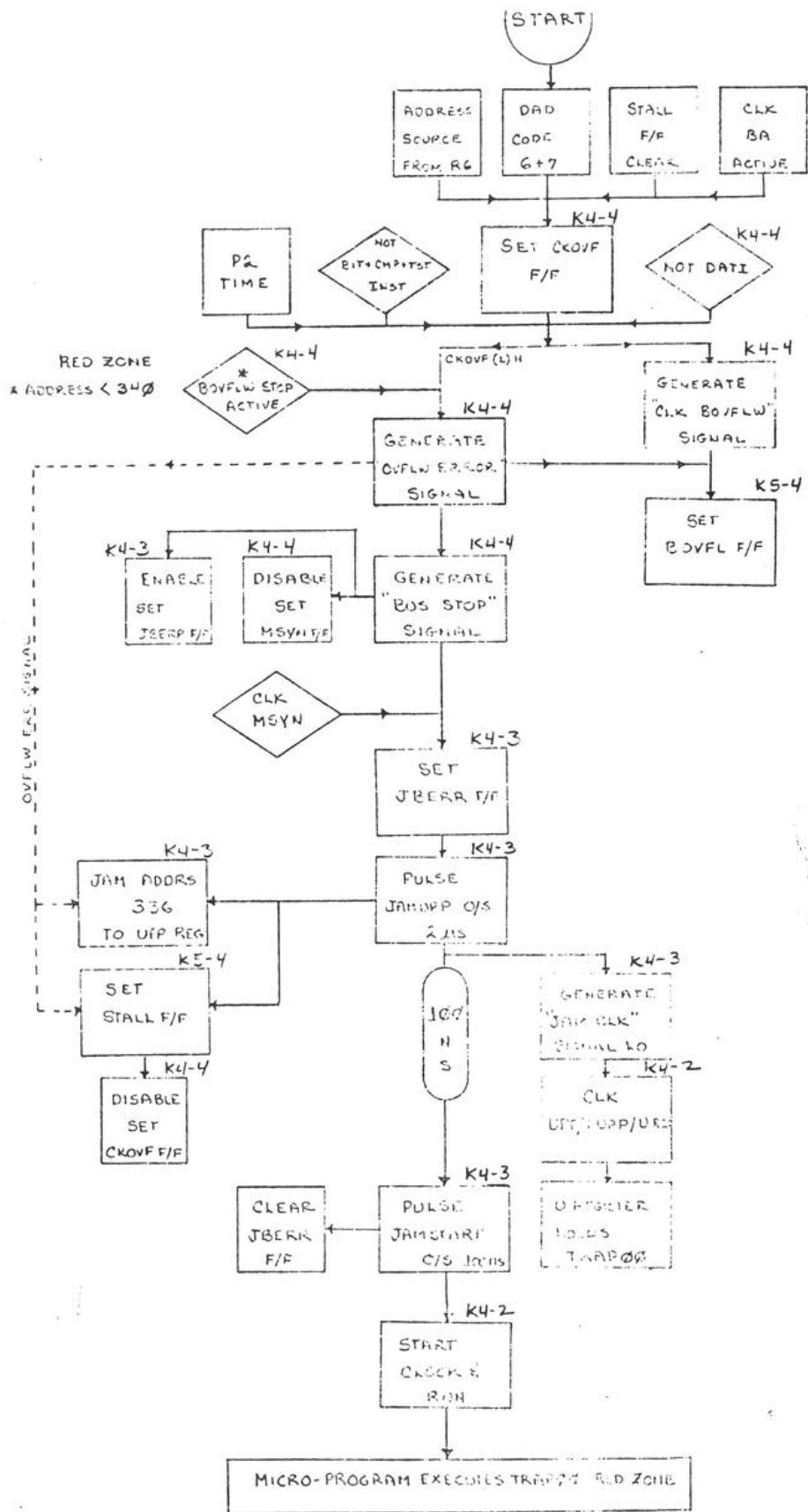
STACK OVERFLOW



* NOTE

TWO ADDITIONAL PUSHES ON THE STACK ARE DONE IN THE YELLOW ZONE TRAP ROUTINE AND ARE SENSED BY CKOVF F/F BUT DO NOT MATTER UNLESS A RED ZONE VIOLATION OCCURS DURING YELLOW ZONE PUSH

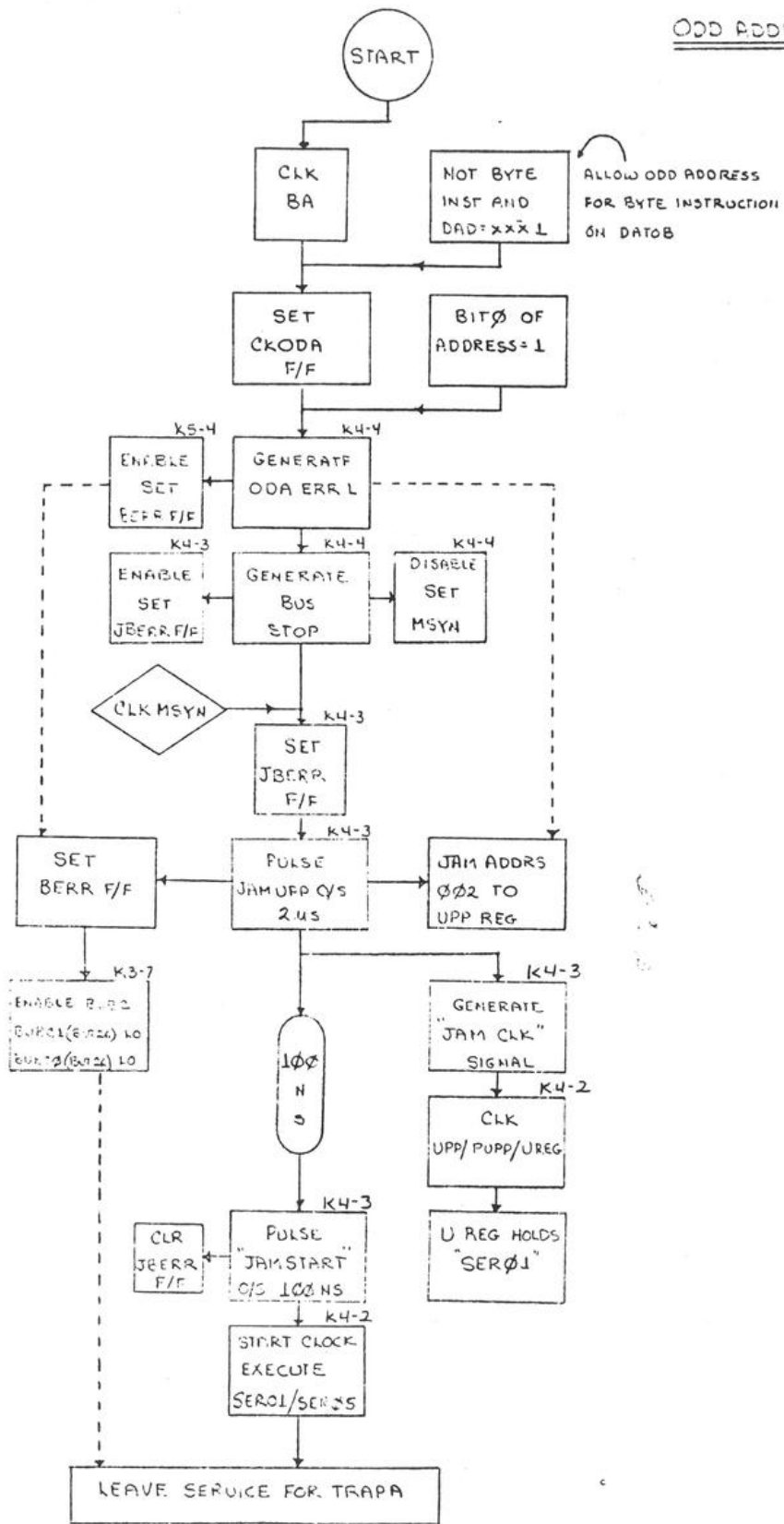
STACK OVERFLOW



NOTE:

- CLKBA IN TRP02 CLEARS CKOVF F/F (STAYS CLEAR AS LONG AS STALL F/F SET)
- BUT01XPL IN TRP20 CLEARS BOVFL F/F
- BUT04#P1 IN TRP21 CLEARS STALL F/F (ENABLE SENSING OUTFLOW)

ODD ADDRESS ERROR



NOTE

BERR F/F IS CLEARED BY BUT 03 PI IN TRPI6
 IF ANOTHER ODA OCCURS UP TO THIS POINT
 YOU HAVE A DOUBLE BUS ERROR (DUBBER)

PDP11/40 QUIZ
TROUBLE ISOLATION

ANALYZE THE PROBLEM SYMPTOMS GIVEN BELOW AND IN EACH CASE, GIVE AT LEAST ONE IC (MODULE NUMBER, CHIP NUMBER AND PIN NUMBER) THAT COULD CAUSE THE PROBLEM.

1. THE CLOCK IS DISABLED FROM THE MAINTENANCE BOARD (KMLL), YOU POWER UP THE PROCESSOR WITH THE HALT/ENABLE SWITCH IN THE HALT POSITION. UPP IS JAMMED TO ROM LOCATION 337 INSTEAD OF 30.

2. YOU ARE USING MAINT. MODULE TO SINGLE CLOCK THE CONSOLE FUNCTIONS. NO MATTER WHICH SWITCH YOU DEPRESS, YOU DISCOVER THAT ROM ALWAYS STAYS IN THE CONSOLE LOOP (26 → 46 → 26 → 46) ROM WILL NOT GO TO LOCATION 27 WHEN YOU DEPRESS A CONSOLE CONTROL SWITCH.

~~E28 P10~~
K3-2 K2-2
K5-6 E9P10

3. YOU ARE SINGLE CLOCKING THE PROCESSOR TO CHECK OUT THE LOAD ADDRESS SEQUENCE. THE SEQUENCE IS NORMAL UNTIL PUPP GOES TO 051, HERE YOU NOTE THE CONSOLE ADDRESS LIGHTS INDICATE A 17.

u. Reg 610 30

K2-6 E28 P10
Jammed high

TROUBLE ISOLATION
[CONT]

4. WHEN SINGLE CLOCKING THE PROCESSOR THRU A HALT INSTRUCTION, YOU HAVE NORMAL INDICATIONS UNTIL PUPP = 005, HERE YOU NOTE THAT UPP GOES TO 114 INSTEAD OF 122, WHICH IS THE REQUIRED SEQUENCE FOR A HALT.

K3-9 ⁹¹⁰ ~~114~~ ~~122~~
114

W015 = 00001

FOR QUESTIONS 5-9 ASSUME THAT YOU ARE SINGLE CLOCKING THE SUBTRACT INSTRUCTION SHOWN BELOW:

500- SUB #20, @ (3)+
502- 20
504- HALT

R3 = 3000
3000 = 5000
5000 = 40

5. IN THE VERY FIRST STEP OF FETCH [FET02, LOC 16] WE NOTE THAT THE CONSOLE ADDRESS LIGHTS INDICATE A 3000 INSTEAD OF 500. Bit 2 ~~high~~ _{low}

6. NORMAL INDICATION ON THE FIRST THREE ROM STATES BUT WHEN WE CLOCK IN FET05, WE NOTE THE CONSOLE DATA LIGHTS INDICATE A 503

7. NORMAL INDICATIONS UNTIL WE CLOCK IN SRC15 LOC 250. HERE WE NOTE THAT UPP GOES TO 137 INSTEAD OF 162.

K37 176 P6

TROUBLE ISOLATION
[CONT]

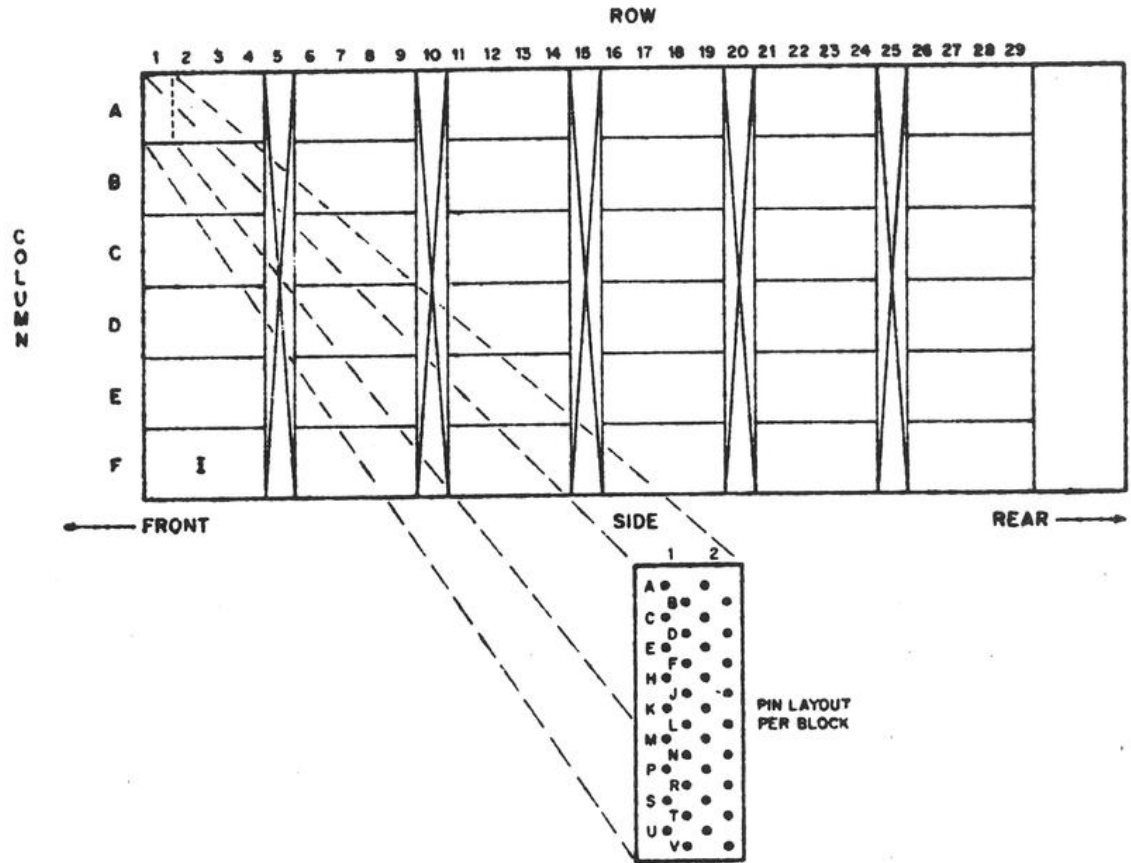
8. NORMAL INDICATIONS UNTIL WE CLOCK IN DOP12 LOCATION 367. HERE WE NOTE THE CONSOLE DATA LIGHTS INDICATE A 17

9. IN THE LAST MICRO-WORD DOP20, LOC 375 WE NOTE THAT THE "C" BIT INDICATOR ON THE MAINT MODULE IS LIGHTED.

TROUBLE ISOLATION

1. JAMUPP PROBLEM
2. BUT PROBLEM
3. SBC PROBLEM
4. IR DECODE PROBLEM
5. GPR ADDRESS SWITCH
6. INSERTED CARRY ON PC UPDATE
7. GETTING FALSE ODD BYTE SIGNAL
8. GETTING ONE'S COMPLEMENT INSTEAD OF TWO'S COMP
9. PSW "C" SHOULD SET IF OVFLW ON SUBTRACT

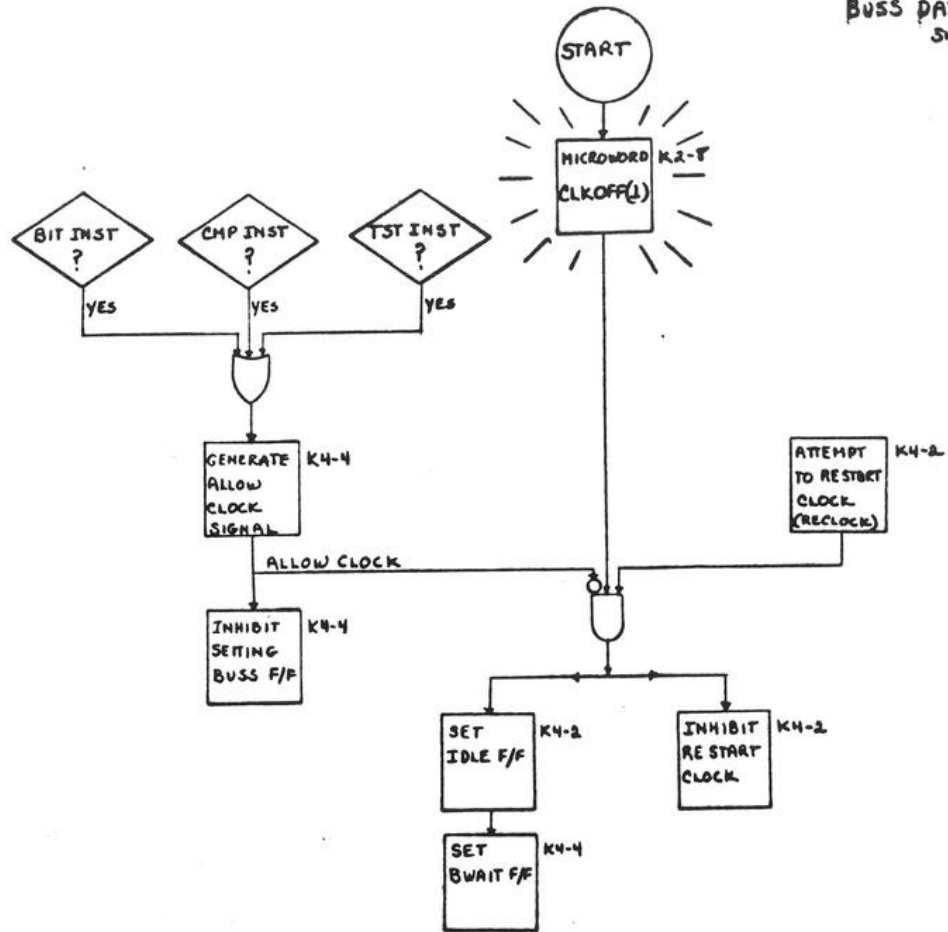
PDP-11 MODULE BLOCK AND PIN LAYOUT



PIN SIDE VIEW

DAY 5

2-42

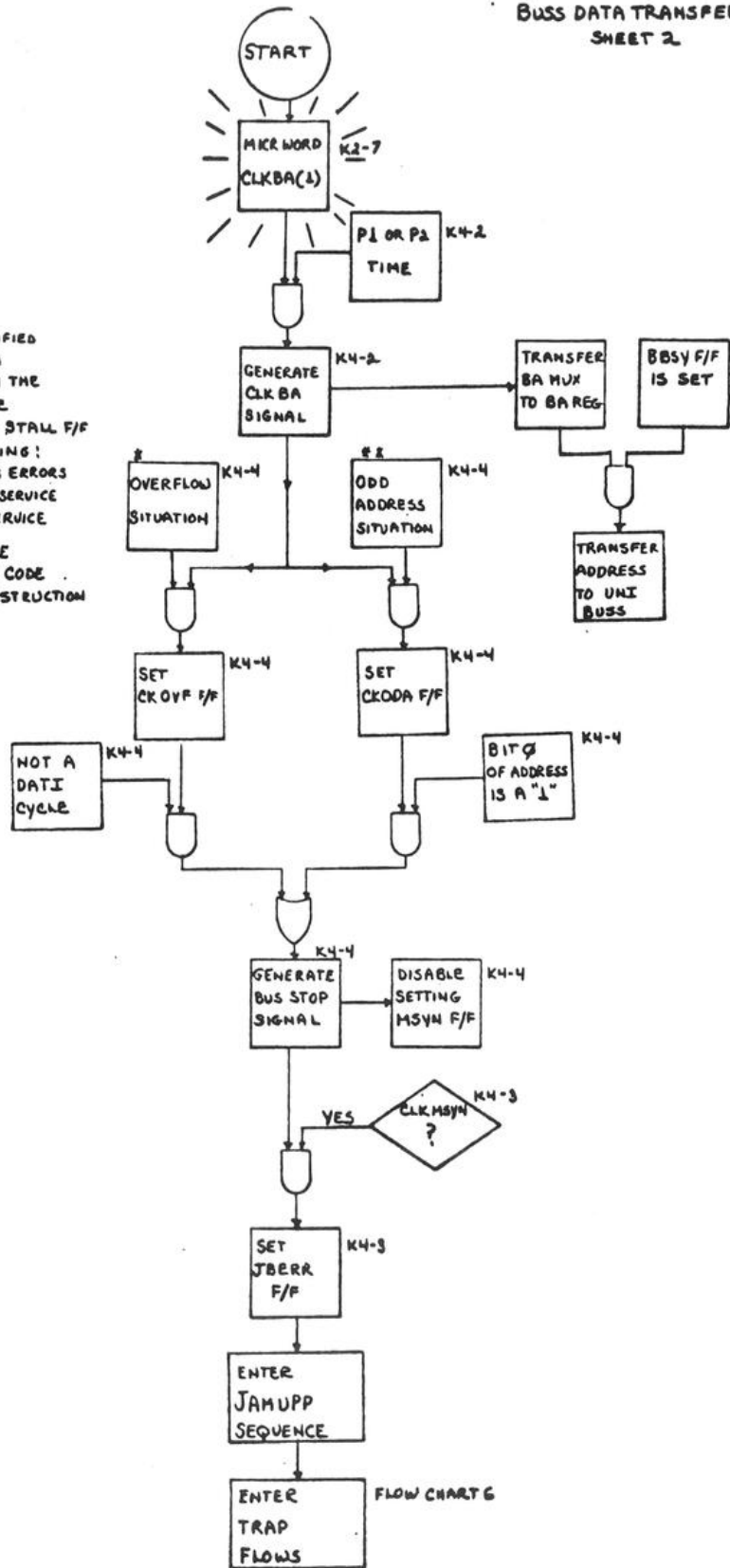


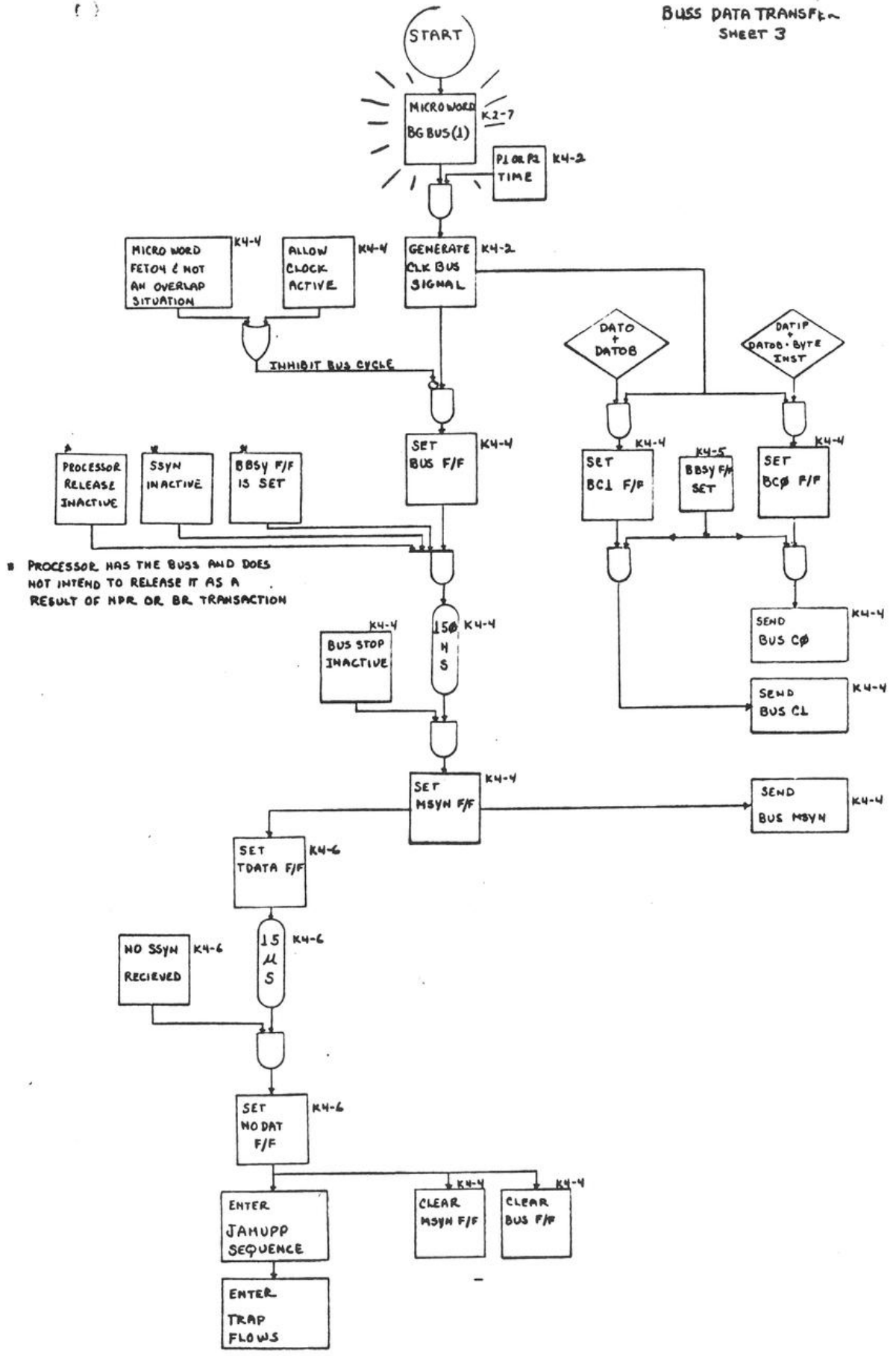
2-43

* OVERFLOW SITUATIONS ARE SPECIFIED BY U WORD DAD CODE AND A REGISTER ADDRESS OF R6 ON THE UNI-BUS. OVERFLOW CAN BE INHIBITED BY SETTING THE STALL F/F DURING ONE OF THE FOLLOWING:

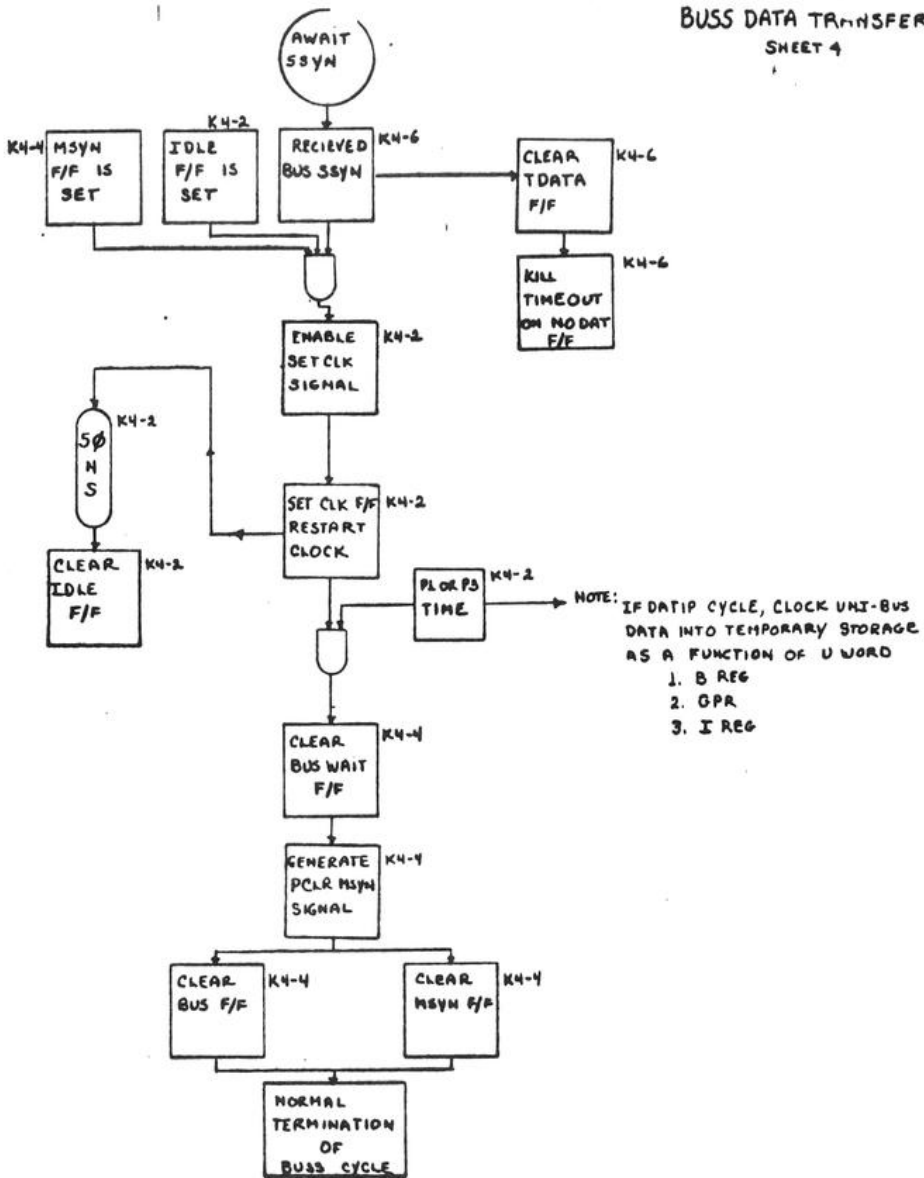
1. DOUBLE BUSS ERRORS
2. POWER DOWN SERVICE
3. OVERFLOW SERVICE

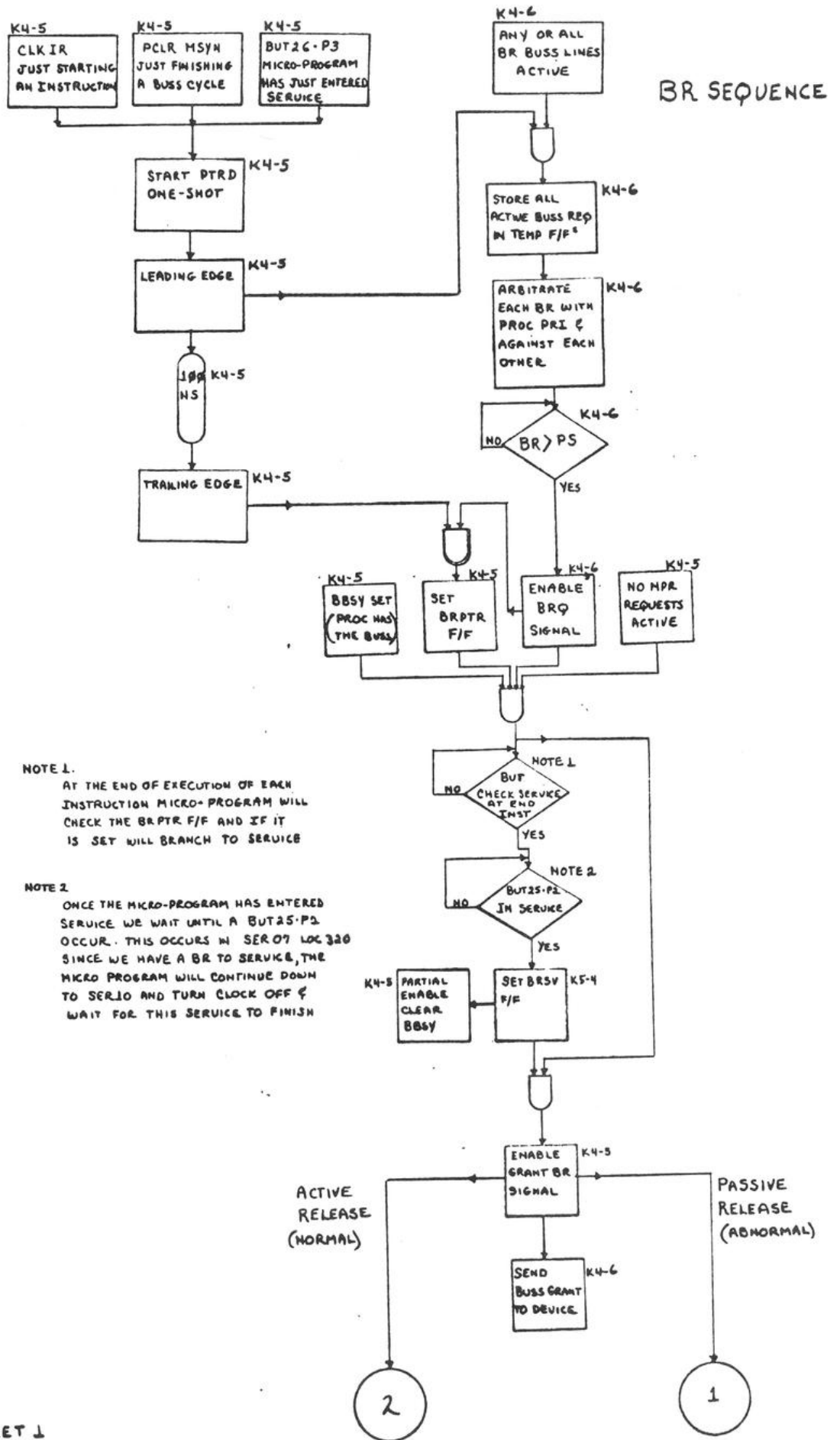
** ODD ADDRESS SITUATIONS ARE SPECIFIED BY U WORD DAD CODE AND IR DECODE = BYTE INSTRUCTION





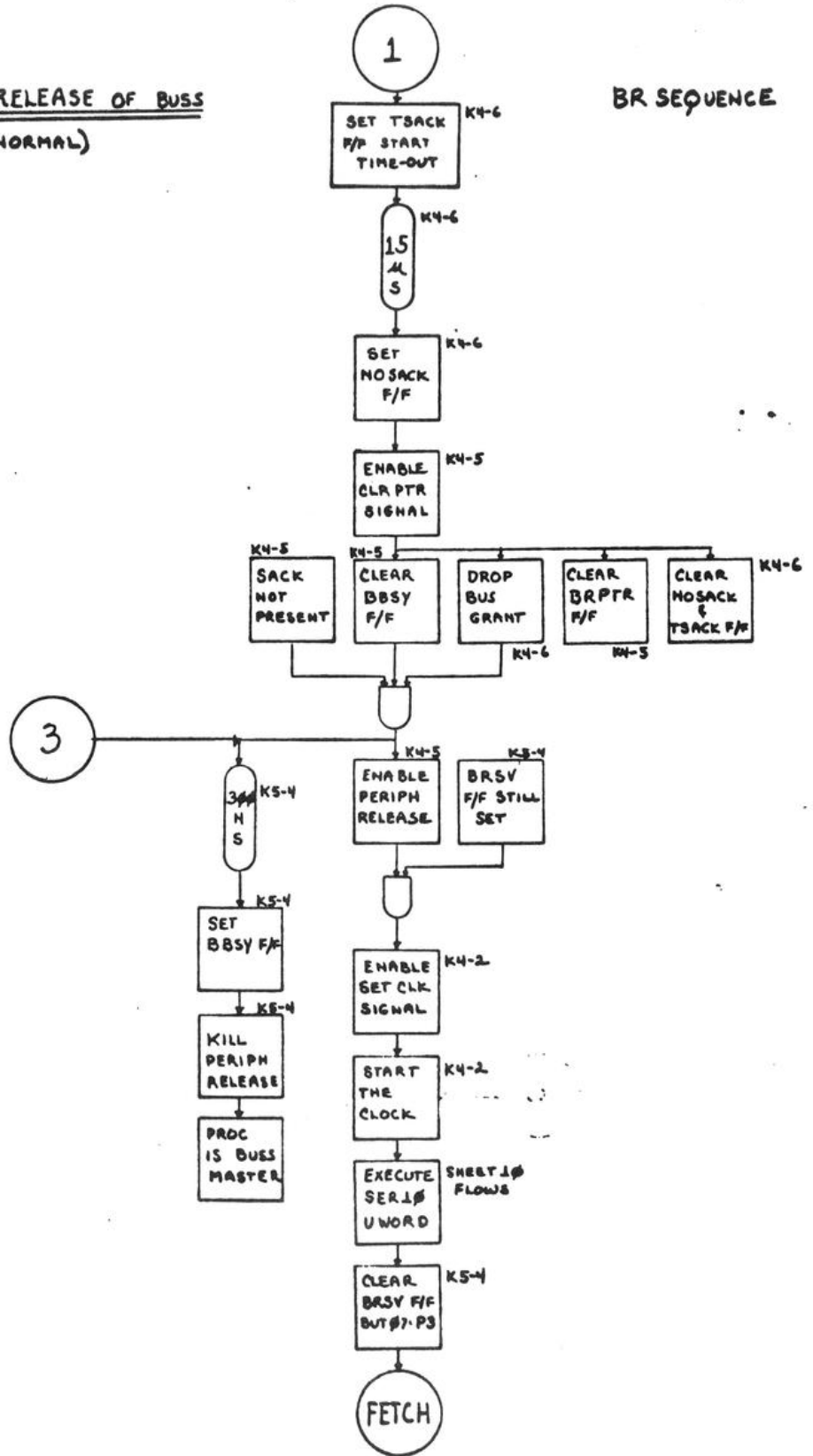
2-45



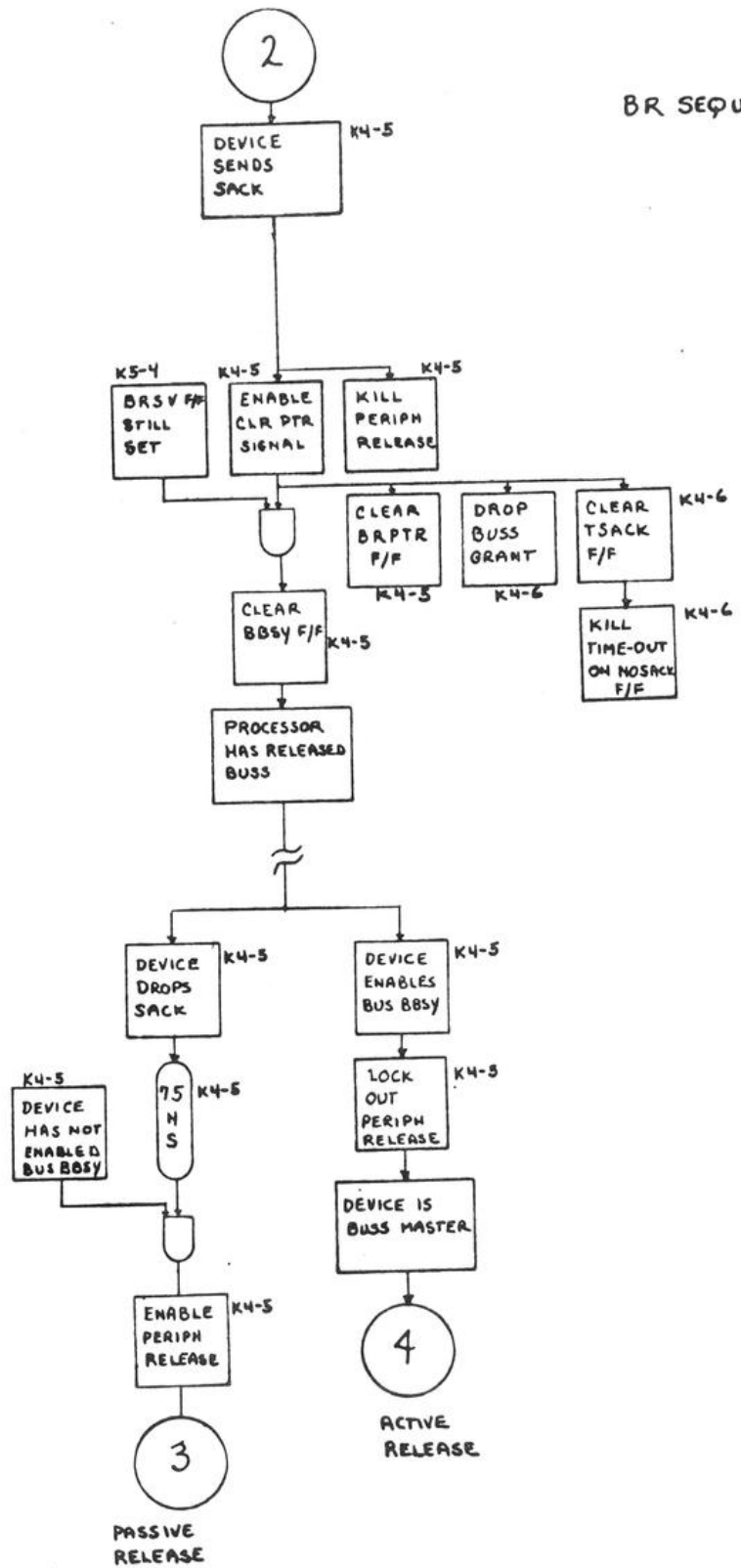


PASSIVE RELEASE OF BUSS
(ABNORMAL)

BR SEQUENCE



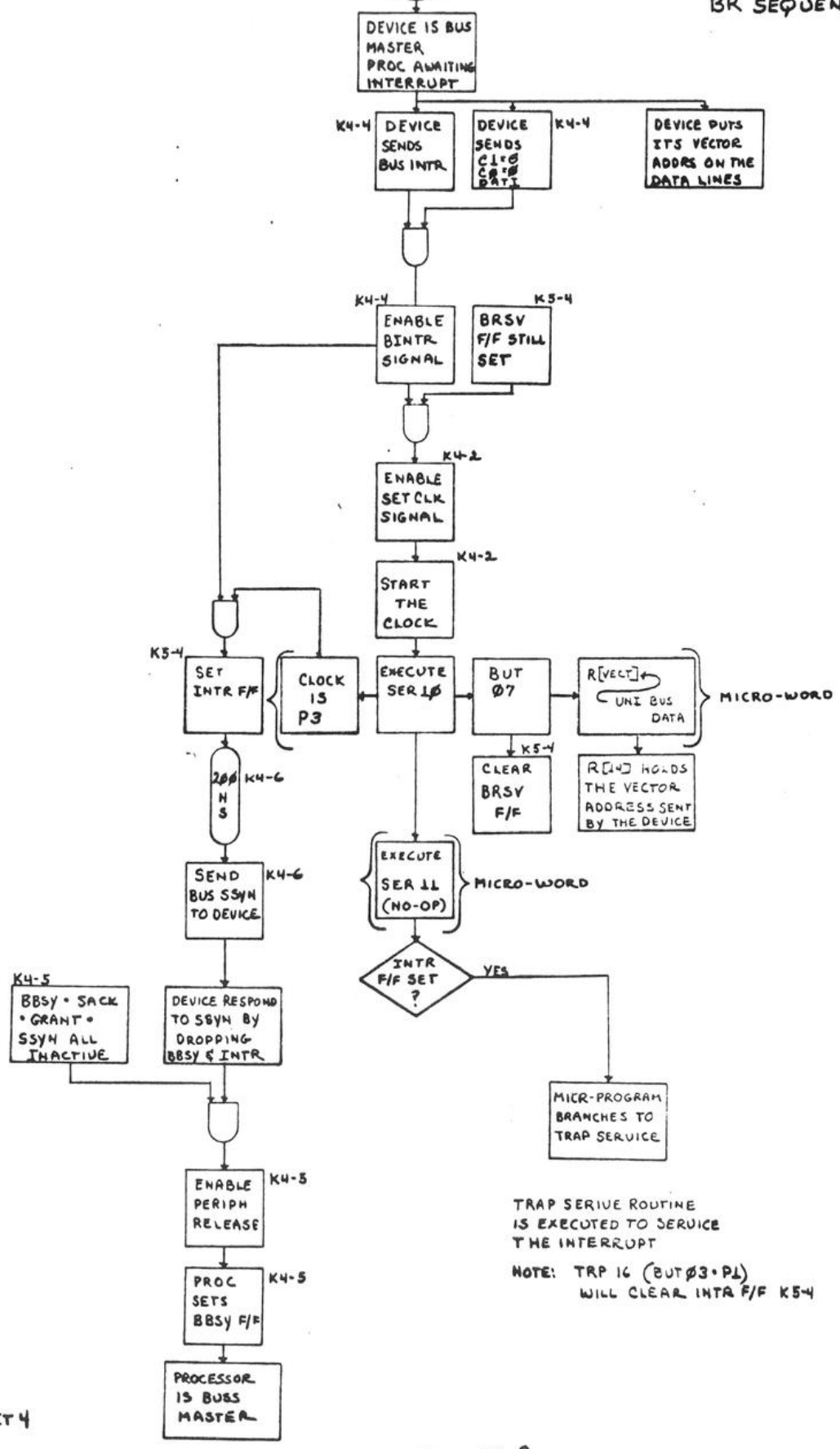
BR SEQUENCE



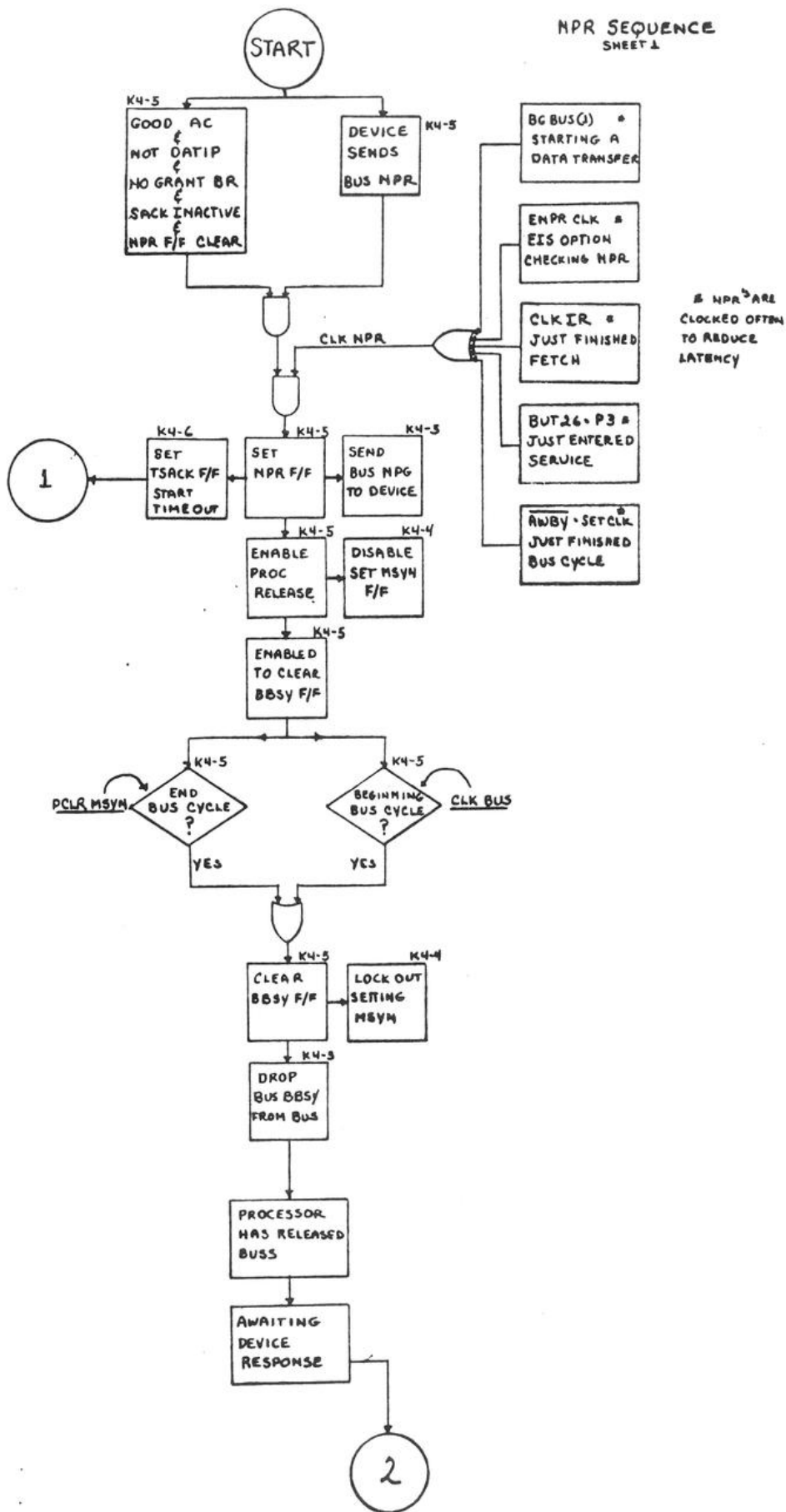
2-49

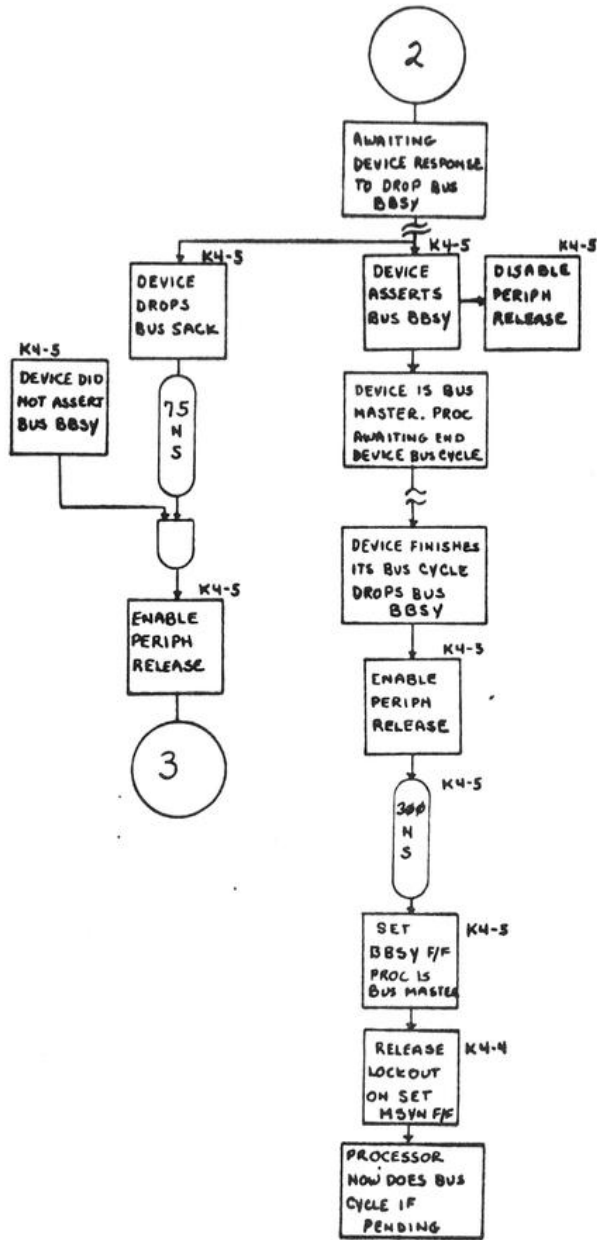
4

BR SEQUENCE

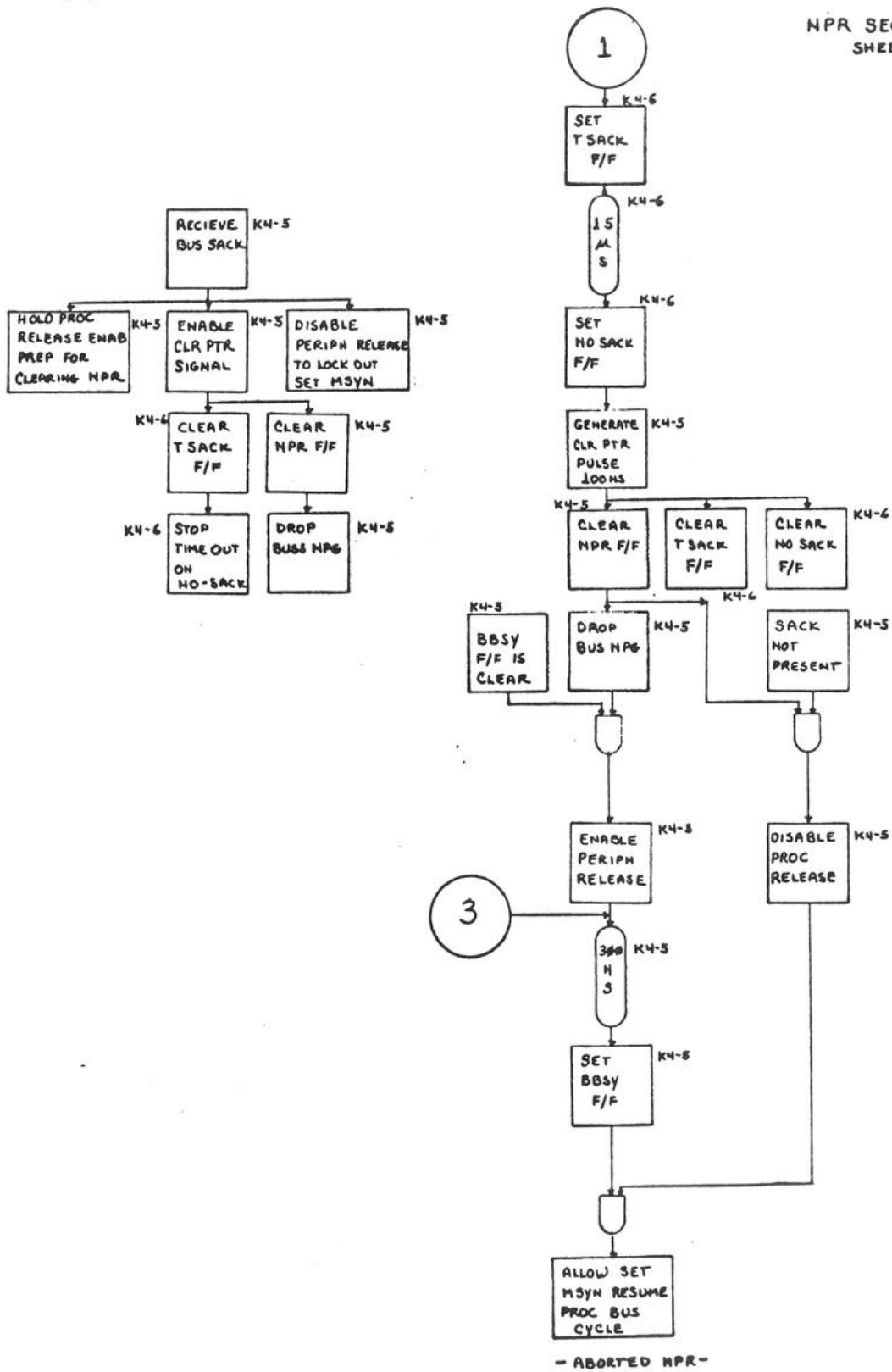


TRAP SERVICE ROUTINE IS EXECUTED TO SERVICE THE INTERRUPT
 NOTE: TRP 16 (BUT 03-PL) WILL CLEAR INTR F/F K5-4





NORMAL TERMINATION



- ABORTED NPR -

PDP 11/40

WEEK

2

EXAM

1. TO DISPLAY THE UNI-BUS DATA LINES ON THE CONSOLE DATA DISPLAY, BITS $U\langle 24:23 \rangle$ OF THE U WORD MUST BE PROGRAMMED AS:

- A. $\emptyset\emptyset$
- B. $\emptyset L$
- C. $L\emptyset$
- D. LL

2. THE MICRO-INSTRUCTION SHOWN BELOW IS BEING EXECUTED. WHAT IS THE STATE OF $UREG\langle 16:\emptyset9 \rangle$?

- A. $\emptyset\emptyset 11\emptyset 1\emptyset L$
- B. $1\emptyset\emptyset 11\emptyset\emptyset L$
- C. $\emptyset\emptyset\emptyset 11\emptyset\emptyset L$
- D. $\emptyset\emptyset 1\emptyset 1\emptyset 1\emptyset$

PI: B, R[SOURCE] \leftarrow D

3. DURING THE MICRO-INSTRUCTION THAT ENABLES DELIVERING THE RESULTS OF THE INSTRUCTION SHOWN BELOW, WHAT WOULD BE THE STATE OF $WRH(I)$ AND $WRL(J)$ (REFER TO K2-7)

- A. H, H
- B. H, L
- C. L, H
- D. L, L

$6\emptyset\emptyset$ MOV B(I), %2

$R1 = 5\emptyset3$

4. WHICH OF THE FOLLOWING ELEMENTARY OPERATIONS DICTATES THAT A CLOCK LENGTH OF THREE MUST BE SPECIFIED?

- A. $D \leftarrow R[SP] \text{ MINUS } 2$
- B. $R[PC] \leftarrow D$
- C. $R[SF] \leftarrow \text{UNIBUS DATA}$
- D. $R[PC] \leftarrow R[PC] \text{ PLUS } 2$

5. WHICH OPERATION SHOWN BELOW REQUIRES TWO MICRO-INSTRUCTIONS TO EXECUTE?

- A. $R[PC] \leftarrow R[PC] \text{ PLUS } 2$
- B. $D \leftarrow R[DEST] \text{ PLUS UNIBUS DATA}$
- C. $B \leftarrow R[SOURCE]$
- D. $BA \leftarrow R[SF] \text{ PLUS } B$

6. REFER TO K3-2 PRINT. THE MICRO-INSTRUCTION BEING EXECUTED IS ENCODED TO BUT JMP+JSR. WHICH BUT MULTIPLEXOR CHIP IS SELECTED

- A. E82
- B. E72
- C. E81
- D. E97

7. THE MICRO-INSTRUCTION PRESENTLY BEING EXECUTED SPECIFIES A CLOCK LENGTH OF THREE. THE NEXT MICRO-INSTRUCTION WILL BE CLOCKED INTO THE UREG AT THE:
- A. LEADING EDGE OF P2
 - B. TRAILING EDGE OF P3
 - C. LEADING EDGE OF P3
 - D. TRAILING EDGE OF P2

BEFORE ANSWERING QUESTIONS 8 THRU 10 COMPLETE A MICRO-PROGRAM WORKSHEET FOR THE INSTRUCTION SHOWN BELOW. START AT FET 02 AND INCLUDE ALL MICRO-INSTRUCTIONS FROM START TO FINISH.

→ 500 - CMP 702, (3) R2 = 350
502 - HALT R3 = 500

8. IF YOU MANUALLY CLOCK THE MICRO-PROGRAM UNTIL PUPP = 267, YOU SHOULD OBSERVE _____ IN THE BUFP LIGHTS OF THE MAINTENANCE MODULE?
- A. 266
 - B. 220
 - C. 225
 - D. 224

9. IF YOU MANUALLY CLOCK UNTIL PUPP=367
YOU SHOULD OBSERVE _____ IN THE
DATA LIGHTS ON THE CONSOLE?

- A. 020213
- B. 060134
- C. 160035
- D. 160135

10. WHAT SHOULD BE IN THE CONSOLE ADDRESS DISPLAY
WHEN PUPP=161

- A. 476
- B. 500
- C. 502
- D. 504

11. YOU ARE MANUALLY CLOCKING THE MICRO-PROGRAM
TO VERIFY THE INSTRUCTION SHOWN BELOW. THE NEXT
MICRO-WORD EXECUTED AFTER SSL03 SHOULD BE

- A. DOP16
- B. DOP17
- C. DOP18
- D. DOP19

INCB %2

R2=100

12. DURING EXECUTION OF A ROLB INSTRUCTION, WHICH DATA FACILITY DOES THE ACTUAL SHIFTING ?

- A. B MUX
- B. D MUX
- C. B REG
- D. ALU

13. THE INSTRUCTION SHOWN BELOW IS BEING SINGLE CLOCKED. THE BUT INST L IN FET \emptyset 4 SHOULD ACTIVATE MICRO-BRANCH CONTROL SIGNALS

- A. BUBC \emptyset AND BUBC1
- B. BUBC1 AND BUBC2
- C. BUBC3 AND BUBC4
- D. BUBC2 AND BUBC4

RTS 3

14 REFER TO SHEET 3 OF FLOWS. DURING EXECUTION OF THE MICRO-INSTRUCTION TAGGED DST16, WHAT SHOULD BE THE STATE OF SBMLL AND SBML \emptyset ON K2-5

- A. L, L
- B. H, L
- C. L, H
- D. H, H

15. CONSIDER THE PRINCIPLE OF MICRO-BRANCHING USED IN THE KD-LLA. IF A MICRO-WORD HAS A BASE ADDRESS OF 37ϕ , HOW MANY ADDRESS PATHS ARE OPEN TO US IN ADDRESSING THE NEXT MICRO-WORD. ASSUME BUT37

- A. 2
- B. 3
- C. 6
- D. 8

16. WHEN SINGLE CLOCKING THE MARK INSTRUCTION, YOU STOP THE SEQUENCE WITH PUPP = 354. IF YOU SCOPED SDML(1) AND SDM ϕ (1) ON K2-5 YOU WOULD EXPECT TO OBSERVE

- A. HIGH, HIGH
- B. LOW, LOW
- C. HIGH, LOW
- D. LOW, HIGH

17. YOU ARE CHECKING OUT THE DEPOSIT OPERATION BY DEPOSITING ALL ONES INTO LOCATION 500. YOU MANUALLY CLOCK UNTIL PUPP=67. WHAT SHOULD YOU OBSERVE IN THE CONSOLE ADDRESS DISPLAY?

- A. 177777
- B. 500
- C. 177500
- D. 177570

18. REFER TO K1-7 PRINT: WHICH OF THE FOLLOWING BUS ADDRESSES WILL THE SIGNAL ^{ENABLE} BOVFL STOP?

- A. 400
- B. 370
- C. 350
- D. 330

19. THE MICRO-PROGRAM DOES A JAMOPP TO LOC 002 FOR ANY MICRO-INSTRUCTION THAT SPECIFIES A DATA TRANSFER (DATI OR DATO) YOU ARE GETTING PROPER Ssyn RESPONSE TO MSYN. TROUBLE HAS BEEN ISOLATED TO THE K4 MODULE. WHICH CHIP

- A. E20
- B. E56
- C. E38
- D. E10

20

WHILE CHECKING OUT THE CONSOLE, YOU NOTE THAT YOU CAN EXAMINE REGISTERS BUT CANNOT EXAMINE ANY LOCATION ON THE BUS. YOU SINGLE CLOCK THRU AN EXAMINE OF LOC 500 AND FIND THAT THE MICRO-PROGRAM SKIPS AROUND EXM06, EXM07 AND EXM08 BACK INTO THE CONSOLE LOOP. THE PROBLEM IS MOST LIKELY CHIP

A. E82

E. E98

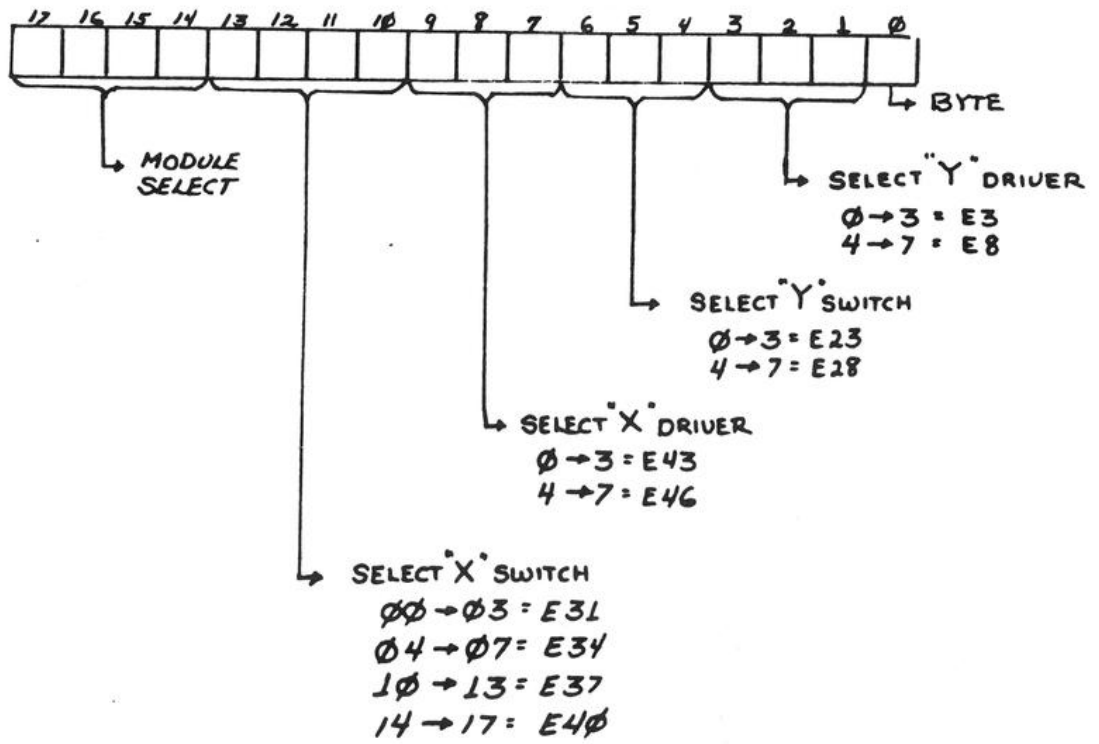
C. E81

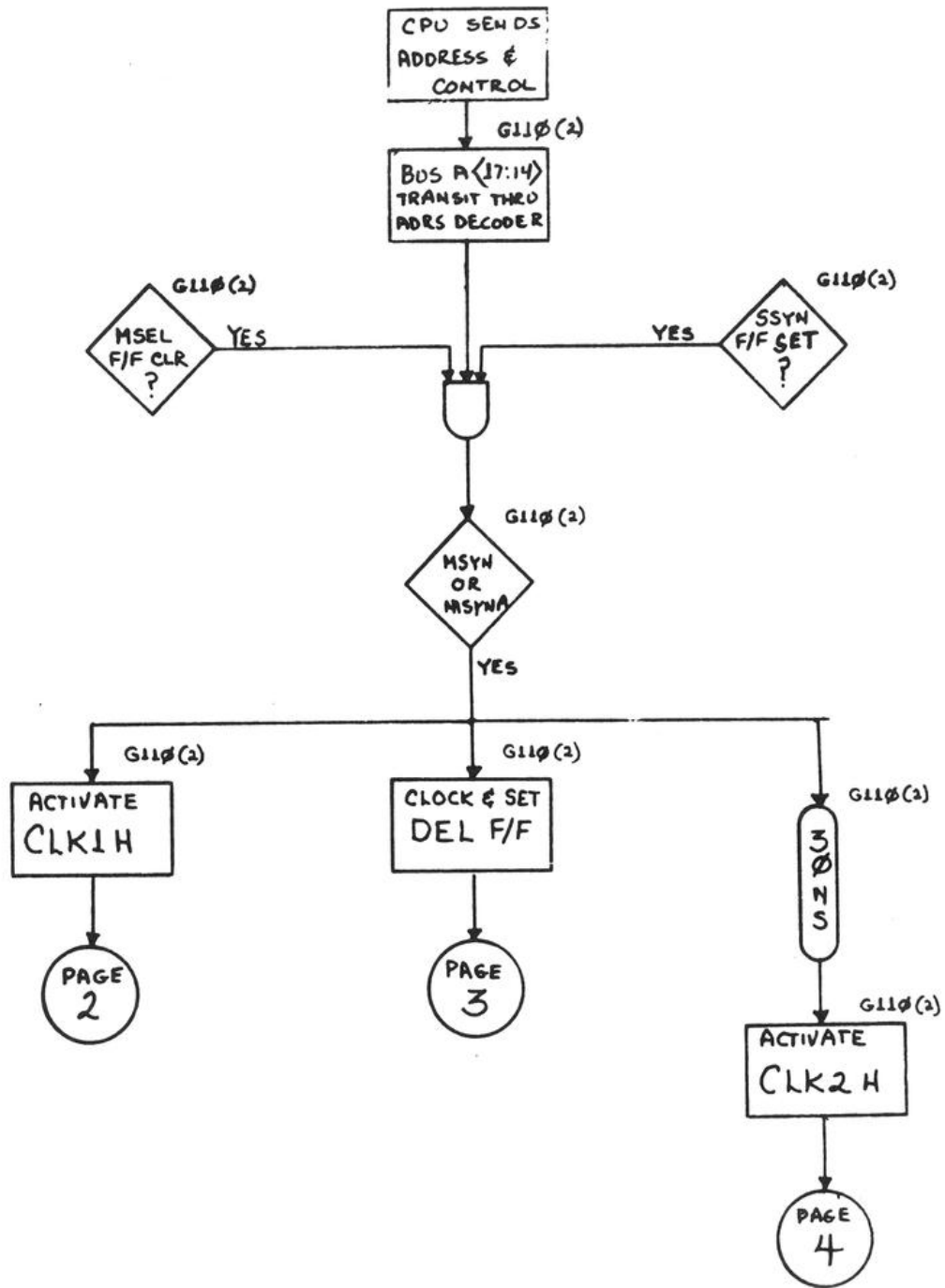
D. E73

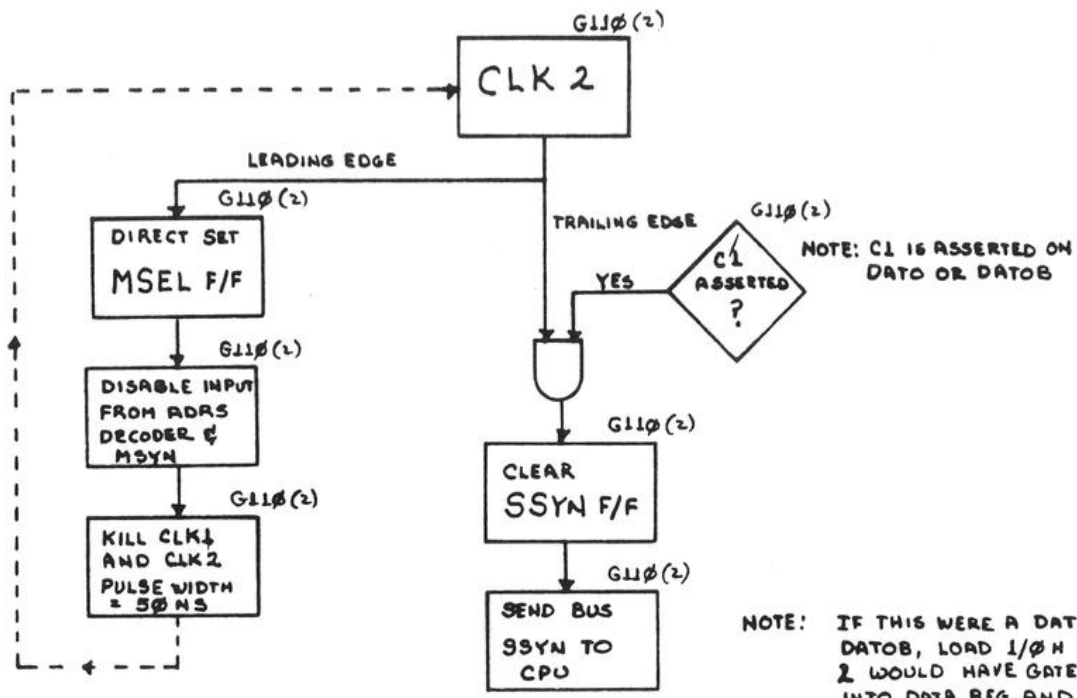
MM-11

MEMORY

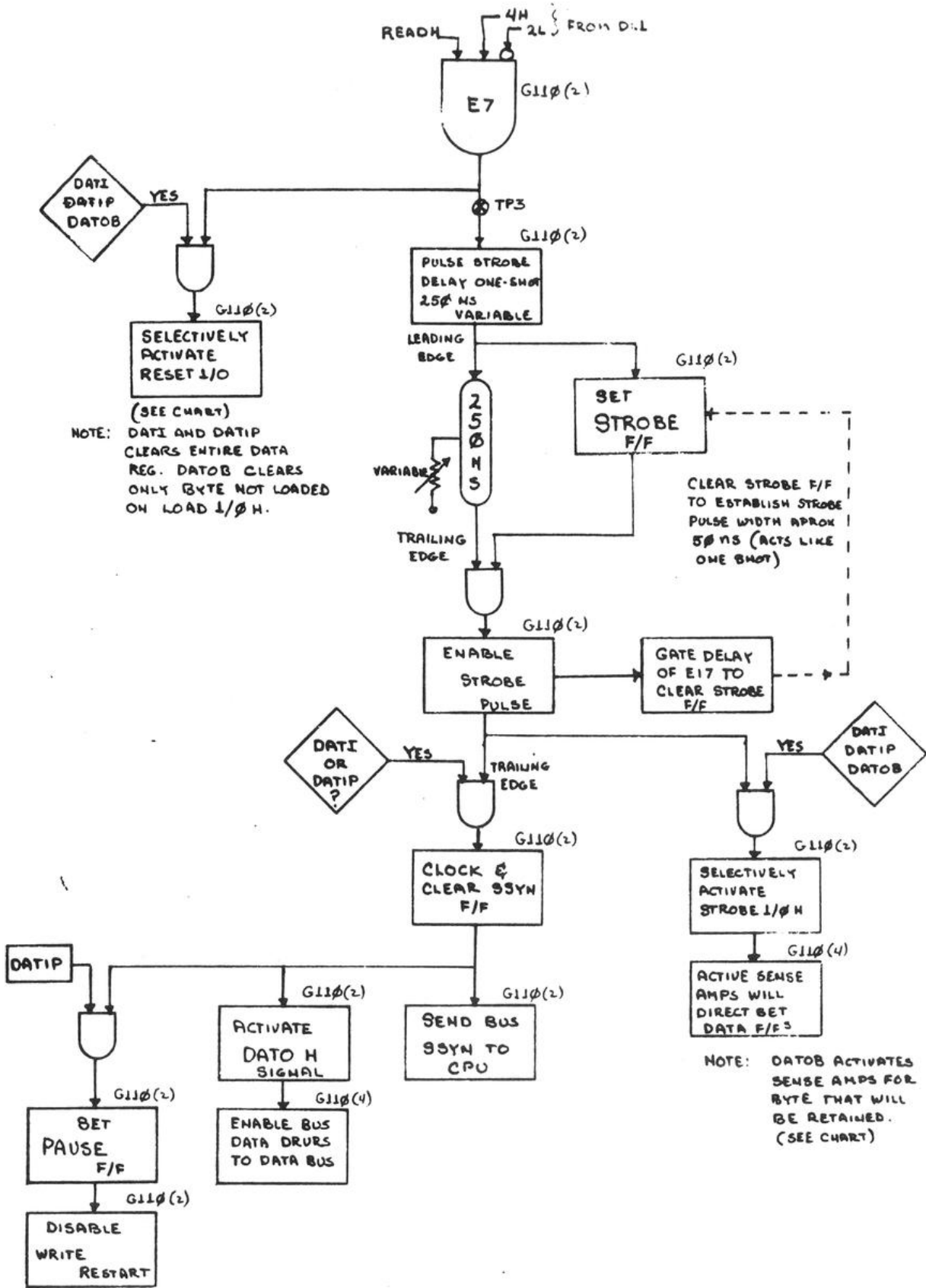
MEMORY ADDRESS FORMAT

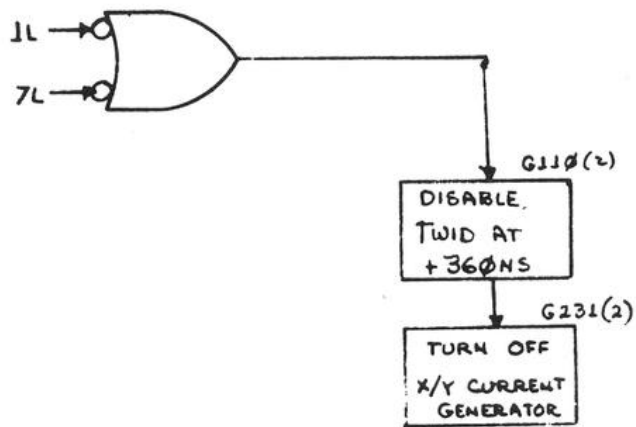
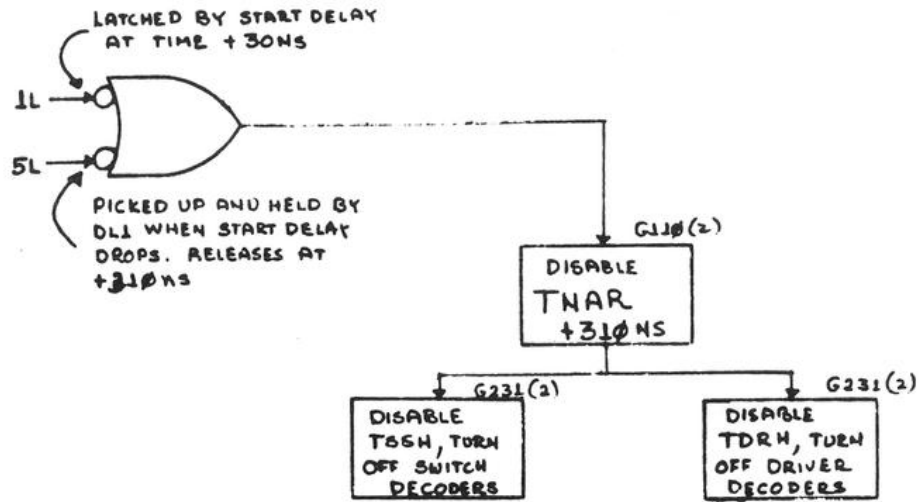


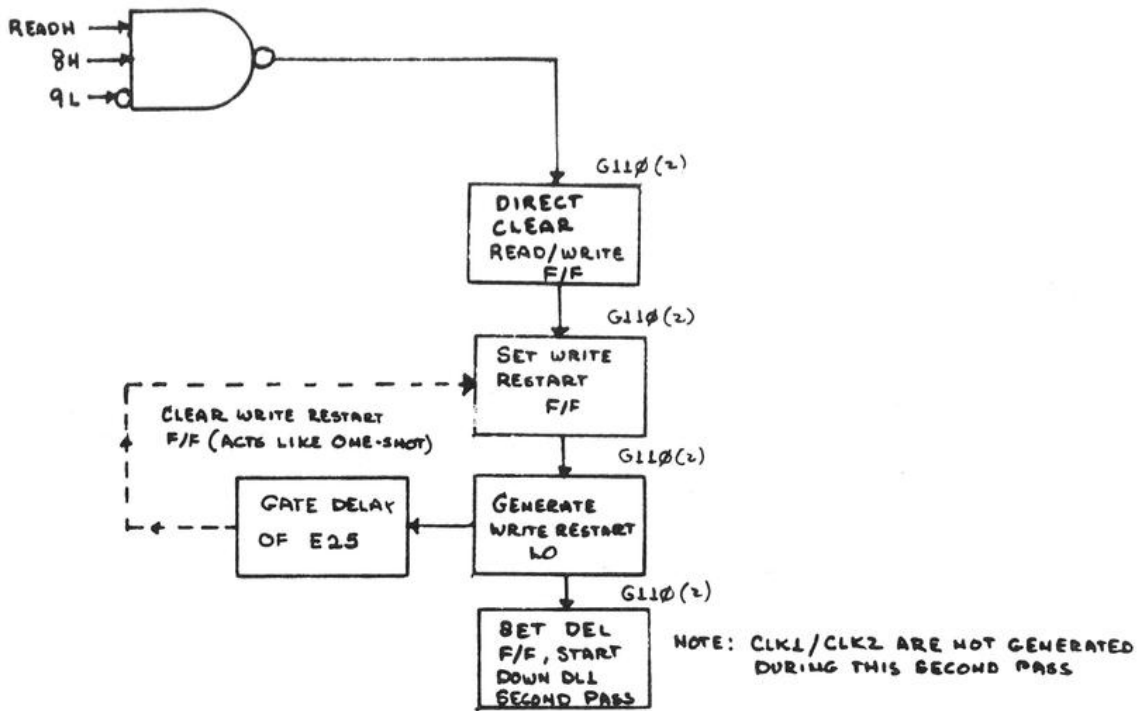




NOTE: IF THIS WERE A DAT0 OR DAT0B, LOAD 1/φH ON PAGE 2 WOULD HAVE GATED DATA INTO DATA REG AND BUS Ssyn WOULD BE PROPER RESPONSE. NOTE HOW EARLY IN MEM CYCLE Ssyn IS SENT ON DAT0/DAT0B







A SECOND PASS IS MADE DOWN DLL WITH THE READ/WRITE F/F CLEAR. THIS DOES A WRITE RESTORE AT THE SELECTED LOCATION INHIBIT DRIVERS GO ON WITH TWID AND SENSE AMPS ARE DISABLED DURING THIS PASS.

