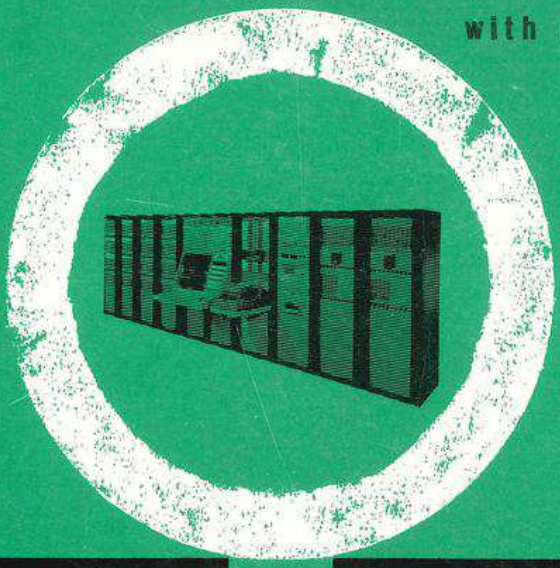
TRICE
THEORY AND MAINTENANCE MANUAL

with Illustrated Parts List



CSP-151

Packard Bell Computer

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with
Illustrated Parts List

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FIGURES (Cont)

TABLES

1. GENERAL INFORMATION

A. SCOPE OF MANUAL

This manual contains general and specific information which describes the theory of operation and maintenance procedures for Transistorized Realtime Incremental Computer Expandable (TRICE) systems. Written text is augmented with appropriate illustrations, such as block diagrams, logic diagrams or schematic diagrams. Information within this manual is written to the level of an electronic technician having a working knowledge of transistorized digital circuits and a rudimentary knowledge of calculus to the extent of knowing the concepts of integration and differentials.

B. SCOPE OF SECTION

This section of the manual contains general information which describes the overall purpose and capabilities of the TRICE system and specific information which describes the physical and electrical characteristics of the system and sub-assemblies within the system.

C. IDENTIFICATION OF EQUIPMENT

TRICE systems are manufactured by Packard Bell Computer, a division of Packard Bell Electronics, Los Angeles, California. The frontispiece is an overall view of a typical TRICE system.

D. PURPOSE, USE, AND CAPABILITIES OF TRICE

Each TRICE system is a special purpose digital computer which contains digital differential analyzer modules which are inter-connected via a patchboard to solve mathematical problems involving differentials with the speed normally associated with analog computers and the accuracy inherent to digital computers. Conventional digital modules and circuits are used within the timing, control, and storage circuits and permit the internal operations of the TRICE to proceed automatically upon receipt of appropriate data and instructions from an input device. The results of any computation may be outputted to visual displays on the front panel or to an appropriate output device.

The overall capabilities of a TRICE system is dependent upon the number of options incorporated into the basic system as described in the subsequent paragraph.

E. DESCRIPTION OF TRICE (Figures 1-1 and 1-2)

Figure 1-1 is a typical TRICE system and Figure 1-2 is a block diagram of the same. Both of these drawings illustrate that a basic TRICE system is comprised of a patchboard, control and indicator panel, control unit, buffer register, keyboard, and a TMB-5 rack containing digital differential analyzer modules (TRICE modules). The function of these components is described in subsequent paragraphs.

E-1. PATCHBOARD

The patchboard permits the individual TRICE modules to be inter connected in accordance with the dictates of the problem to be solved.

FIGURE I-1. TRICE SYSTEM (MAJOR COMPONENTS)

E-2. CONTROL AND INDICATOR PANEL

The control and indicator panel contains function switches which work in conjunction with the patchboard for determining the routing of signals between the TRICE modules, and visual indicators which permit operating personnel to monitor the contents of the various registers as well as the presence or absence of primary power.

E-3. CONTROL UNIT

The control unit is comprised primarily of circuits which permit the overall operation of the TRICE to be synchronized with associated input and output devices.

E-4. BUFFER REGISTER

The buffer register serves as a mediating device between the TRICE modules and the PB-250. The buffer register is capable of exchanging information with a TRICE module at a rate of 3 megacycles and with the PB-250 at a rate of 2 megacycles. The contents of the buffer register is also made available for visual display by operating personnel.

E-5. KEYBOARD

The keyboard is comprised of 35 pushbutton type switches which permit operating personnel to manually enter control and data signals to the TRICE. Individual keys are labelled with appropriate identification as to function or data.

E-6. TMB-5 RACK

Each TMB-5 rack contains up to 16 integrator modules, 4 variable multiplier modules, 4 constant multiplier modules, 4 summer modules,

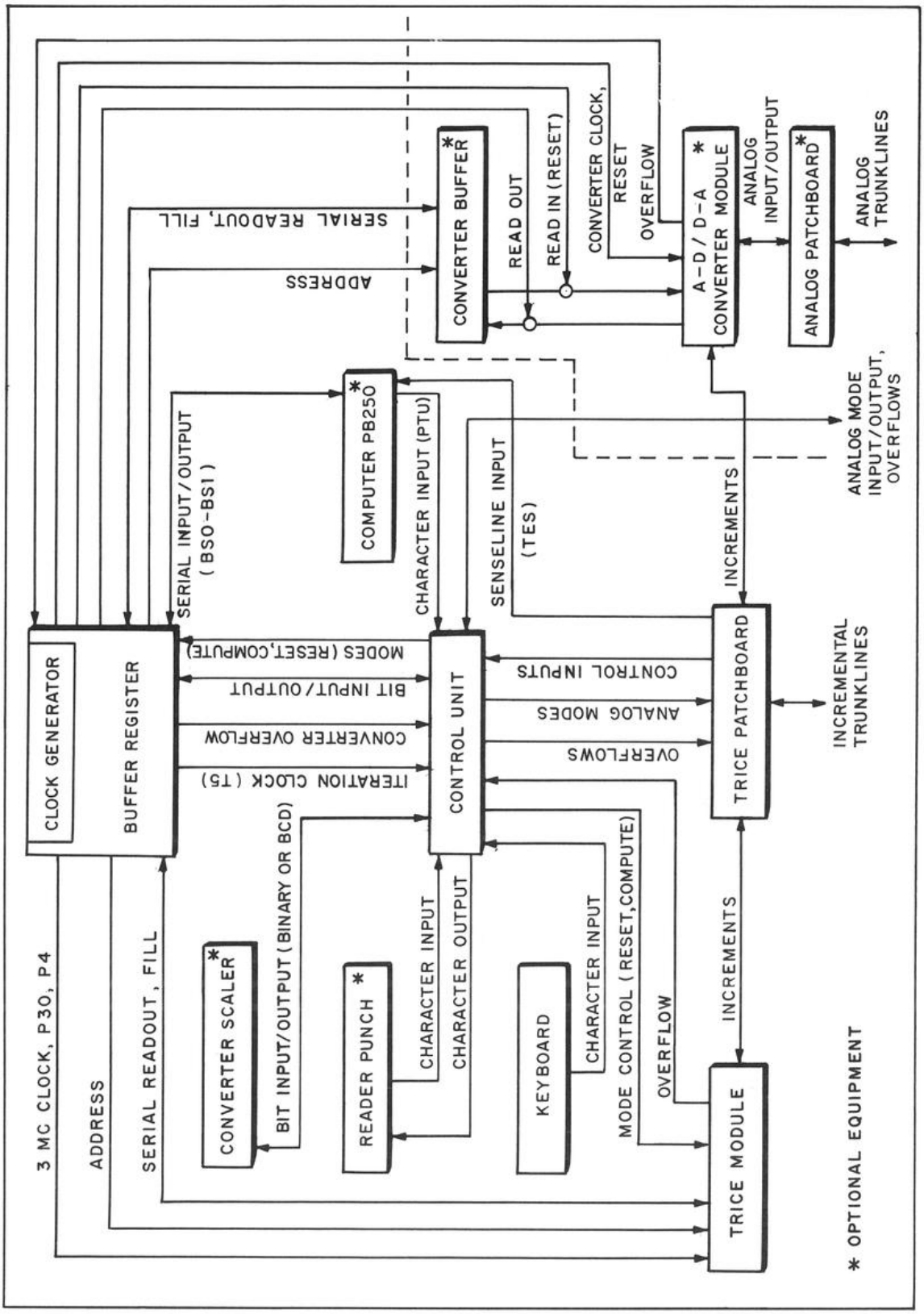

FIGURE I-2. TRICE (BLOCK DIAGRAM)

and 4 servo modules. A brief functional description of these modules is given in subsequent paragraphs.

E-6a. Integrator

Each integrator module contains three registers, designated as R, Y, and I, and associated logic circuits which permit the basic equation (dz = ydx) to be mechanized. The I register is used to store a numerical value which represents the initial condition of the problem to be solved. The Y register permits a summation of individual dy input pulses which, in turn, are added into the R register when a dx pulse is received. The contents of all registers are restricted to be a fraction. A carry pulse, designated as dz, is generated whenever the contents of the R register exceeds a fractional value.

E-6b. Constant Multiplier

A constant multiplier module contains two registers, designated as R and I registers, and associated logic circuits which permit the equation (dz = Kdx) to be mechanized. The I register contains a constant which can be added into the R register each time a dx pulse is generated. Thus, by repetitive addition a multiplication function is performed. The R register is restricted to containing only a fraction. Any carry pulses which occur out of the R register are designated as dz pulses.

E-6c. Variable Multiplier

Each variable multiplier module contains five registers, designated as R, X, Y, Ix, and Iy, which permit the equation d(xy) = ydx + xdy + dxdy to be mechanized. The Ix register is used to store the initial value of a problem which is to be transferred into the X register. The Iy register stores an initial value which is to be transferred into

the Y register. The X register accumulates (or summates) the individual dx inputs, and is added to the R register whenever a dy pulse is generated. The Y register accumulates the individual dy inputs, and is added to the R register whenever a dx pulse is generated. The R register is common to the X and Y registers and permits an algebraic summation of the two registers to be performed. The R register is restricted to containing a fractional value and generates a dz output whenever the contents exceed unity value in either a plus or minus direction.

E-6d. Servo

Each servo module contains two registers, designated as the Y and I registers, and functions as a special computing element which is used as a nulling device in the solution of differential equations or as a decision element in the generation of discontinuous or non-linear functions. The I register is used to store the initial value of the problem and the Y register serves as an accumulator of the individual dy pulses received.

E-6e. Summer

The summer module is comprised basically of logic gates which permit a summation to be performed on as many as six different dy inputs. The summer module can only be used in conjunction with a Y register of an integrator or servo module.

E-7. OPTIONS

The basic TRICE system described above may be expanded by various optional equipment described in subsequent paragraphs which permit the capabilities and speed of the TRICE system to be enhanced.

E-7a. TMB-5 Rack

Additional TMB-5 racks containing TRICE modules may be added to the basic system whenever more complex problems are to be solved. A maximum of four TMB-5 racks may be incorporated into one system.

E-7b. TMB-6 Rack

Whenever the TRICE system is to work in conjunction with analog equipment (i.e., plotter), a TMB-6 rack containing a maximum of 12 analog to digital converters, 12 digital to analog converters, and 6 reference power supplies may be readily added to the system. Each digital to analog converter is capable of converting 14 binary bits (including sign) into an equivalent analog voltage within the range of ±6-2/3 volts. Each analog to digital converter is capable of digitizing an analog input of ±100 volts into 14 binary bits (including sign). The reference power supplies are used to generate precise voltages as required by the converters. Note: Each analog to digital converter may be converted into a digital to analog converter by positioning a front panel control on the converter.

E-7c. PB-250 Computer

To improve the speed of transferring data and control signals into and out of the TRICE, a PB-250 computer may be used. PB-250 PTU commands are used to set up the control circuits. A BSO command permits data to be transferred serially from the PB-250 into the buffer register of the TRICE and a BSI command permits data to be transferred serially from the buffer register of the TRICE into the PB-250. PB-250 TES commands can sense the state of TRICE signals via sense inputs on the TRICE patchboard.

E-7d. Paper Tape Reader and Punch

The paper tape reader and punch permits digital data to be transferred into and out of the TRICE at the rate of 60 characters per second. Paper tapes containing data and control signals may be produced with an off-line Flexowriter.

E-7e. Decimal Converter Scaler

The decimal converter scaler is capable of converting binary information into decimal information and vice versa. The converter scaler is normally used whenever the information on the paper tape is in a decimal format. Operations within the TRICE are performed using a straight binary configuration.

E-7f. Linkage

When the TRICE system is used in conjunction with analog computers or other input/output devices, interfacing or linkage circuits are normally required. These circuits are housed within a separate equipment rack.

F. LEADING PARTICULARS

Refer to Table 1-1 for physical characteristics of the individual TRICE modules and Table 1-2 for the operating characteristics. Table 1-3 lists the major components of a basic TRICE system as well as optional modules and input/output devices.

Table 1-1.

TRICE SYSTEM PHYSICAL CHARACTERISTICS

Components	Height (in.)	Depth (in.)	Length (in.)	Width (in.)
Overall Basic System	72	28	72	-
Modules				
Integrator	12-3/4	-	20	1-3/4
Constant Multiplier	12-3/4	-	20	1-3/4
Servo	12-3/4	-	20	1-3/4
ΔY Summer	12-3/4	-	20	1-3/4
Variable Multiplier	12-3/4	-	20	3-1/2

Table 1-2.

OPERATING CHARACTERISTICS

	3.14573 Mc Clock Frequency	3.00000 Mc Clock Frequency
Word Length	24 bits	30 bits
Integration Rate	2^{17}/sec	10^{5}/sec
Word Time	7.629 μsec	10 μsec
Maximum Usable Word Length	20 bits	26 bits

2. TEST EQUIPMENT AND SPECIAL TOOLS

A. SCOPE OF SECTION

This section provides information concerning test equipment required for troubleshooting, maintenance, and repair of the TRICE system.

B. TEST EQUIPMENT

Table 2-1 lists test equipment required for troubleshooting, maintaining, and repairing the TRICE system.

Table 2-1.

TEST EQUIPMENT

Item	Description	Alternate	Purpose
1	Oscilloscope; Tektronix Corp., Type 533 with Type CA Preamplifier	An equivalent unit	Measures pulse rise time; shows waveforms visually.
2	Multimeter; Simpson Corp., Model 267	An equivalent unit	Measures resistance, current, and potential differences.

C. SPECIAL TEST EQUIPMENT

Table 2-2 lists the special test equipment required to assist in troubleshooting the TRICE system.

Table 2-2.

TRICE SYSTEM

SPECIAL TEST EQUIPMENT

Item	Description	Alternate	Purpose
1	TRICE MTT-1 Module Tester	An equivalent unit	To pinpoint malfunctions of TRICE computing modules.
2	TRICE DLT-1 Memory Tester	An equivalent unit	To pinpoint malfunctions of TRICE memory modules.

C-1. TRICE MTT-1 MODULE TESTER

The TRICE MTT-1 Module Tester is a self-contained unit which requires standard 115-vac power input, and generates its own dc voltages. It is built specifically for testing TRICE computing modules of the following types:

1) Integrator I5
2) Servo S5
3) Constant Multiplier CM5
4) Variable Multiplier VM5
5) Summer SU5

Refer to the MTT-1 Module Tester Operation and Maintenance Manual, CSP-154, for a detailed explanation on this equipment.

C-2. TRICE DLT-1 MEMORY TESTER

The TRICE DLT-1 Memory Tester is a self-contained unit requiring standard 115-vac power input, and generating its own dc voltages and timing signals. The timing logic can be switched for 24-bit, 30-bit, and 32-bit word length by a jumper-plug on the logic and timing module. The clock frequency can be either 3.000000 Mc or 3.145730 Mc, depending on frequency required.

Refer to the DLT-1 Memory Tester Operation and Maintenance Manual, CSP-155, for a detailed explanation of the TRICE memory tester.

3. THEORY OF OPERATION

A. SCOPE OF SECTION

This section describes the theory of operation for the TRICE system and for individual modules and control circuits. Written text is augmented by references to block diagrams, logic diagrams, schematic diagrams, timing charts, and logic equations.

B. GENERAL (Figure 3-1)

The TRICE computer system contains independent digital differential analyzer computing modules which operate in parallel and are controlled and interconnected through a control console. Each computing module operates serially. One-word recirculating registers and serial adders perform the mechanization of the digital differential analyzer algorithms. Communication between modules is incremental. In each iteration (word time), pairs of lines indicate the existence and sign of output increments of the computing modules. On an analog-type patchboard, these lines can be connected to the increment inputs of the computing modules according to the program (map).

Initial conditions and constants can be filled and digital output obtained through the input-output devices of the control console Figure 3-2. By means of an address register, each computing module can be selected for communication of its register contents to a common buffer register. Visual read-out of the register value is available from the buffer register indicator lights.

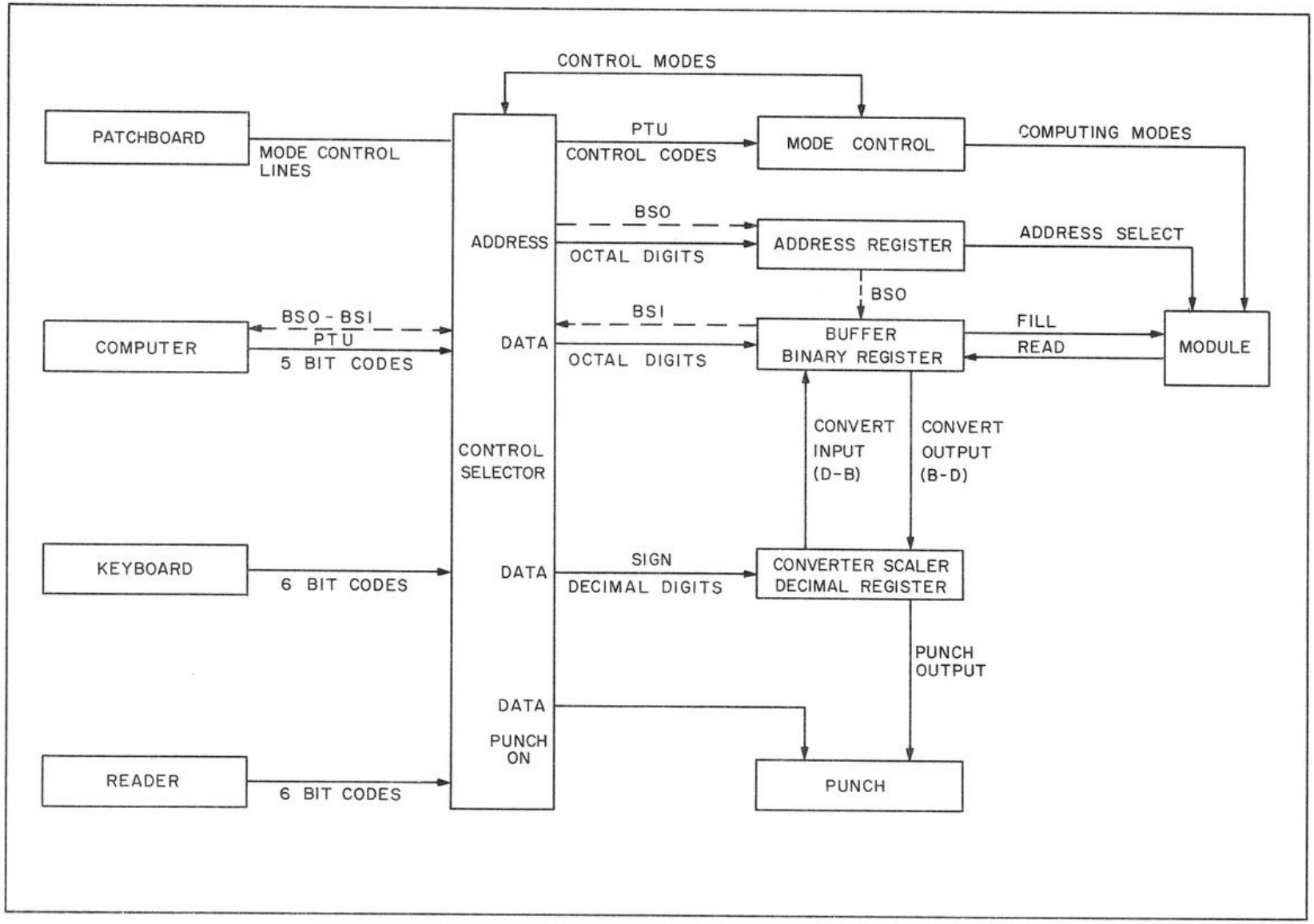

FIGURE 3-1. INPUT-OUTPUT CONTROL (BLOCK DIAGRAM)

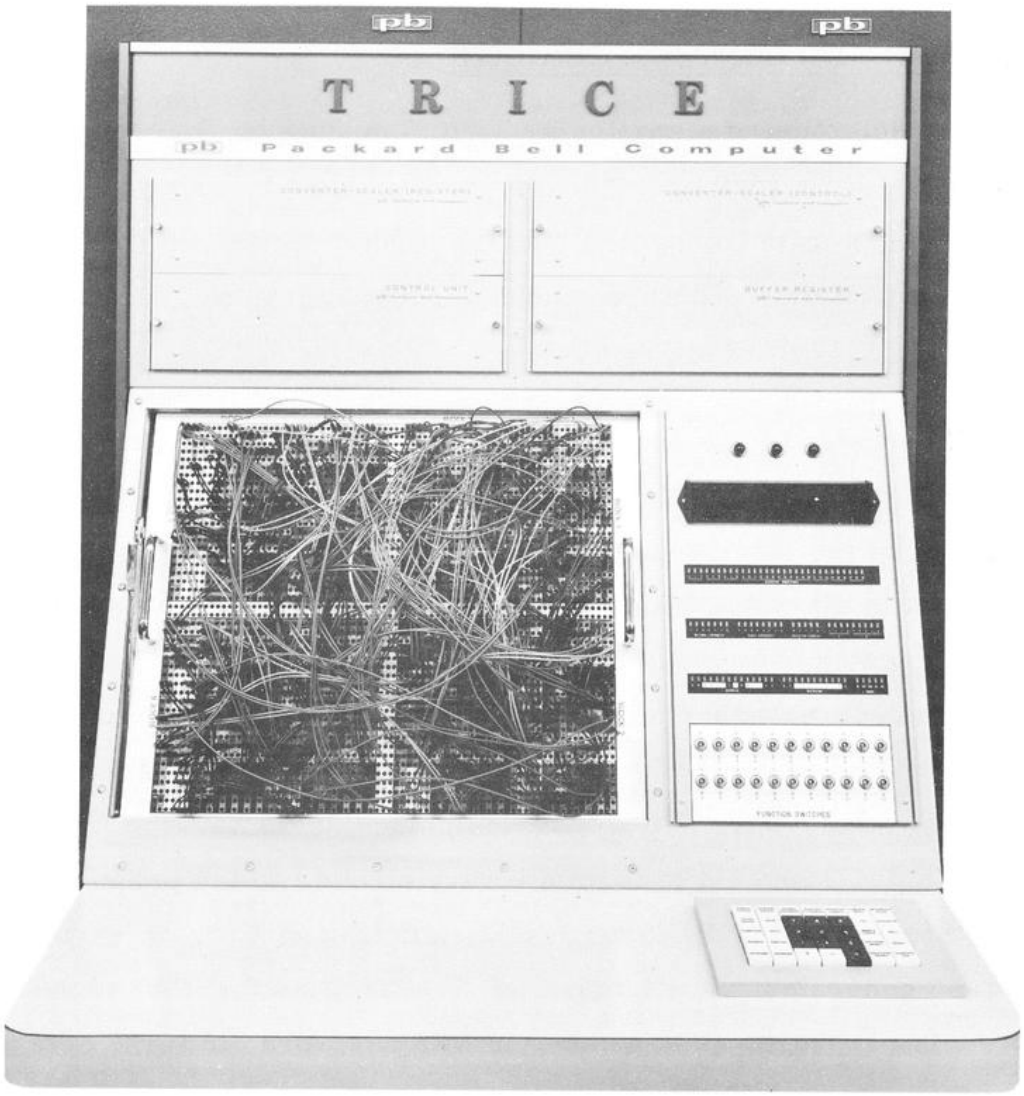

FIGURE 3-2. TRICE CONTROL CONSOLE

In addition, the buffer register can communicate with a PB 250 computer for format conversion, typewriter, and paper tape input-output.

C. TIMING AND CONTROL CIRCUITS

The selection of a particular TRICE module or converter for a subsequent fill or read operation is accomplished by using digital circuits to generate timing and control pulses. A description of these circuits is contained within the subsequent paragraphs.

C-1. TIMING

The source of all timing signals in TRICE is a crystal oscillator clock generator having a frequency of 3.000000 or 3.145730 megacycles. The output of the clock generator, as illustrated in Figure 3-3, is distributed to all of the TRICE modules, all of the converters, and to a binary counter comprised of flip-flops T1 through T5. Each TRICE module and converter module contains clock shaping and amplifying circuits which permit the clock pulses received via the coax cables to be reconstituted. Five flip-flops, designated as T1 through T5, are logically interconnected to form a binary counter which permits intra-word timing pulses of P1 through P32, P1 through P30, or P1 through P24 to be generated. The number of P pulses is a function of the number of bits per word. The number of bits per word, in turn, determine the basic frequency of the clock generator. As listed in Table 3-1 the clock frequency of a 30 bits per word TRICE system is 3.000000 megacycles. The clock frequency of a 32 or 24 bits per word TRICE system is 3.145730 megacycles. Tables 3-1 also lists the corresponding iteration rates and word times for each frequency.

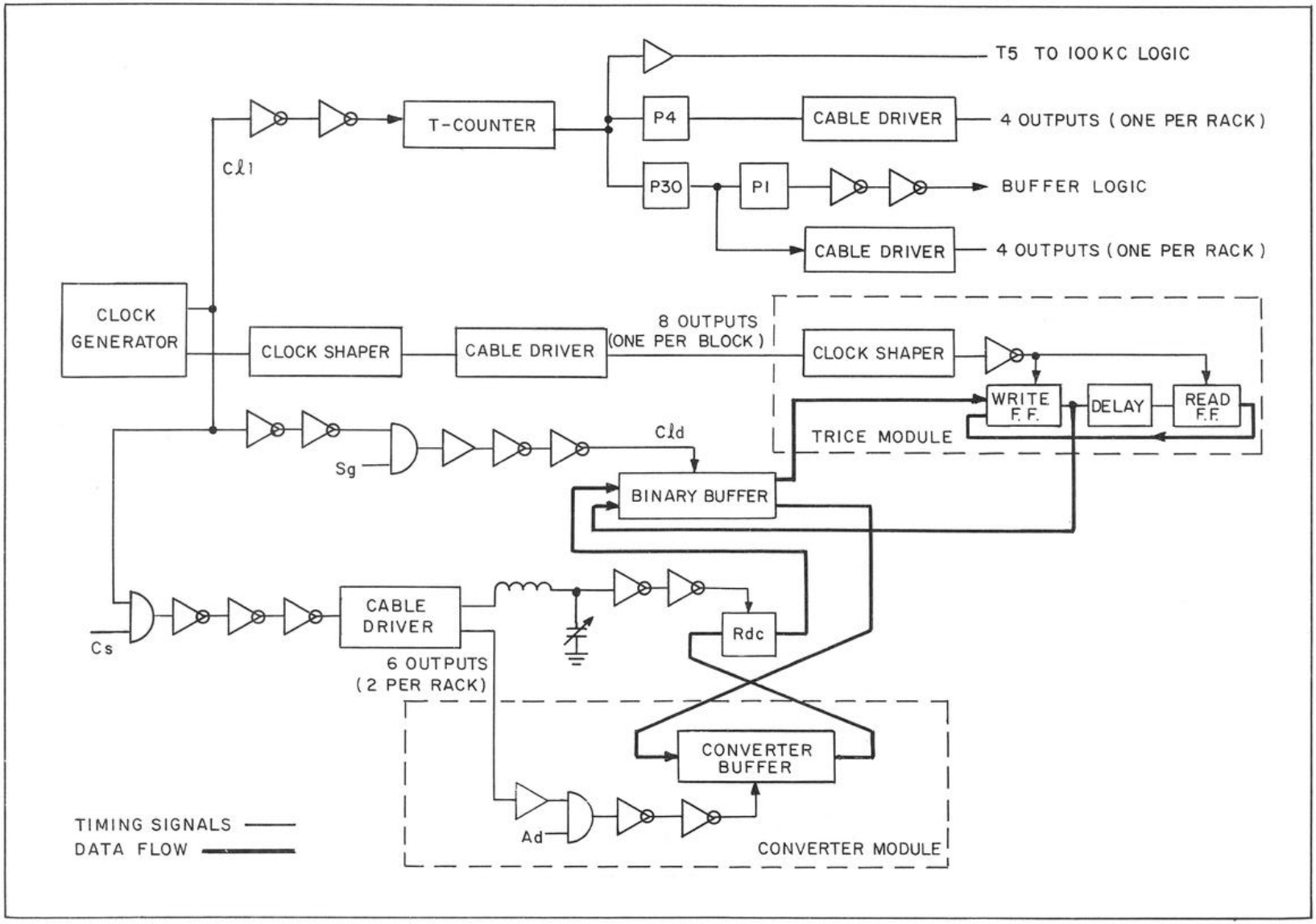

FIGURE 3-3. BASIC CLOCK DISTRIBUTION (TRICE SYSTEM)

Table 3-1.

CLOCK RATE AND ITERATION RATE

WORD TIMING

Clock Rate Pulses/Sec	Frequency Megacycles	Bit Time μ Seconds	Bits/Word	Iteration Rate (T5) Words/Sec	Word Time μ Seconds
$3 \cdot 2^{20}$	3.145730	.318	32	$3 \cdot 2^{15}$ or 98304/sec	10.17
$3 \cdot 10^{6}$	3.000000	.333	30	10^{5} or 100000/sec	10.00
$3 \cdot 2^{20}$	3.145730	.318	24	2^{17} or 131072/sec	7.62

Logic equations for the T1 through T5 flip-flops are as follows:

T1

$t1 = \overline{T1}C\ell 1$

$ot1 = T1C\ell 1$

T2

$t2 = \overline{T2}C\ell 1\ (T1\overline{P16})$

$ot2 = T2C\ell 1\ (T1\overline{P16})$

Note: The $\overline{P16}$ term is present only on modulo 30 counter.

T3

$t3 = \overline{T3}C\ell 1\ (T2T1)$

$ot3 = T3C\ell 1\ (T2T1)$

T4

$t4 = \overline{T4}C\ell 1\ (T3T2T1)$

$ot4 = T4C\ell 1\ (T3T2T1)$

Note: A $\overline{P16}$ term is added to both equations for modulo 24 counter only.

T5

$t5 = \overline{T5}C\ell 1\ (T4T3T2T1)$

$ot5 = T5C\ell 1\ (T4T3T2T1)$

In the preceeding equations, the $C\ell 1$ term is a true output from the clock generator and T or $\overline{T}$ signals are true and false signals from the individual T flip-flops as designated by the associated number. The $\overline{P16}$ signal is true at all times except at P16 time. This term is added to the AND gate controlling the resetting of flip-flop T2 only if the flip-flops are to function as a modulo 30 counter or to the AND gate controlling the resetting of the T4 flip-flop if the flip-flops are to function as a modulo 24 counter. The $\overline{P16}$ term is not used when the T1 through T5 flip-flops function as a modulo 32 counter.

Table 3-2 lists the various consecutive configurations of the T1 through T5 flip-flops for each mode of operation. The initial configuration of these flip-flops is defined to be that configuration in which all of the flip-flops are off. This configuration is designated as P1 time of each word. The terminal configuration of these flip-flops is defined

Table 3-2.

WORD TIMING: T-COUNTER SEQUENCE

	T1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1
	T2	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1
	T3	0	0	0	0	1	1	1	1	0	0	0	0	1	1	1	1	0	0	0	0	1	1	1	1	0	0	0	0	1	1	1	1
(32)	T4	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
	T5	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
	COUNT	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
	P-TIME	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32
	T1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1				
	T2	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1	1	1	0	0	1	1	0	0	1	1	0	0				
	T3	0	0	0	0	1	1	1	1	0	0	0	0	1	1	1	1	0	0	1	1	1	1	0	0	0	0	1	1				
(30)	T4	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	1	1	1	1	1	1				
	T5	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1				
	COUNT	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	18	19	20	21	22	23	24	25	26	27	28	29				
	P-TIME	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28				
	T1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1								
	T2	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1								
	T3	0	0	0	0	1	1	1	1	0	0	0	0	1	1	1	1	0	0	0	0	1	1	1	1								
(24)	T4	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1								
	T5	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1								
	COUNT	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	24	25	26	27	28	29	30	31								
	P-TIME	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24								

to be that configuration in which all of the flip-flops are on. This configuration is designated as P32 time within a 32 bit word, P30 time within a 30 bit word or P24 time within a 24 bit word. In the logic equations the corresponding timing signal is called P30. Table 3-2 illustrates that the configuration of the T1 through T5 flip-flops are identical for the first 16 bit times and the last eight bit times. The configuration of the flip-flops at P17 time is controlled by the $\overline{P16}$ term listed in previous equations. In a 32 bit per word system, the $\overline{P16}$ term is absent and hence the flip-flops function as a conventional binary counter where T1 is the least significant bit having a weight of 1 and T5 is the most significant bit having a weight of 16. In a 30 bit per word system, the $\overline{P16}$ term inhibits the resetting of flip-flop T2 at the end of P16 time and hence the counter is advanced by a count of three. In a 24 bit per word system, the $\overline{P16}$ term inhibits the resetting of flip-flops T4 at the end of P16 time and hence, the counter is advanced by a count of nine.

Flip-flops P1, P4 and P30 generate the designated timing pulses and are controlled by the following logic equations:

P30

$$p30 = \overline{P30}C\ell 1\,(T5T4T3T2\overline{T1})$$

$$op30 = P30C\ell 1$$

P1

$$p1 = \overline{P1}C\,\ell\,1P30$$

$$op1 = P1C\,\ell\,1$$

P4

$$p4 = \overline{P4}C\,\ell\,1\,(\overline{T5}\,\overline{T4}\,\overline{T3}T2\overline{T1})$$

$$op4 = P4C\,\ell\,1$$

Note: The P30 flip-flop is true during the last bit timing of each word regardless of the number of bits per word.

In addition, a P16 signal is generated by a diode logic gate which mechanizes the following equation:

$$P16 = \overline{T5}T4T3T2T1$$

The time interval between equivalent points of two successive T5 pulses defines the duration of one word time. Table 3-1 lists the word times as a function of the clock frequency.

C-2. CONTROL CIRCUITS

The overall operation of the TRICE system requires control circuits which permit the following:

a. Selection of a control mode such as KEYBOARD, READER, COMPUTER or PATCHBOARD.
b. Selection of a computing mode such as INTEGRATE, HALT, RESET or COMPUTE OFF.
c. Selection of a special computing mode such as SELECTED RESET, PATCHED RESET, INTEGRATE SLOW or SINGLE CYCLE.
d. Selection of input-output mode such as DISPLAY, ADDRESS, DATA or PUNCH OUTPUT.
e. Selection of input-output function such as READ or FILL.
f. Selection of a decimal converter scaler operation:
   Convert input, convert output, decimal exponent, scale exponent, register length.

Reader and Punch Output apply to the reader punch unit TRP1. The computer control mode enables the PB 250 for control of TRICE.

The decimal converter scale operations apply to the Decimal Converter Scaler Unit DCS1.

C-2a. Selection of Control Mode

The selection of a keyboard, paper tape reader, PB 250 computer or patchboard as an input device to control the TRICE system is accomplished by using two flip-flops designated as U and W. These flip-flops assume any one of four configurations to signify a specific input device as follows:

$\overline{U}\,\overline{W}$ = keyboard

$U\overline{W}$ = reader

UW = computer

$\overline{U}W$ = patchboard

Logic equations to control the status of the U and W flip-flops are as follows:

U

$u = LpV\ell + LpU\ell + GpBc4 + GpBc5$

$ou = Gp\,(Bc3+Bc6) + \textcircled{T}$

W

$w = Gp\,(Bc5+Bc6)$

$ow = Gp\,(Bc3+Bc4) + Lp\,(U\ell + T\ell) + \textcircled{T}$

The $\textcircled{T}$ signal is generated by the keyboard and permits the keyboard to assume control at any time. The Lp signal is generated during latter half of each word time when the TRICE is in a PATCHBOARD control mode. ($Lp = \overline{U}WT5$). The $T\ell$, $U\ell$ and $V\ell$ signals are generated on the patchboard. These signals permit the control mode to be transferred from the PATCHBOARD to one of the other input devices. The $V\ell$ signal permits the U flip-flop to be set and thus transfer the control mode to the computer. The $U\ell$ signal permits the U flip-flop to be set and the W flip-flop to be reset and thus transfer control to the reader. The $T\ell$ signal permits control to be transferred to keyboard by resetting the W flip-flop.

The Gp signal is generated during non-patchboard modes. The logic equation for generating the Gp signal is as follows:

$$Gp = Bp\ (B6B5Po + B6\overline{B5}Pe)$$

The Po signal is true if an odd number of true bits are contained within the first four bits of the character being processed and Pe is true if the character contains an even number of true bits.

The Bp signal is generated by a logic gate only during non-patchboard control modes and is controlled by the following logic equation:

$$Bp = \overline{W}\ Cp + UW\ Cpg$$

The $\overline{W}$ signal is true only during keyboard or reader control modes and the U and W terms are true only during computer control mode. The Cpg signal is a timing signal generated by the computer and the Cp signal is a timing signal generated by a flip-flop within the TRICE during keyboard or reader operations.

$$cp = \overline{Cp}\ T5\ (Kb\ \overline{Cb}\ \overline{U} + \overline{Rb}\ U\overline{W} + \overline{Rb}\ P\ A4\ \overline{Kb}$$

Cp

$$ocp = Cp\ T5$$

The T5 signal permits the Cp flip-flop to be true for one word time as defined by the interval between two successive T5 pulses. The Kb signal indicates that the keyboard has been activated. The $U\overline{W}$ term indicate that from the reader and $\overline{Rb}$ indicates that the reader is ready to read a character. The $\overline{Cb}$ signal is comparable to the $\overline{Rb}$ signal and indicates that the keyboard is ready to generate another character. The $\overline{Rb}$ and $\overline{Cb}$ signals function as electrical interlocks by preventing a second character from being accepted until the previous character

has been properly processed. These terms also prevent a single character from being processed more than once.

Figure 3-4 illustrates the relationship between the various signals when control codes are received from the keyboard. Logic equations for generating Kc, Kb, Cp and Cb signals are as follows:

Kb

$$kb = \overline{Kb}\ (C2)\ (Ct)$$

$$okb = Kb\ Kc$$

$$Kc = (K1) + (K2) + (K3) + (K4) + (K5) + (K6)$$

Cp

$$cp = \overline{Cp}\ T5\ (Kb\ \overline{Cb}\ U + \overline{Rb}\ \overline{U}\ W + \overline{Rb}\ P\ A4\ \overline{Kb})$$

$$ocp = Cp\ T5$$

Cb

$$cb = \overline{Cb}\ T5\ Cp$$

$$ocb = Cb\ T5\ \overline{Kb}$$

The Bc3 through Bc6 signals which appear in the logic equations of the U and W flip-flops are generated automatically as a function of the data being received from the keyboard, reader or computer.

In the following equations, L1 through L5 are signals from the computer, R1 through R6 are signals from the paper tape reader and (K1) through (K6) are signals from the keyboard.

$$B1 = \overline{U}\ \overline{W}\ (K1) + U\ \overline{W}\ R1 + U\ W\ L1$$

$$B2 = \overline{U}\ \overline{W}\ (K2) + U\ \overline{W}\ R2 + U\ W\ L2$$

$$B3 = \overline{U}\ \overline{W}\ (K3) + U\ \overline{W}\ R3 + U\ W\ L3$$

$$B4 = \overline{U}\ \overline{W}\ (K4) + U\ \overline{W}\ R4 + U\ W\ L4$$

$$B5 = \overline{U}\ \overline{W}\ (K5) + U\ \overline{W}\ R5 + U\ W\ L5$$

$$B6 = \overline{U}\ \overline{W}\ (K6) + U\ \overline{W}\ R6 + U\ W$$

$$Bc0 = \overline{B4}\ \overline{B3}\ \overline{B2}\ \overline{B1}$$

$$Bc1 = \overline{B4}\ \overline{B3}\ \overline{B2}\ B1$$

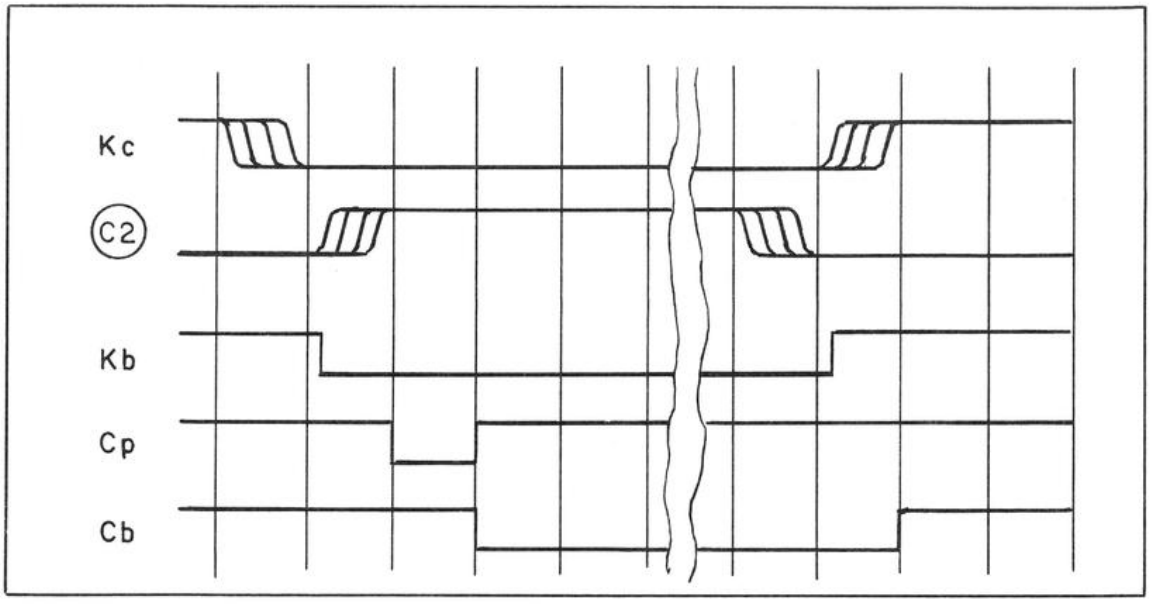

FIGURE 3-4. CONTROL CODES FROM KEYBOARD

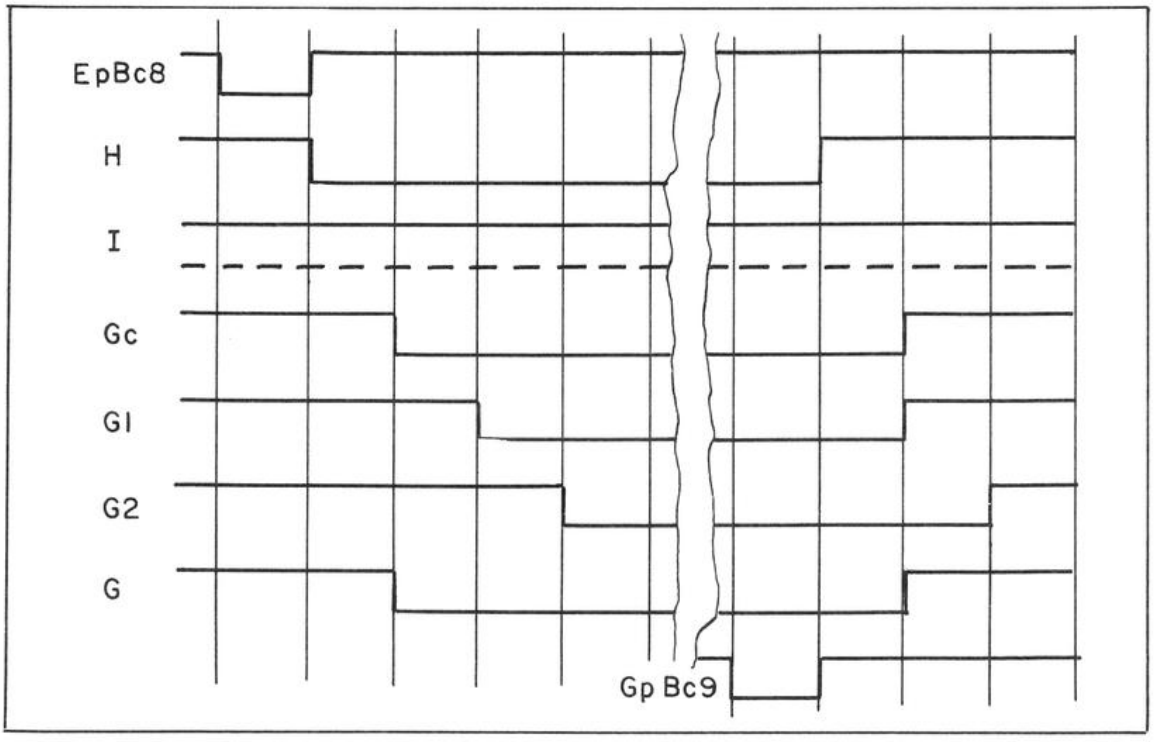

FIGURE 3-5. COMPUTE OFF TO HALT— HALT TO COMPUTE OFF

$$Bc2 = \overline{B4}\ \overline{B3}\ B2\ \overline{B1}$$

$$Bc3 = \overline{B4}\ \overline{B3}\ B2\ B1$$

$$Bc4 = \overline{B4}\ B3\ \overline{B2}\ \overline{B1}$$

$$Bc5 = \overline{B4}\ B3\ \overline{B2}\ B1$$

$$Bc6 = \overline{B4}\ B3\ B2\ \overline{B1}$$

$$Bc7 = \overline{B4}\ B3\ B2\ B1$$

$$Bc8 = B4\ \overline{B3}\ \overline{B2}\ \overline{B1}$$

$$Bc9 = B4\ \overline{B3}\ \overline{B2}\ B1$$

The preceding equations indicate how the various signals received from the paper tape reader, computer or keyboard are automatically converted into B1 through B6 signals. The B1 through B4 signals, in turn, are converted into Bc0 through Bc9 signals.

As shown in the equations for the U and W flip-flops, the Bc3 signal causes the U and W flip-flops to be reset. This condition places the TRICE system into the KEYBOARD control mode. A Bc4 signal turns on flip-flop U and resets flip-flop W and the TRICE system is in the READER control mode. A Bc5 signal places the TRICE system in to the COMPUTER control mode by turning on both flip-flops. A Bc6 signal resets the U flip-flop and turns on the W flip-flop to place the TRICE into a PATCHBOARD control mode.

The Bc1 through Bc9 signals are continuously monitored to determine whether an even or odd number of true bits are present within the B1 through B4 signals. Logic equations to perform this function are as follows:

$$Pe = Bc3 + Bc5 + Bc6 + Bc9$$

$$Po = Bc1 + Bc2 + Bc4 + Bc7 + Bc8$$

Table 3-3 lists the correlation which exists between the signals generated by the paper tape reader, keyboard and the computer to

Table 3-3. (Sheet 1 of 2)

CONTROL CODES

6 Bit Code	(PTU) 5 Bit Code	Tape Code	Typewriter Code	Keyboard Name	Logic			Patchboard Input
					Code	Clock	State	
00		·			Bc0			
01		· ●	1	1	Bc1	Dp		
02		· ●	2	2	Bc2	Dp		
03		· ●●	L	REGISTER LENGTH	Bc3	Fp		
04		·●	4	4	Bc4	Dp		
05		·● ●	N	CONVERT INPUT	Bc5	Fp		
06		·●●	O	CONVERT OUTPUT	Bc6	Fp		
07		·●●●	7	7	Bc7	Dp		
10		●·	8	8	Bc8	Dp		
11		●· ●	R		Bc9	Fp		
12		●· ●						
13		●· ●●	STOP					
14		●·●						
15		●·● ●						
16		●·●●						
17		●·●●●						
20		● ·	SPACE	DATA	Bc0	Fp	$\overline{A}\,\overline{D}$	
21		● · ●	J	DECIMAL EXPONENT	Bc1	Fp		
22		● · ●	K	SCALING EXPONENT	Bc2	Fp		
23		● · ●●	3	3	Bc3	Dp		
24		● ·●	M		Bc4	Fp		
25		● ·● ●	5	5	Bc5	Dp		
26		● ·●●	6	6	Bc6	Dp		
27		● ·●●●	P	PUNCH OUTPUT	Bc7	Fp	A D	
30		●●·	Q		Bc8	Fp		
31		●●· ●	9	9	Bc9	Dp		
32		●●· ●						
33		●●· ●●						
34		●●·●						
35		●●·● ●						
36		●●·●●	+	+	$\overline{B}1$	Sp		
37		●●·●●●	-	-	B1	Sp		

Table 3-3. (Sheet 2 of 2)

CONTROL CODES

6-Bit Code	(PTU) 5-Bit Code	Tape Code	Typewriter Code	Keyboard Name	Logic			Patchboard Input
					Code	Clock	State	
40	00	● ·	O	O	Bc0	Dp		
41	01	● · ●	A	ADDRESS	Bc1	Ep	A $\overline{D}$	
42	02	● · ●	B		Bc2	Ep		
43	03	● · ●●	T	KEYBOARD	Bc3	Gp	$\overline{U}$ $\overline{W}$	K
44	04	● ·●	D	DISPLAY	Bc4	Ep	$\overline{A}$ D	
45	05	● ·● ●	V	COMPUTER	Bc5	Gp	U W	C
46	06	● ·●●	W	PATCHBOARD	Bc6	Gp	$\overline{U}$ W	
47	07	● ·●●●	G	INTEGRATE	Bc7	Ep	H I	I
50	10	● ●·	H	HALT	Bc8	Ep	H $\overline{I}$	H
51	11	● ●· ●	Z	COMPUTE OFF	Bc9	Gp	$\overline{H}$ $\overline{I}$	CO
52	12	● ●· ●						
53	13	● ●· ●●	.					
54	14	● ●·●						
55	15	● ●·● ●						
56	16	● ●·●●	C/R					
57	17	● ●·●●●						
60	20	●● ·	,		Bc0			
61	21	●● · ●	$		Bc1	Gp		
62	22	●● · ●	S	INTEGRATE SLOW	Bc2	Gp	S	
63	23	●● · ●●	C	SINGLE CYCLE	Bc3	Ep	(C)	SC
64	24	●● ·●	U	READER	Bc4	Gp	U $\overline{W}$	R
65	25	●● ·● ●	E	READ	Bc5	Ep	(So)	
66	26	●● ·●●	F	FILL	Bc6	Ep	(Si)	
67	27	●● ·●●o	X	SELECTED RESET	Bc7	Gp	(Rsc)	
70	30	●●●·	Y	PATCHED RESET	Bc8	Gp	(Rpc)	PR
71	31	●●●· ●	I	RESET	Bc9	Ep	$\overline{HI}$,(Rtc)	RT
72	32	●●●· ●	U/C					
73	33	●●●· ●●	,					
74	34	●●●·●	L/C					
75	35	●●●·● ●						
76	36	●●●·●●	TAB					
77	37	●●●·●●●	DELETE					

Table 3-4.

PATCHBOARD CONTROL LINES

Inputs			Outputs			Inputs	
I	Integrate	TRICE Computing Modes	OP	Operate	Analog Computer Modes	0	Sense Lines (PB250 TES)
H	Halt		HO	Hold		1	
RT	Reset		IC	Initial Condition		2	
CO	Compute Off		PS	Pot Set		3	
K	Keyboard	TRICE Control Modes	Ofa	Overflow Analog		4	
R	Reader		Ofm	TRICE or Converter		5	
C	Computer		Ofc	Converter		6	
PR	Patched Reset		Oft	TRICE		7	
SC	Single Cycle		Of1	TRICE Block 1		10	
XO	Not Used		Of2	Block 2		11	
X1			Of3	Block 3		12	
X2			Of4	Block 4		13	
X3			Of5	Block 5		14	
X4			Of6	Block 6		15	
X5			Of7	Block 7		16	
X6			Of8	Block 8		17	

control the TRICE. Table 3-4 lists the input and output control line of the patchboard.

C-2b. Selection of a Basic Compute Mode

TRICE modules internally can have two states; the compute on condition, in which increments can be received and generated, and the compute off condition, when computation in the module is disabled. In a normal problem setup all increments originate from the independent variable input from the patchboard (lines Te and Ts). These lines are connected to the dx input of the integrators integrating for the independent variable. Before the start of a computing run the initial values contained in the I registers of the modules are inserted into the Y registers by the reset operation. To allow more flexible programming the reset operation can be performed in three selective ways.

1) All modules are reset in the total (normal) reset operation.
2) Only the modules which have their patched reset input connected to the patched reset bus (on the patchboard) are reset in the patched reset operation.
3) Each module can be individually selected by the address selection logic and reset in the selected reset operation.

Flip-flops H and I are used to control the selection of INTEGATE, HALT, RESET or COMPUTE OFF compute modes. The significance of the four different configurations is as follows:

$H\,I$ = INTEGRATE
$H\,\overline{I}$ = HALT
$\overline{H}\,I$ = RESET
$\overline{H}\,\overline{I}$ = COMPUTE OFF

Logic equations to control the status of the H and I flip-flops are as follows:

H

$$h = Lp\ (H\ell + G\ell) + Ep\ (Bc7 + Bc8)$$

$$oh = Lp\ (Z\ell + I\ell) + Bc9\ (Ep + Gp)$$

I

$$i = Lp\ (G\ell + I\ell) + Ep\ (Bc7 + Bc9)$$

$$oi = Lp\ (H\ell + Z\ell) + Ep\ Bc8 + Gp\ Bc9$$

During PATCHBOARD control mode, the Lp signal is true during the latter portion of each word time. The coincidence of a $G\ell$ signal with the Lp signal sets flip-flops H and I. The TRICE system is set to the INTEGRATE compute mode. The coincidence of an $H\ell$ signal with the Lp signal sets flip-flop H and resets flip-flop I. $H\overline{I}$ defines the HALT compute mode. The coincidence of an $I\ell$ signal with the Lp signal resets flip-flop H and sets flip-flop I. $\overline{H}\,I$ defines the RESET compute mode. The coincidence of a $Z\ell$ signal with the Lp signal resets both flip-flops. When both flip-flops H and I are off, the TRICE system is in the COMPUTE OFF compute mode.

The equations which contain the Bc7 through Bc9 terms permit the H and I flip-flops to be set accordingly with information received from the keyboard, paper tape reader or computer, as described previously. The Gp term has been defined under control modes. The Ep term is defined by the following logic equation:

$$Ep = Bp\ (B6\ \overline{B5}\ Po + B6\ B5\ Pe)$$

Thus, the Ep signal is generated if there is an even number of true bits within the character received from the keyboard, reader or computer. Whereas, the Gp signal is generated if there is an odd number of true bits.

A coincidence of an Ep signal with a Bc7 signal sets flip-flops H and I to the INTEGRATE compute mode. A coincidence of an Ep signal with a Bc8 signal set flip-flop H and resets flip-flop I to the HALT compute mode. A coincidence of an Ep signal with a Bc9 signal resets flip-flop H and sets flip-flop I to the RESET compute mode and the coincidence of a Gp signal with a Bc9 resets both flip-flops to the COMPUTE OFF compute mode.

C-2c. Selection of a Special Computing Mode

The four basic computing modes described in the previous paragraph may be modified to permit more flexible programming. A SELECTED RESET computing mode causes only an addressed module to be reset and a PATCHED RESET computing mode causes only the modules which are properly wired via patchboard to be reset. The RESET computing mode causes all TRICE modules to be reset. The special reset modes are executed within any basic computing mode. A SINGLE CYCLE and INTEGRATE SLOW compute mode may be executed only during the basic HALT compute mode.

The various reset modes are controlled by the following flip-flops and logic equations:

Rsc

$$rsc = \overline{Rsc}\ Gp\ Bc7$$

$$orsc = Rsc\ (G2\ R)$$

Rpc

$$rpc = \overline{Rpc}\ Gp\ Bc8 + \overline{R}\ Lp\ Y\ell$$

$$orpc = Rpc\ (G2\ R)$$

Rtc

$$rtc = \overline{Rtc}\ Ep\ Bc9 + \overline{R}\ Lp\ I\ \ell$$

$$ortc = Rtc\ (G2\ R)$$

R

$$r = \overline{R}\ T5\ \overline{G1}\ (Rsc + Rpc + Rtc)$$

$$or = R\ T5\ \overline{G1}$$

$Rs = Rsc\ R$

$Rp = Rpc\ R$

$Rt = Rtc\ R$

The preceding equations indicate that the Rsc flip-flop (selected reset) is set only by a control code Bc7 Gp received from the keyboard, paper tape reader or computer. The Rpc flip-flop (patched reset) is set by a control code Bc8 Gp received from the keyboard, paper tape reader or computer and by a $Y\ell$ signal from the patchboard. The Rtc flip-flop (total reset) is set by a control code Bc9 Ep received from keyboard, reader, or computer and an $I\ell$ signal received from the patchboard. The R flip-flop is set whenever any one of the above mentioned flip-flops is set. The preceeding equations also indicate that an Rs, Rp or Rt signal is generated whenever a coincidence occurs between the R flip-flop being on and the Rsc, Rpc or Rtc flip-flops respectively, being on.

In addition to the timing signals of Gp and Ep, which have been described previously, G1 and G2 are timing signals generated by the G1 and G2 flip-flops.

Logic equations for the G1 and G2 flip-flops are as follows:

G1

$g1 = \overline{G1}\ \overline{R} + \overline{G1}\ T5\ H\ Gc$

$og1 = G1\ T5\ \overline{H}\ G2 + G1\ T5\ G2\ (Rsc + Rpc + Rtc)$

G2

$g2 = \overline{G2}\ T5\ G1$

$og2 = G2\ T5\ \overline{G1}$

Timing signals Gc and G are generated by the following equations:

Gc

$gc = \overline{Gc}\ T5\ H$

$ogc = Gc\ T5\ \overline{H}$

$G = Gc\ \overline{R}$

The relationship between the various timing signals is illustrated on Figure 3-5 through 3-8. Figure 3-6 illustrates that a Te signal becomes true during an INTEGRATE mode. The logic equations for controlling the Te signal are as follows:

Te

$$te = \overline{Te}\ T5\ C + \overline{Te}\ T5\ H\ I$$

$$ote = Te\ T5\ (\overline{H} + \overline{I})$$

In the preceding equations the H and I terms define the INTEGRATE mode and $\overline{H} + \overline{I}$ define non-INTEGRATE modes. The C term is true only during a SINGLE CYCLE or INTEGRATE SLOW mode and is described further in subsequent paragraphs.

Logic equations for the S and C flip-flops which control the SINGLE CYCLE and INTEGRATE SLOW modes are as follows:

S

$$s = \overline{S}\ Gp\ Bc2$$

$$os = S\ T5\ \overline{H} + Ep\ Bc8$$

C

$$c = \overline{C}\ Lp\ C\ell + Ep\ Bc3 + Sr\ S$$

$$oc = C\ T5\ Te$$

In the preceding equations, the Sr signal is obtained from a free running multivibrator having a frequency of 100 cps.

The S flip-flop may be turned on with a control code Bc2 Gp and turned off at the fall of T5 during TOTAL RESET or COMPUTE OFF modes as defined by the $\overline{H}$ signal or by a control code Bc8 Ep.

The C flip-flop may be turned on by a $C\ell$ signal from the patchboard; a control code Bc3 Ep from the keyboard, reader or computer; or by the coincidence of an Sr and S signal. In all cases, the C flip-flop is automatically turned off by the coincidence of the Te and T5 signal. The Te signal is true during any INTEGRATE mode. Figures 3-9 and

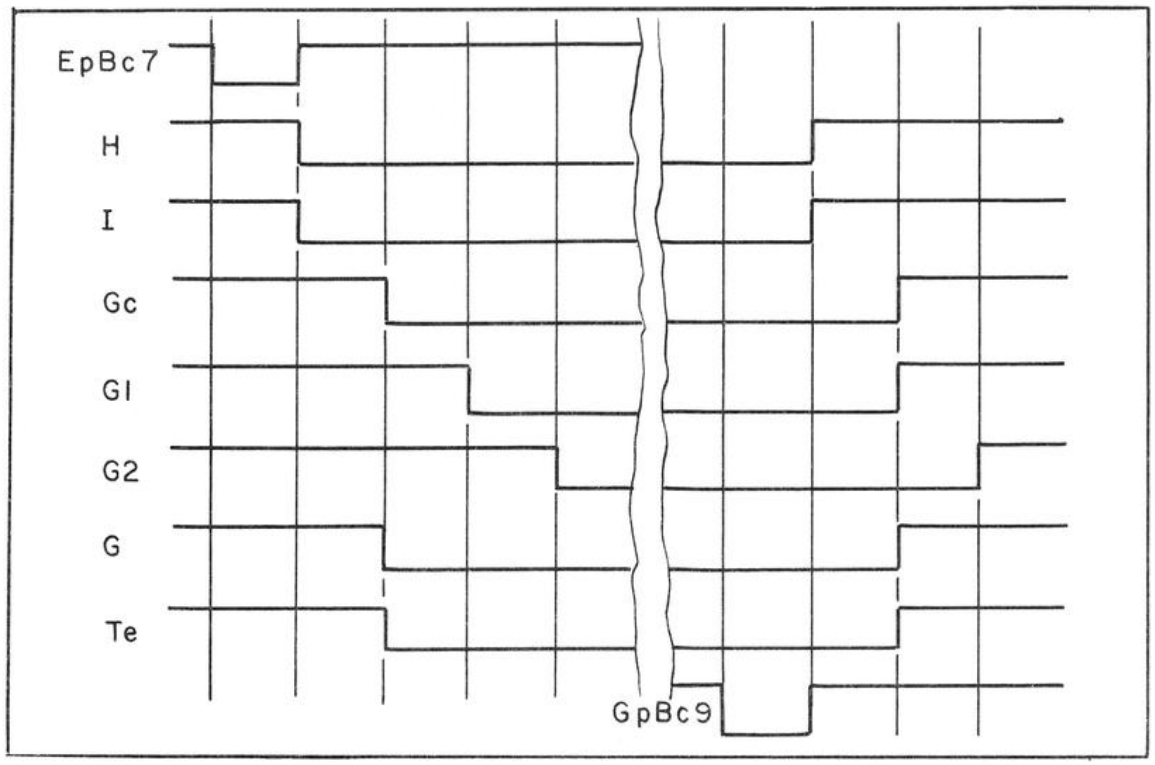

FIGURE 3-6. COMPUTE OFF TO INTEGRATE – INTEGRATE TO COMPUTE OFF

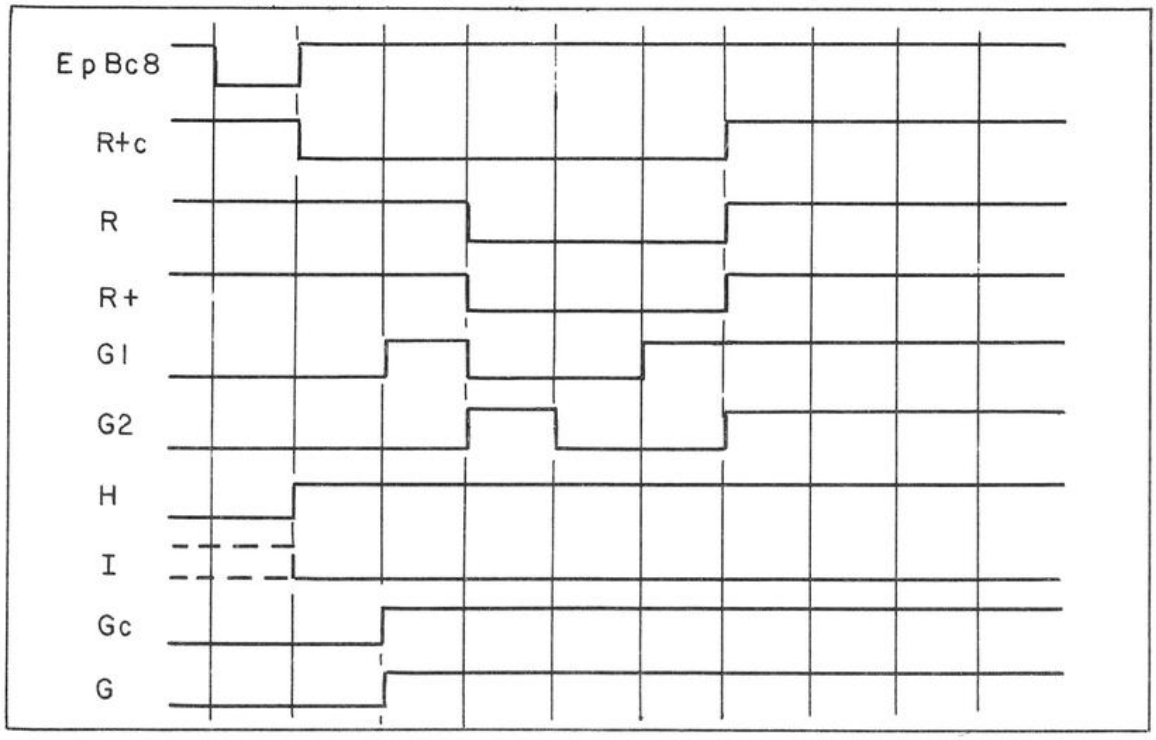

FIGURE 3-7. HALT ($H\bar{I}$) OR INTEGRATE (HI) TO RESET

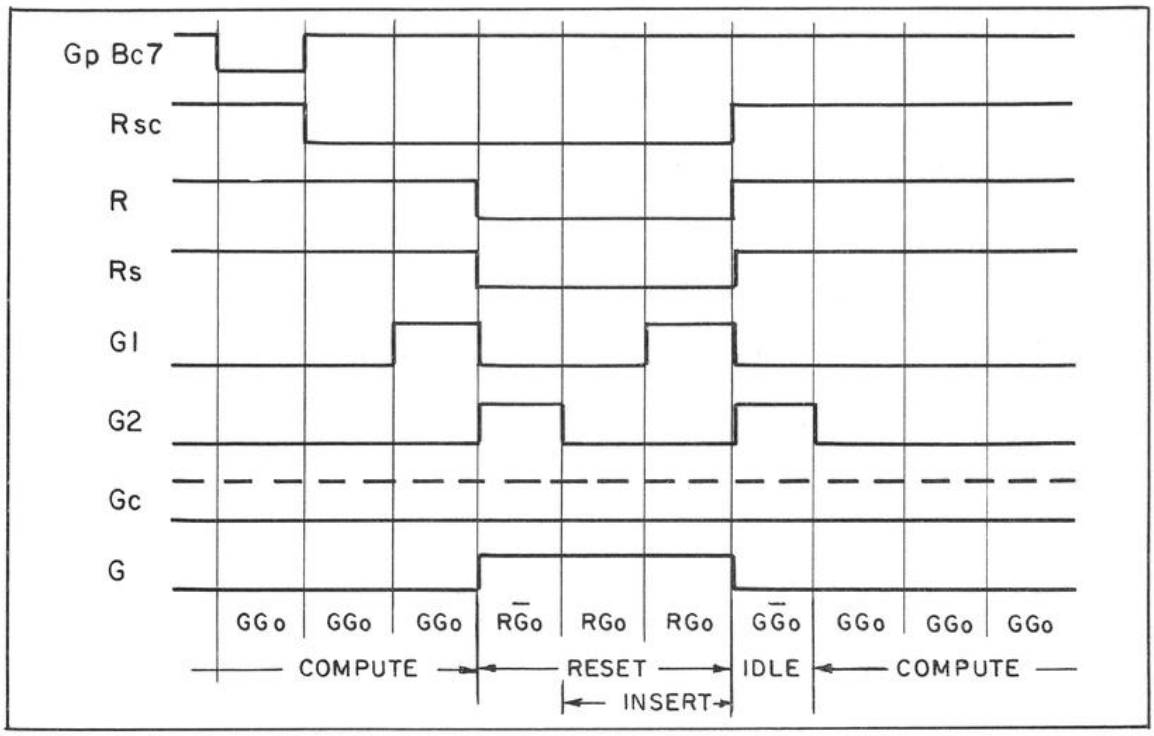

FIGURE 3-8. INTEGRATE OR HALT TO SELECTED RESET TO INTEGRATE OR HALT

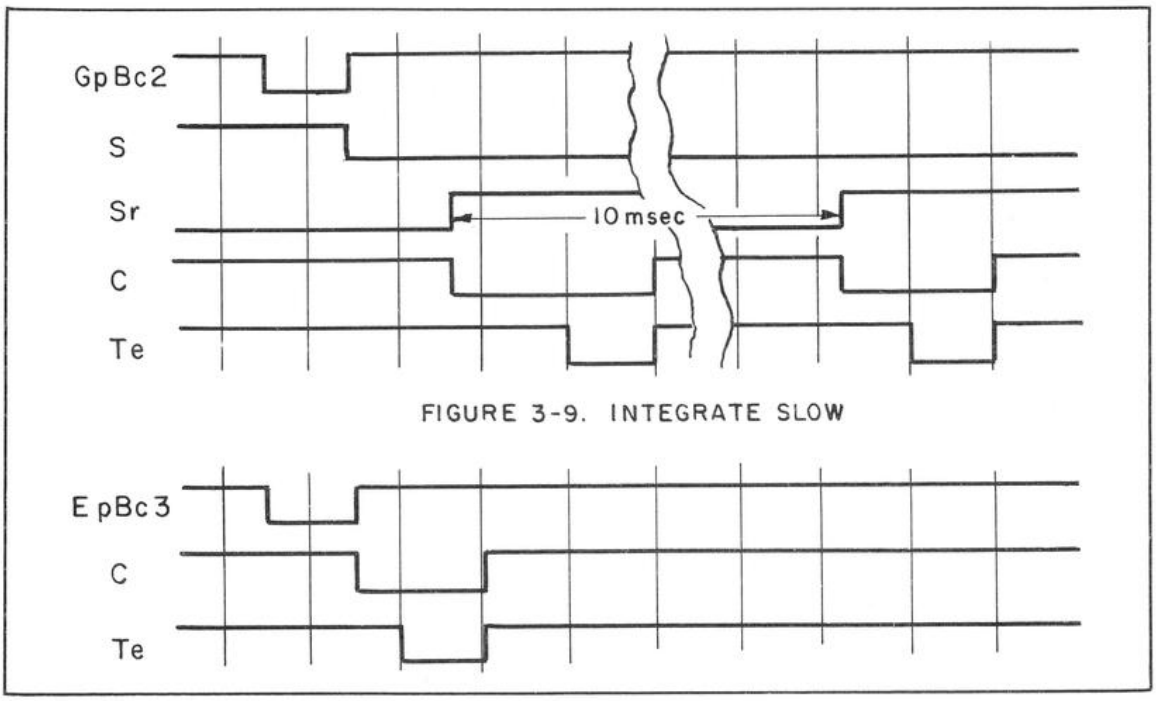

FIGURE 3-9. INTEGRATE SLOW

FIGURE 3-10. SINGLE CYCLE

3-10 illustrate the relative timing of the various signals when S and C signals are generated.

C-2d. Selection of Input/Output Mode

The selection of ADDRESS, DATA, DISPLAY or PUNCH OUTPUT modes is controlled by flip-flops A and D. The configuration of these two flip-flops indicate the different input/output modes as follows:

A D = PUNCH OUTPUT
A $\overline{D}$ = ADDRESS
$\overline{A}$ D = DISPLAY
$\overline{A}$ $\overline{D}$ = DATA

The ADDRESS mode is selected when the address in the binary display is to be changed. The DATA mode is selected when the information in the binary display register or the decimal display register is to be changed. The DISPLAY mode permits the contents of the addressed module to be read at the rate of 100 cps and displayed in the binary display register and the decimal display register. During PUNCH OUTPUT mode, the contents of the decimal display register is punched on paper tape.

Logic equations for controlling the A and D flip-flops are as follows:

A
$a = \overline{A}\ Ep\ Bc1 + Fp\ Bc7$
$oa = A\ Ep\ Bc4 + Fp\ Bc0$

D
$d = \overline{D}\ Ep\ Bc4 + Fp\ Bc7$
$od = D\ Ep\ Bc1 + Fp\ Bc0$

Logic equations for the Ep and Bc1 through Bc7 control codes have been given previously. Logic equations for the Fp signal are as follows:

$Fp = B_p\ (\overline{B6}\ B5\ Po + \overline{B6}\ \overline{B5}\ Pe + \overline{B6}\ B5\ Bc0)$

During an ADDRESS mode (A $\overline{D}$), an address register comprised of nine flip-flops, Ra1 through Ra9, is loaded by the character input. Complete logic equations for theseflip-flops are as follows:

Ra1

$$ra1 = \overline{Ra1}\ C\ell a\ Gdg + Spa\ B1$$

$$ora1 = Ra1\ C\ell a\ \overline{Gdg} + Spa\ \overline{B1}$$

Ra2

$$ra2 = \overline{Ra2}\ C\ell a\ Ra1 + Ab\ Dpa\ B3$$

$$ora2 = Ra2\ C\ell a\ \overline{Ra1} + Spa$$

Ra3

$$ra3 = \overline{Ra3}\ C\ell a\ Ra2 + Ab\ Dpd\ B2$$

$$ora3 = Ra3\ C\ell a\ \overline{Ra2} + Spa$$

Ra4

$$ra4 = \overline{Ra4}\ C\ell a\ Ra3 + Ab\ Dpa\ B1$$

$$ora4 = Ra4\ C\ell a\ \overline{Ra3} + Spa$$

Ra5

$$ra5 = \overline{Ra5}\ C\ell a\ Ra4 + At\ Dpa\ B1$$

$$ora5 = Ra5\ C\ell a\ \overline{Ra4} + Spa$$

Ra6

$$ra6 = \overline{Ra6}\ C\ell a\ Ra5 + Au\ Dpa\ B3$$

$$ora6 = Ra6\ C\ell a\ \overline{Ra5} + Spa$$

Ra7

$$ra7 = \overline{Ra7}\ C\ell a\ Ra6 + Au\ Dpa\ B2$$

$$ora7 = Ra7\ C\ell a\ \overline{Ra6} + Spa$$

Ra8

$$ra8 = \overline{Ra8}\ C\ell a\ Ra7 + Au\ Dpa\ B1$$

$$ora8 = Ra8\ C\ell a\ \overline{Ra7} + Spa$$

Ra9

$$ra9 = \overline{Ra9}\ C\ell a\ Ra8 + (\overline{Ab}\ \overline{At}\ \overline{Au})\ Dpa\ B1$$

$$ora9 = Ra9\ C\ell a\ \overline{Ra8} + (\overline{Ab}\ \overline{At}\ \overline{Au})\ Dpa\ \overline{B1}$$

The equations containing a Cℓ a term permit the Ra1 through Ra9 flip-flops to be a shift register. Information is obtained from Gdg and shifted into Ra1 and then to the other flip-flops in a sequential manner. These equations are used when working with PB250 as described in subsequent paragraphs.

Logic equations for generating Sp, Spa, Dp, Dpa, Ab, At and Au are as follows:

$$Sp = Bp\ \overline{B6}\ B5\ B4\ B3\ B2$$

$$Dp = Bp\ (\overline{B6}\ \overline{B5}\ Po + \overline{B6}\ B5\ Pe + B6\ B5\ Bc0)$$

$$Spa = Sp\ (A\overline{D})$$

$$Dpa = Dp\ (A\overline{D})$$

$$ab = \overline{Ab}\ Spa$$

Ab

$$oab = Ab\ Dpa$$

$$at = \overline{At}\ Dpa\ Ab$$

At

$$oat = At\ Dpa + Spa$$

$$au = \overline{Au}\ Dpa\ At$$

Au

$$oau = Au\ Dpa + Spa$$

The Sp signal is true when a sign character is being processed and the Dp signal is true when a digit character is being processed.

The proceding equations for the Ra1 through Ra9 flip-flops control the following sequence of operations:

1. A plus or minus sign causes an Spa signal to be generated.
2. The Spa signal allows Ra1 to be set or reset in accordance with the B1 signal received from the control unit. The Spa

signal also resets Ra2 through Ra8 flip-flops and sets flip-flop Ab. Flip-flops At and Au are reset by Spa signals.

3. A character representing a digit causes a Dpa signal to be generated.
4. The Dpa signal in conjunction with the Ab signal permit the B1, B2 and B3 bits to be transferred into the Ra4, Ra3 and Ra2 flip-flops, respectively. The Ab flip-flop is reset and the At flip-flop is set by the Dpa and Ab combination.
5. The second Dpa signal is generated when the second digit character input is received from the control unit. The Dpa signal in conjunction with the At signal set Ra5 if B1 is true. If B1 is false, Ra5 remain reset. The At Dpa signal resets flip-flop At and sets flip-flop Au.
6. The third Dpa signal is generated when the third digit character input is received from the control unit. This Dpa signal in conjunction with the Au signal set Ra8, Ra7 and Ra6 in accordance with B1, B2 and B3 bits, respectively. The third Dpa signal and Au signal also reset the Au flip-flop.
7. The fourth Dpa signal is generated when the fourth character input is received. At this time, the Ab, At and Au flip-flops are all reset and the Ra9 flip-flop will be set or reset in accordance to the B1 bit.

The contents of the address register contains four fields of information. If the Ra1 flip-flop is off, the address designates a TRICE module and if the Ra1 flip-flop is on, the address designates a converter. Ra2, Ra3 and Ra4 flip-flops contain the block address of he TRICE module or converter. Ra5 through Ra8 flip-flops contain the unit address of the TRICE module or converter in the octal system. The status of the Ra9 flip-flop is only applicable when a TRICE module is

addressed. If Ra9 is false the Y register of the module is addressed and if Ra9 is true the I register is addressed.

Figure 3-11 is a simplified block and logic diagram illustrating the loading of the address register. Table 3-5 lists the various configurations and significance of the address register.

Logic equations for converting the contents of the Ra2 through Ra4 flip-flops into the appropriate $\overline{B}$ signals are as follow:

$$\overline{B1} = Ra2 + Ra3 + \overline{Ra4}$$
$$\overline{B2} = Ra2 + \overline{Ra3} + Ra4$$
$$\overline{B3} = Ra2 + \overline{Ra3} + \overline{Ra4}$$
$$\overline{B4} = \overline{Ra2} + Ra3 + Ra4$$
$$\overline{B5} = \overline{Ra2} + Ra3 + \overline{Ra4}$$
$$\overline{B6} = \overline{Ra2} + \overline{Ra3} + Ra4$$
$$\overline{B7} = \overline{Ra2} + \overline{Ra3} + \overline{Ra4}$$
$$\overline{B8} = Ra2 + Ra3 + Ra4$$

Logic equations for converting the contents of the Ra5 through Ra8 flip-flops into the appropriate U signals (U00 through $U17_8$) are as follows:

$$\overline{U0} = Ra5 + Ra6 + Ra7 + Ra8$$
$$\overline{U1} = Ra5 + Ra6 + Ra7 + \overline{Ra8}$$
$$\overline{U2} = Ra5 + Ra6 + \overline{Ra7} + Ra8$$
$$\overline{U3} = Ra5 + Ra6 + \overline{Ra7} + \overline{Ra8}$$
$$\overline{U4} = Ra5 + \overline{Ra6} + Ra7 + Ra8$$
$$\overline{U5} = Ra5 + \overline{Ra6} + Ra7 + \overline{Ra8}$$
$$\overline{U6} = Ra5 + \overline{Ra6} + \overline{Ra7} + Ra8$$
$$\overline{U7} = Ra5 + \overline{Ra6} + \overline{Ra7} + \overline{Ra8}$$
$$\overline{U8} = \overline{Ra5} + Ra6 + Ra7 + Ra8$$
$$\overline{U9} = \overline{Ra5} + Ra6 + Ra7 + \overline{Ra8}$$

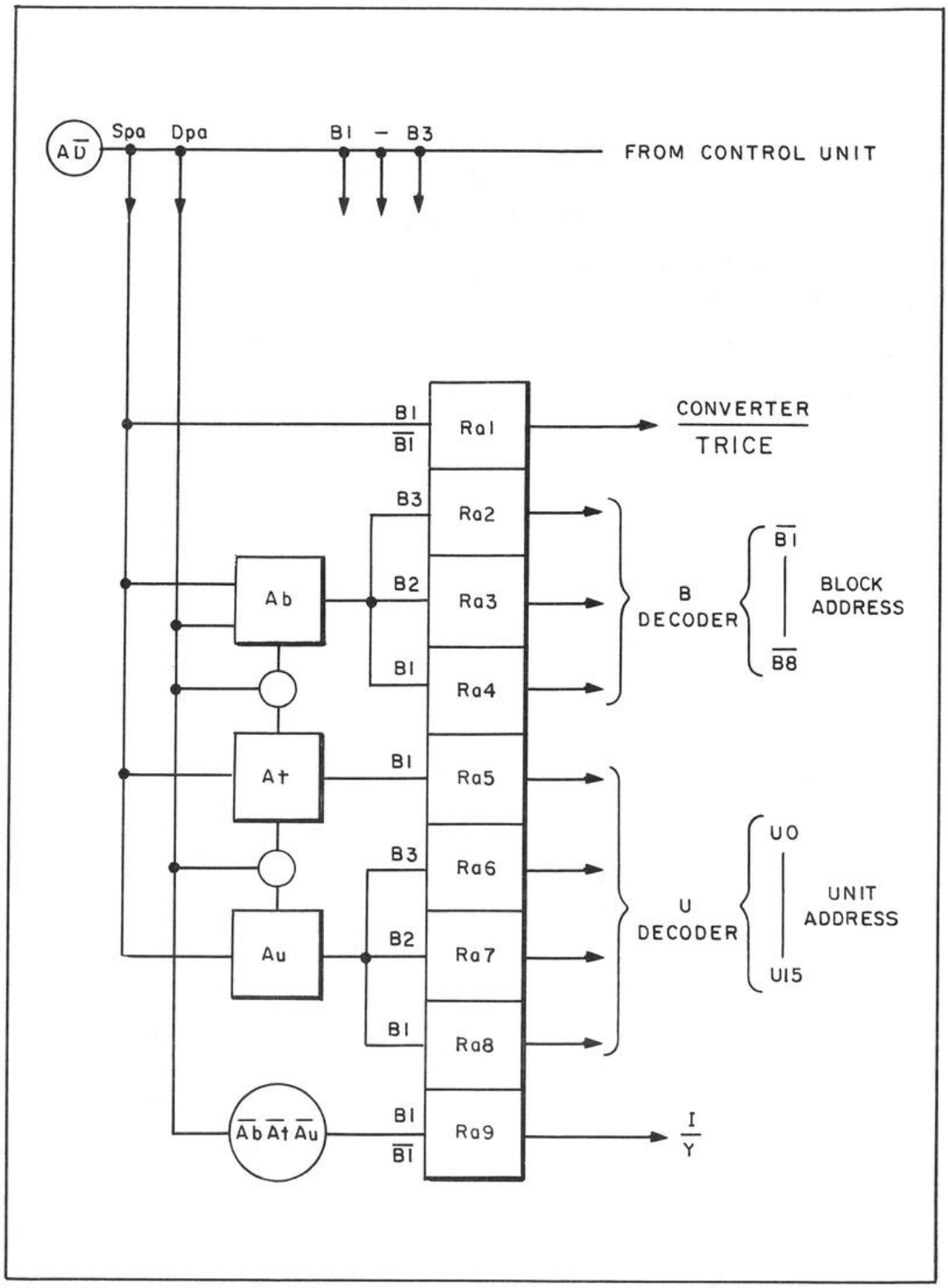

FIGURE 3-11. ADDRESS INPUT CONNECTIONS

Table 3-5. (Sheet 1 of 2)

ADDRESS REGISTER FORMAT

TRICE Modules						
Digit Bit	C 1	B 2 3 4	T 5	U 6 7 8	I 9	Module
	0	0 0 1	0	0 0 0	0	I 100 Y
			0	0 0 0	1	I 100 I
			0	0 0 1	0	I 101 Y
			0	0 0 1	1	I 101 I
			0	0 1 0	0	I 102 Y
			0	0 1 0	1	I 102 I
			0	0 1 1	0	I 103 Y
			0	0 1 1	1	I 103 I
			0	1 0 0	0	I 104 Y
			0	1 0 0	1	I 104 I
			0	1 0 1	0	I 105 Y
			0	1 0 1	1	I 105 I
			0	1 1 0	0	I 106 Y
			0	1 1 0	1	I 106 I
			0	1 1 1	0	I 107 Y
			0	1 1 1	1	I 107 I
			1	0 0 0	0	S 110 Y
			1	0 0 0	1	S 110 I
			1	0 0 1	0	S 111 Y
			1	0 0 1	1	S 111 I
			1	0 1 0	1	CM 112
			1	0 1 1	1	CM 113
			1	1 0 0	0	VM 114-5 X
			1	1 0 0	1	VM 114-5 Ix
			1	1 0 1	0	VM 114-5 Y
			1	1 0 1	1	VM 114-5 Iy
			1	1 1 0	0	VM 116-7 X
			1	1 1 0	1	VM 116-7 Ix
			1	1 1 1	0	VM 116-7 Y
			1	1 1 1	1	VM 116-7 Iy

Table 3-5. (Sheet 2 of 2)

ADDRESS REGISTER FORMAT

Converter Modules

Digit Bit	C 1	B 2 3 4	T 5	U 6 7 8	I 9	Module
	1	0 0 1	0	0 0 0	X	D 100
			0	0 0 1	X	A 101
			0	0 1 0	X	D 102
			0	0 1 1	X	A 103
			0	1 0 0	X	D 104
			0	1 0 1	X	A 105
			0	1 1 0	X	D 106
			0	1 1 1	X	A 107

Block Selection

Digit Bit	C 1	B 2 3 4	T 5	U 6 7 8	I 9	Module Block	
	0	0 0 1				TRICE Block 1	1st Rack
	0	0 1 0				Block 2	
	0	0 1 1				Block 3	2nd Rack
	0	1 0 0				Block 4	
	0	1 0 1				Block 5	3rd Rack
	0	1 1 0				Block 6	
	0	1 1 1				Block 7	4th Rack
	0	0 0 0				Block 8	
	1	0 0 1				Converter Block 1	1st Rack
	1	0 1 0				Block 2	
	1	0 1 1				Block 3	
	1	1 0 0				Block 4	2nd Rack
	1	1 0 1				Block 5	
	1	1 1 0				Block 6	
	1	1 1 1				Block 7	3rd Rack
	1	0 0 0				Block 8	

$$\overline{U10} = \overline{Ra5} + Ra6 + \overline{Ra7} + Ra8$$

$$\overline{U11} = \overline{Ra5} + Ra6 + \overline{Ra7} + \overline{Ra8}$$

$$\overline{U12} = \overline{Ra5} + \overline{Ra6} + Ra7 + Ra8$$

$$\overline{U13} = \overline{Ra5} + \overline{Ra6} + Ra7 + \overline{Ra8}$$

$$\overline{U14} = \overline{Ra5} + \overline{Ra6} + \overline{Ra7} + Ra8$$

$$\overline{U15} = \overline{Ra5} + \overline{Ra6} + \overline{Ra7} + \overline{Ra8}$$

The DATA mode ($\overline{A}\ \overline{D}$) is used to enter new data into the binary data buffer and decimal converter scaler which is to be transferred into the selected TRICE module or converter from the keyboard or paper tape reader as specified by the address register. The DATA mode permits the various registers within the TRICE to be loaded with the proper information prior to the execution of a fill operation. Information received from the keyboard or paper tape reader is processed through flip-flops Db1 through Db4 prior to be transferred into the binary data buffer and decimal converter scaler. Logic equations for the Db1 through Db4 flip-flops are as follows:

$$db1 = Dpd\ B1$$

Db1

$$odb1 = Db1\ Mc + \overline{Dpd}$$

$$db2 = \overline{Db2}\ Mc\ Db1 + Dpd\ B2$$

Db2

$$odb2 = Db2\ Mc\ \overline{Db1} + \overline{Dpd}$$

$$db3 = \overline{Db3}\ Mc\ Db2 + Dpd\ B3$$

Db3

$$odb3 = Db3\ Mc\ \overline{Db2} + \overline{Dpd}$$

$$db4 = \overline{Db4}\ Mc\ Db3 + Dpd\ B4$$

Db4

$$odb4 = Db4\ Mc\ \overline{Db3} + \overline{Dpd}$$

In the preceding equations, the $\overline{Dpd}$ signal in the reset side of the flip-flops causes all of the flip-flops to be reset at the leading edge

of the Dpd signal. The Dpd signal in conjunction with the appropriate B signal (B1 through B4) from the keyboard or papertape reader set the Db1 through Db4 flip-flops at the trailing edge of the Dpd signal. Logic equations for generating a Dpd signal are as follows:

$$Dpd = Dp\ \overline{A}\ \overline{D}$$

$$Dp = Bp\ (\overline{B6}\ \overline{B5}\ Po + \overline{B6}\ B5\ Pe + B6\ \overline{B5}\ Bc0)$$

The equations containing an Mc signal are used when the information within the Db1 through Db4 flip-flops is to be shifted in a serial manner from Db1 toward Db4 flip-flops. Logic equations for generating the Mc signal and associated timing and control signals for the shift operation are as follows:

Mc = Md T5 1 T 52

T51

t51 = $\overline{T51}$ T5

ot51 = T51 T5

T52

t52 = $\overline{T52}$ T51

ot52 = T52 T51

Mc1

mc1 = $\overline{Mc1}$ Mc

omc1 = Mc1 Mc + $\overline{Dpd}$

Mc2

mc2 = $\overline{Mc2}$ Mc1

omc2 = Mc2 Mc1 + $\overline{Dpd}$

Md

md = $\overline{Md}$ Dpd

omd = Md Mc2

Figure 3-12 is a timing chart of the various signals generated during the shift operation. Flip-flops T51 and T52 form a modulo 4 counter which is advanced by T5 signals. A Dpd signal may be generated at any time by the character input. Flip-flop Md serves as a

temporary memory device and is set whenever a Dpd signal has been received. The Md flip-flop is reset after four shift pulses (Mc) have been generated. During the time that the Md signal is true, a Mc pulse is generated whenever the T51 and T52 flip-flops are true simultaneously. The first shift pulse may occur at any time but subsequent shift pulses are generated periodically every four word times until the Md flip-flop is reset. The Mc1 and Mc2 flip-flops also function as a modulo four counter and are advanced whenever a Mc pulse is generated. Figure 3-13 is a combination logic and block diagram showing the data flow into and out of the Db1 through Db4 flip-flops.

The transferring of information from the Db4 flip-flop to the binary data buffer and to the decimal converter scaler is controlled by the following logic equations:

$$Bic = Db4Md + Coc$$

$$Bip = \overline{\overline{(Mc1}\ \overline{Mc2)}}\ Mc + Cop$$

Note: The term $\overline{\overline{(Mc1}\ \overline{Mc2)}}$ can be reduced to (Mc1 + Mc2). Thus, the Bip signal is generated at all times except when both Mc1 and Mc2 are off, the initial configuration of these two flip-flops.

The Bic signal is true whenever a true bit appears in the Db4 flip-flop and the Bip signal is a control pulse which permits only the original contents of Db1 through Db3 (an octal character) to be shifted into the binary data buffer. All four bits are always transferred into the decimal converter register.

If octal information were processed during the DATA mode, the contents of the binary data buffer is valid and the contents of the decimal converter scaler register is disregarded. Information within the binary data buffer is transferred to the addressed module by executing a FILL operation. If decimal information were processed during the

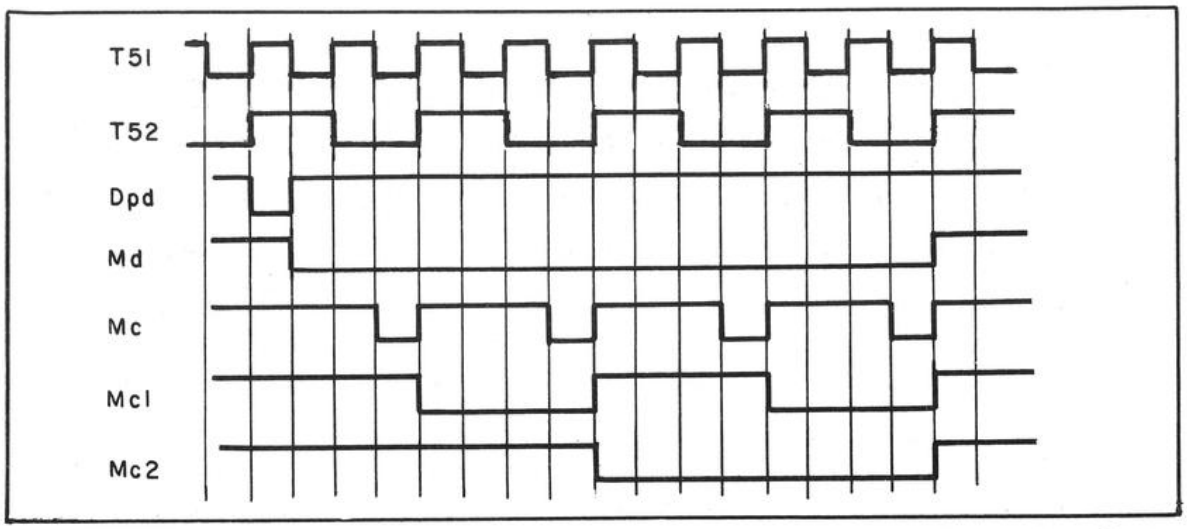

FIGURE 3-12. TIMING AND CONTROL PULSES FOR SHIFTING DATA FROM Db1-Db4

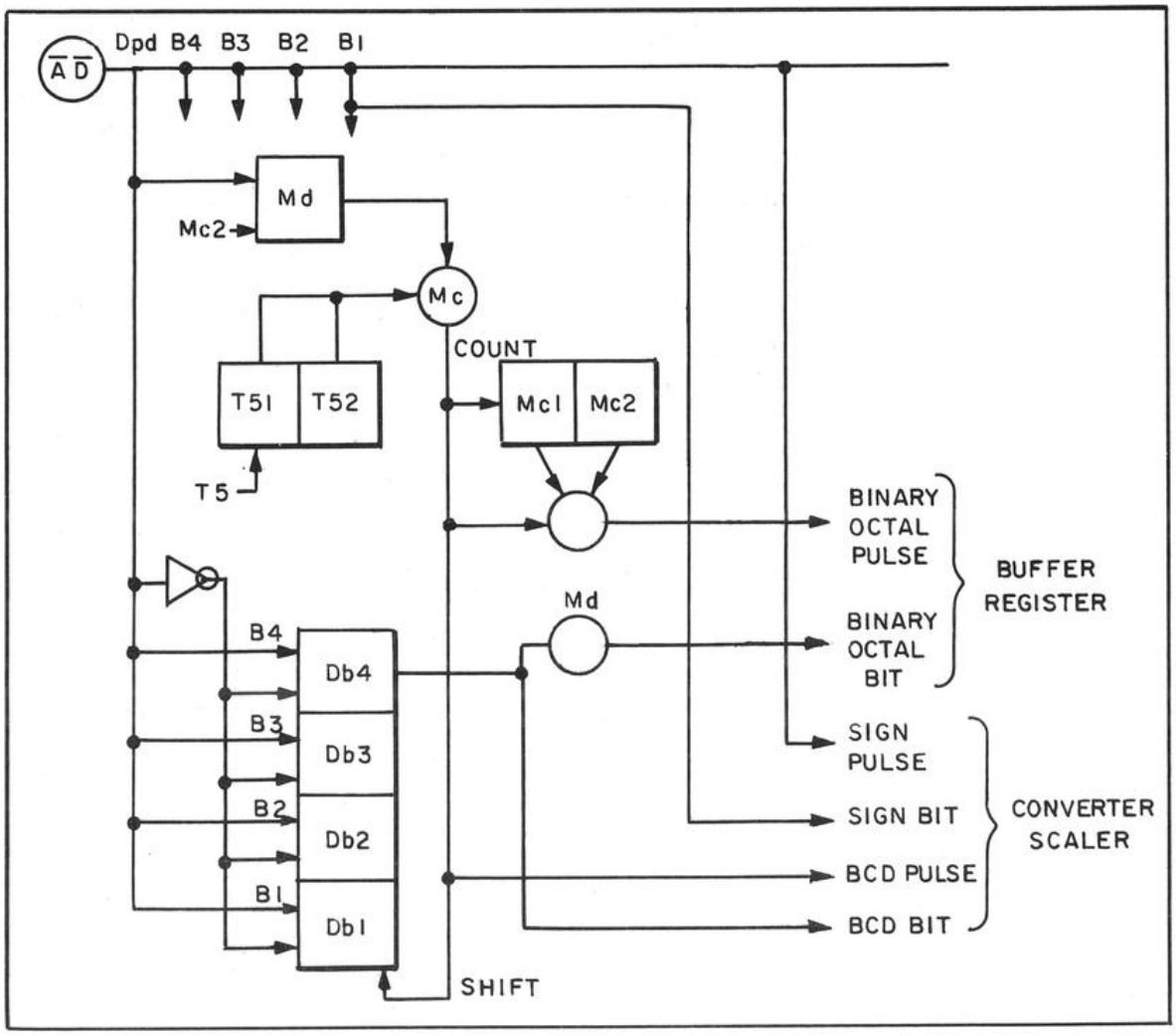

FIGURE 3-13. DATA INPUT CONNECTIONS

DATA mode, the contents of the decimal converter scaler register is valid and the contents of the binary data buffer is erroneous and is disregarded. By executing a CONVERT INPUT operation, the contents within the decimal converter scaler register is converted into an equivalent binary number and transferred into the binary data buffer.

The Bic and Bip signals control the transfer of data into the binary data buffer in the following manner:

1. The Bip Signal turns on the Bi flip-flop.
2. The Bi flip-flop in conjunction with a P30 signal (last bit time of each word) turn on the Sg flip-flop. At the same time, the data bit Bic is transferred into the Rdc flip-flop.
3. During the time that the Sg flip-flop is on, the Rdc flip-flop is added in series with the binary data register between flip-flops Rd30 and Rd1 and information within these flip-flops is shifted from the Rd1 end toward the Rd30 end at a 3 mc rate.
4. After one word time, the Sg and Bi flip-flops are turned off.
5. The Rdc flip-flop now contains the former Rd1 bit and the new bit is in Rd30. The bits which were formerly in positions Rd2 through Rd30 have been shifted to positions Rd1 through Rd29.
6. After the Sg flip-flop is reset, the Rdc flip-flop is disconnected from between Rd1 and Rd30.
7. The Rd1 bit shifted into the Rdc flip-flop is lost when the Rdc flip-flop is reset at the first P1 time after the Sg flip-flop is reset.

Complete logic equations for the various flip-flops mentioned in the preceding paragraph are as follows: (Only equations containing a Bi or Sg term are used during the transfer of information from flip-flops Db1 - Db4 to the binary data buffer)

rdc = $\overline{Rdc}$ Csc (CV) + Bi Sg Cℓ1 Rd30 + Bi $\overline{Sg}$ P30 Cℓ1 Bic + (So Ra1) P1 Cℓ1

Rdc

ordc = Rdc Csc ($\overline{CV}$) + Bi Sg Cℓ1 $\overline{Rd30}$ + $\overline{Sg}$ P1 Cℓ1

rd1 = $\overline{Rd1}$ Cℓd [Es Gsg Ra9 + So $\overline{Ra1}$ (I-Y) + Sc Rdc + Bi Rdc + Bop Rd30]

Rd1

ord1 = Rd1 Cℓd [Es Gsg Ra9 + So $\overline{Ra1}$ (I-Y) + + Sc Rdc $\overline{+ Bi Rdc + Bop Rd30}$]

Rd2 . . . . . Rd29 shift register, shift clock Cℓd

rd30 = $\overline{Rd30}$ Cℓd Rd29

Rd30

0rd30 = Rd30 Cℓd $\overline{Rd29}$

bi = $\overline{Bi}$ Bip Cℓ1

Bi

obi = Bi Sg P30 Cℓ1

sg = $\overline{Sg}$ Cℓ1 [P30 Si + P1 So $\overline{Ra1}$ + P16 (So Ra1) + P30 Bi] + P16 Cℓ1 Bop $\overline{Es}$

Sg

osg = Sg Cℓ1 [P30 Si + P1 So $\overline{Ra1}$ + P16 (So Ra1) + P30 Bi] +Sg Cℓ1 Bop

Cℓ1 = TRICE clock (3 Mc)

Cℓd = Es Gsg Cℓ2 + Es Hsg Cℓ2 + Sg Cℓ1

During PB250 operations (BSO and BSI commands), the address register (Ra1 through Ra9) and the binary data register (Rd1 through Rd30) are connected as a 39 bit shift register. Information from the computer is shifted into Ra1 and toward Ra9. Ra9, in turn, shifts data into Rd1. Data in Rd1 is shifted toward Rd30. For these operations, the COMPUTER control mode (UW) and the ADDRESS mode ($A\overline{D}$) must be selected, which makes signal Es true.

Logic equations for generating control and timing signals associated with the COMPUTER control mode are as follows:

$$C\ell 2 = \text{PB250 clock (2 Mc)}$$
$$Es = (A\ \overline{D})\ (U\ W)$$
$$C\ell d = Es\ Gsg\ C\ell 2 + Es\ Hsg\ C\ell 2 + Sg\ C\ell 1$$
$$C\ell a = Es\ Gsg\ C\ell 2$$
$$Hdg = Rd30$$

During a BSO command, the PB250 generates Gdg and Gsg signals. The Gdg signal represents data output and the Gsg is a shift mask which permits the data to be shifted into the Ra and Rd flip-flops. During a BSI command the PB250 generates an Hsg signal which permits data only from the Rd flip-flops (Hdg) to be shifted into the computer.

Figure 3-14 is a simplified logic and block diagram illustrating the transfer of data between the Ra and Rd flip-flops and the computer.

C-2e. Read Operation

During a read operation, information within the I or Y register of a TRICE module or within a converter module, as specified by the address register, is transferred into the binary data register.

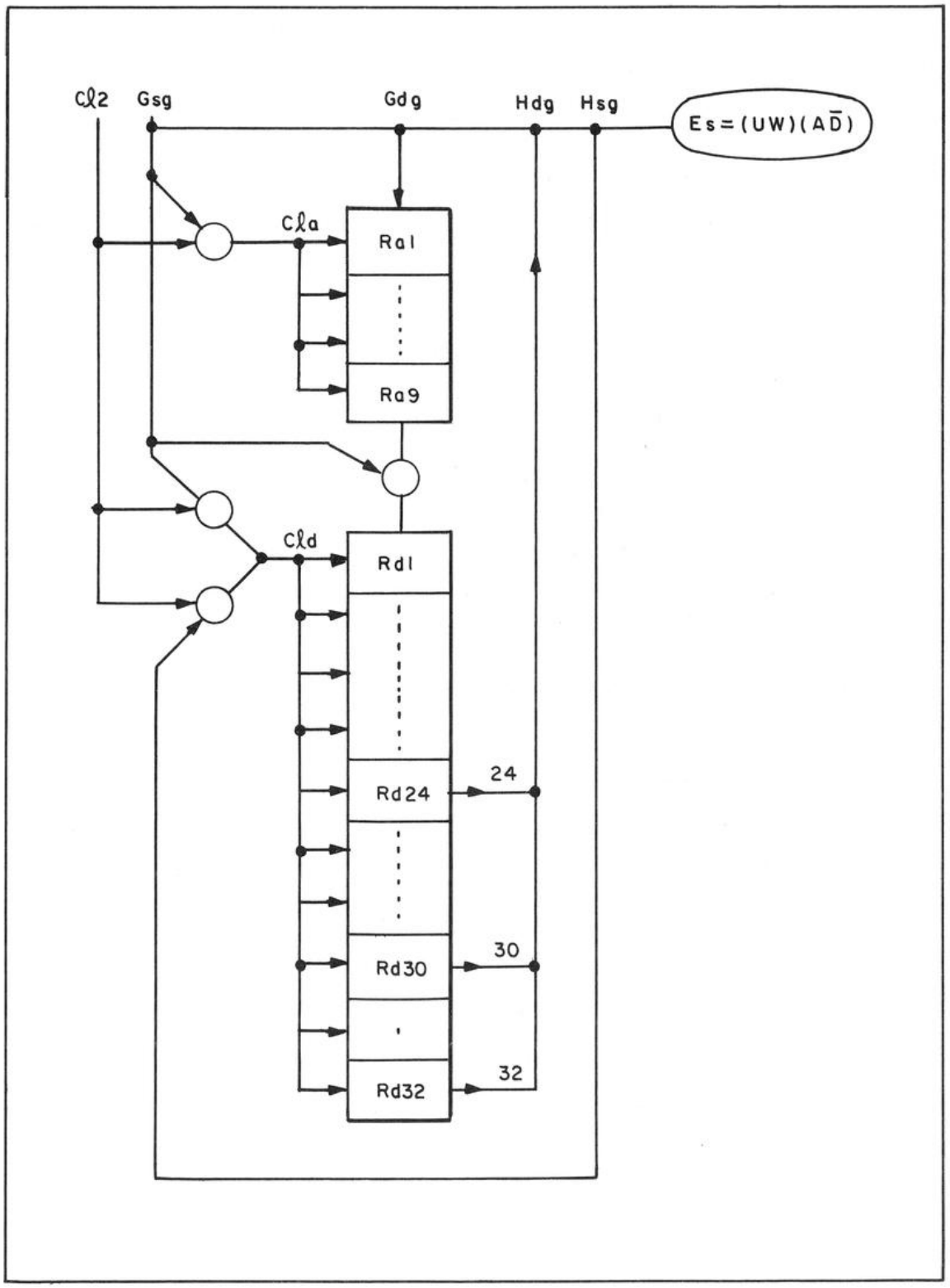

FIGURE 3-14. PB250 DATA INPUT-OUTPUT CONNECTIONS

The following logic equations are used when reading informaton out of a selected TRICE module:

$$Ep = Bp\ (B6\ \overline{B5}\ Po + B6\ B5\ Pe)$$

$$Sop = Ep\ Bc5 + Dip$$

$$so = \overline{So}\ Sop$$

So

$$oso = So\ Sg$$

$$sg = \overline{Sg}\ C\ell 1\ (P1\ So\ \overline{Ra1})\ldots$$

Sg

$$osg = Sg\ C\ell 1\ (P1\ So\ \overline{Ra1})\ldots$$

$$(I\text{-}Y) = \overline{Ra9}\ (Y1 + Y2 + Y3 + Y5 + Y6 + Y7 + Y\ 8) + Ra9\ (I1 + I2 + I3 + I4 + I5 + I6 + I7 + I8)$$

$$rd1 = \overline{Rd1}\ C\ell d\ (So\ \overline{Ra1}\ (I\text{-}Y)\ \ldots$$

Rd1

$$ord1 = Rd1\ C\ell d\ (So\ \overline{Ra1}\ (I\text{-}Y))\ \ldots$$

Upon receipt of a control code (Ep Bc5) an Sop signal is generated which sets flip-flop So. The Sg flip-flop is turned on by the first P1 pulse after So is set. The Sg flip-flop is on for 30 bit times. During this time information from the I or Y register is shifted serially into the Rd1 flip-flop of the binary data register. After 30 bits have been shifted in, a second P1 pulse resets flip-flop Sg and the fall of Sg resets flip-flop So.

Information within converter modules is transferred into the binary data buffer in a similar manner to that described for the TRICE module. Logic equations which control this operation are as follows:

$$Sop = Ep\ Bc5 + Dip$$

$$so = \overline{So}\ Sop$$

So

$$oso = So\ Sg$$

$sg = \overline{Sg}\ C\ell 1\ (P16\ So\ Ral) \ldots$

Sg

$osg = Sg\ C\ell 1\ (P16\ So\ Ral) \ldots$

$sc = \overline{Sc}\ C\ell 1\ P1$

Sc

$osc = Sc\ C\ell 1\ P16$

$Cro = (So\ Ral)\ Sg\ \overline{Sc}$

$Cs = Sc + \ldots$

$Csc = Cs\ C\ell 1$

$(CV) = DA1 + DA2 + DA3 + DA4 + DA5 + DA6 + AD1 + AD2$
$= AD3 + AD4 + AD5 + AD6$

$rdc = \overline{Rdc}\ Csc\ (CV) + (So\ Ral)\ P1\ C\ell 1 + \ldots$

Rdc

$ordc = Rdc\ Csc\ (\overline{CV}) + \overline{Sg}\ P1\ C\ell 1 + \ldots$

$rdl = \overline{Rd1}\ C\ell d\ (Sc\ Rdc) \ldots$

Rd1

$ordl = Rd1\ C\ell d\ \overline{(Sc\ Rdc)} \ldots$

A control code (Ep Bc5) generates an Sop signal which turns on flip-flop So. At P16 time the Sg flip-flop is turned on and remains on until the next P16 time. From P17 through the following P1 time, Sg is on and the Sc signal is false and, a Cro signal is generated and routed to the selected converter. The Cro signal permits a parallel transfer of the data (14 bits including sign) from the counter register to the converter buffer register. The Cro signal is terminated when the Sc flip-flop is set at the fall of P1 time. The Sc flip-flop stays on for 15 bit times and allows an equivalent number of shift clock pulses (Csc) to be generated. During the shift operation, information from the converter buffer register (CV) is shifted serially into the binary data register (Rd1 through Rd30) in a serial manner via flip-flop Rdc. An articifial scaling bit is generated by setting the Rdc flip-flop at the fall

of P1 time. Shifting takes place from P2 through P16 times. The Rdc flip-flop is reset at the fall of the first P1 time following the shift operation. The sign bit of the data received from the converter buffer is in the Rd1 position, the leasts significant bit received from the converter buffer is in the Rd14 position and the artifical scaling bit is in the Rd15 position.

Figures 3-15 through 3-17 are timing charts illustrating the sequence of signals when transferring information into and out of buffer register, TRICE modules, and converter modules.

C-2f. Fill Operation

During a fill operation, information within the binary data register is transferred either to the I register of a selected TRICE module or to the converter buffer register of a selected converter module.

Logic equations for filling into a TRICE module are as follows:

Si

$$si = \overline{Si}\ Ep\ Bc6$$

$$osi = Si\ Sg$$

Sg

$$sg = \overline{Sg}\ C\ell 1\ (P30\ Si) \quad . \quad .$$

$$osg = Sg\ C\ell 1\ (P30\ Si) \quad . \quad . \quad .$$

$$Fs = Si\ \overline{Ral}\ Sg$$

$$If = Rd30\ Si\ Sg$$

The Si flip-flop is turned on by the control code (Ep Bc6) and at the following P30 time the Sg flip-flop is turned on. The combination of Sg, Si and $\overline{Ral}$ generates an Fs signal which is distributed to all TRICE modules. However, only one TRICE module, as determined by the address register, will respond to the Fs signal. Within the selected module, the Fs signal is gated with the If signal to permit new data

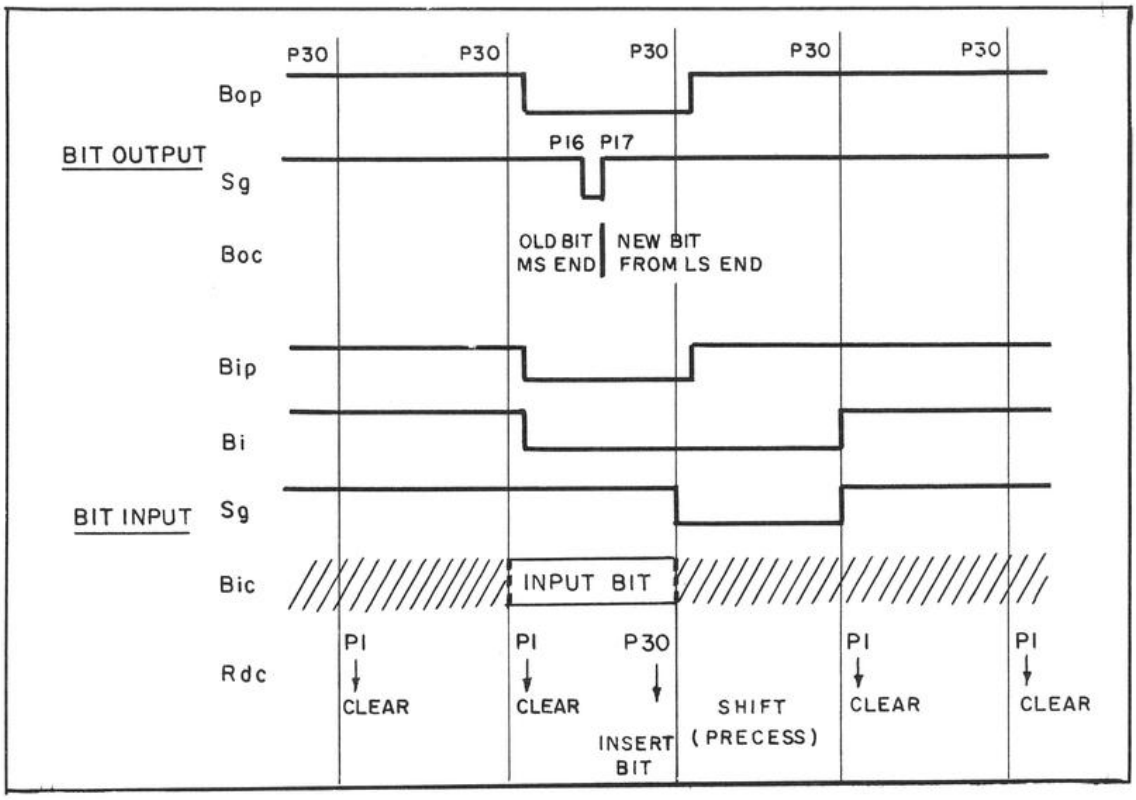

FIGURE 3-15. BUFFER REGISTER: BIT INPUT AND OUTPUT

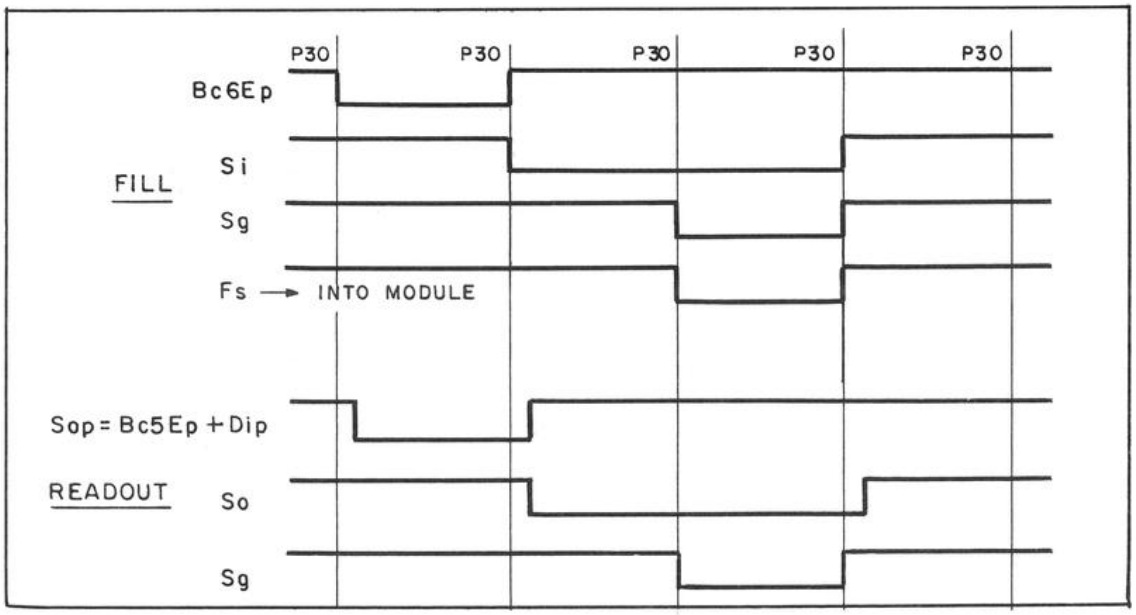

FIGURE 3-16. TRICE MODULE READOUT AND FILL (TIMING)

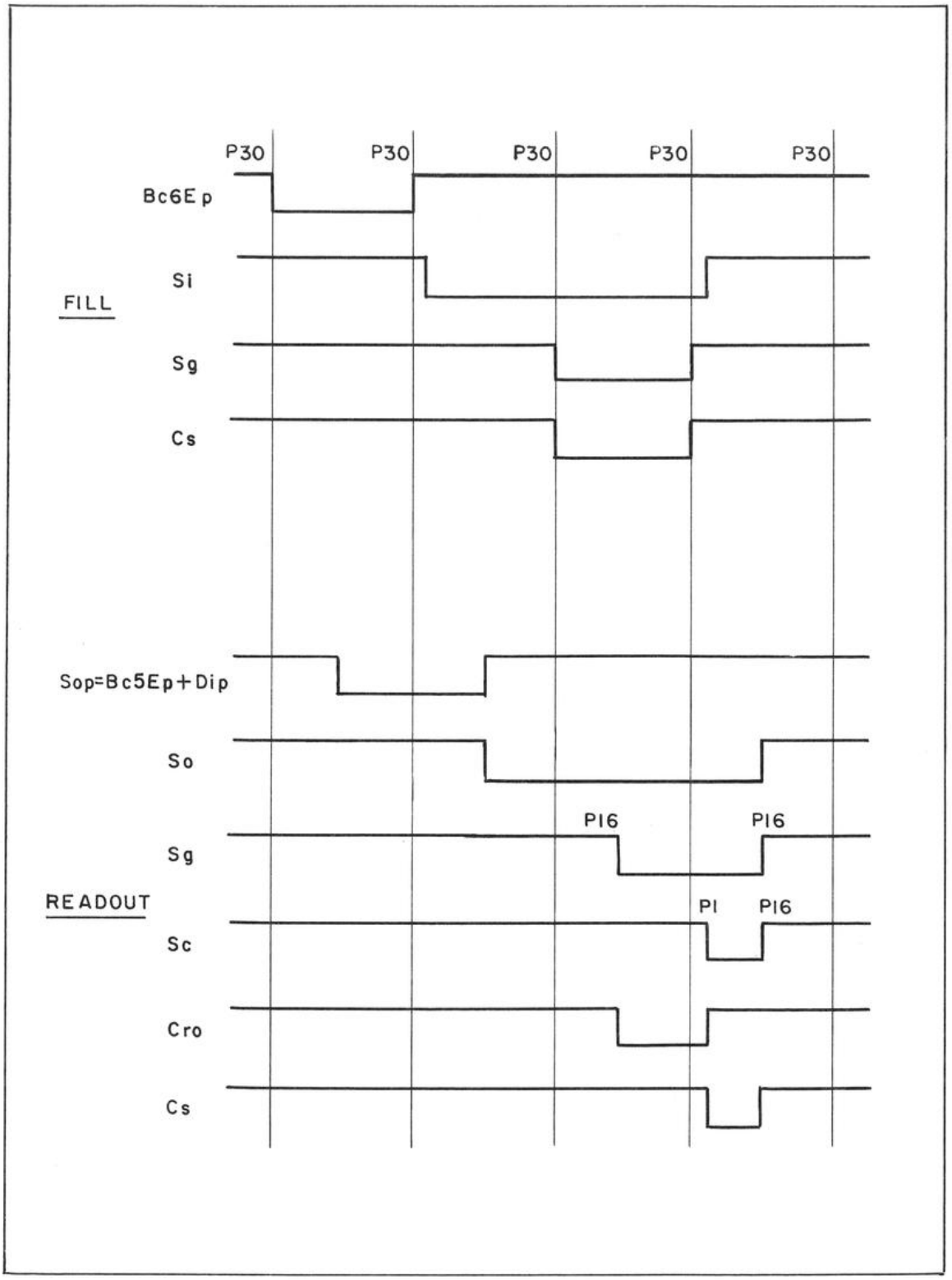

FIGURE 3-17. CONVERTER READOUT AND FILL (TIMING)

to be shifted into the I register from the binary data register. During the time that the Si and Sg signals are true (one word time), information is shifted from the Rd30 flip-flop of the binary data register into the In flip-flop of the I register within the selected TRICE module.

Logic equations for filling the converter buffer of a selected converter module are the same as listed for the TRICE module with the exception that a Cs signal is generated instead of a Fs signal.

Cs = Si Ral Sg

The Cs signal permits Csc signals to be generated which will shift the If signals into the most significant end of the converter buffer.

C-2g. Convert Input

During a convert input operation, information within the decimal converter scaler (BCD format) is converted into an equivalent binary value and transferred into the binary data buffer. Logic equations for tnis operation are as follows:

$Cop = \overline{A4}\ \overline{A3}\ (\overline{A2}\ A1)\ \overline{U1}$ (generated within decimal converter scaler)

$Coc = Cop\ (Ds\ Uo + D18\ \overline{Ds}\ K + \overline{D18}\ Ds\ K + Sb)$ (generated in decimal converter scaler)

$Bic = Coc$

$Bip = Cop$

$bi = \overline{Bi}\ Bip\ C\ell 1$

Bi

$obi = Bi\ Sg\ P30\ C\ell 1$

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$$sg = \overline{Sg}\ C\ell 1\ (P30\ Bi)$$

Sg

$$osg = Sg\ C\ell 1\ (P30\ Bi)$$

$$C\ell d = Sg\ C\ell 1$$

$$rdc = Bi\ Sg\ C\ell 1\ Rd30 + Bi\ \overline{Sg}\ P30\ C\ell 1\ Bic$$

Rdc

$$ordc = Bi\ Sg\ C\ell 1\ \overline{Rd30} + \overline{Sg}\ P1\ C1$$

$$rd1 = \overline{Rd1}\ C\ell d\ (Bi\ Rdc)$$

Rd1

$$ord1 = Rd1\ C\ell d\ \overline{Bi\ Rdc}$$

The Cop and Coc signals generated within the decimal converter scaler cause Bic and Bip signals to be generated within the buffer register unit. The Bip signal is a control or timing pulse which turns on flip-flop Bi. The Sg flip-flop is turned on by the first P30 pulse after the Bi flip-flop is on. The Sg flip-flop remains on for one word time. At the same time that the Sg flip-flop is turned on (fall of P30), a data bit, Bic, is received from the decimal converter scaler and transferred into the Rdc flip-flop. During the time that the Sg signal is true, the Rdc flip-flop is connected in between flip-flops Rd30 and Rd1. As a result, the new bit of data will occupy bit position Rd30 and the bit formerly in Rd1 is lost. The other bits are shifted by one position. This process is repeated until 30 new bits of data are within the binary data register.

Refer to paragraph F for further details on the decimal converter scaler.

C-2h. Convert Output

During a convert output operation, binary information within the binary data register is converted into an equivalent BCD value and

transferred into the decimal converter scaler. Logic equations for this operation are as follow:

Boc = Rd1

Bop = A4 $\overline{A3}$ ($\overline{A2}$ A1) $\overline{U1}$ (generated within decimal converter scaler)

sg = P16 Cℓ 1 Bop $\overline{Es}$

Sg

osg = Sg Cℓ1 Bop

rd1 = $\overline{Rd1}$ Cℓd (Bop Rd30)

Rd1

ord1 = Rd1 Cℓd ($\overline{Bop\ Rd30}$)

In the preceeding equations, the Boc signal follows the Rd1 flip-flop of the binary data register. The Bop signal is generated within the decimal converter scaler. The Sg signal is true only for one Cℓ1 time. As a result only one Cℓd (shift clock) pulse is generated per word time. The Cℓd pulse permits one bit of data to be shifted from Rd30 into Rd1 while the remaining bits within the binary data register are also shifted one place. The data bit shifted from Rd30 into Rd1 becomes the Boc pulse which is routed to the decimal converter scaler.

C-2i. Selection of Display Mode

During the display mode, information within a selected module of converter is read into the binary data register. As such, once the operation is iniitated, logic equations common to the read operation are used for the display mode.

Sr = 100 cps free running multivibrator

dip = $\overline{Dip}$ Sr ($\overline{A}$D)

Dip

odip = Dip T5

$$Sop = Dip$$

$$so = \overline{So}\ Sop$$

So

$$oso = So\ Sg$$

$$sg = \overline{Sg}\ C\ell 1\ (P1\ So\ \overline{Ral} + P16\ (So\ Ral) \quad . \quad . \quad .$$

Sg

$$osg = Sg\ C\ell 1\ (P1\ So\ \overline{Ral} + P16\ (So\ Ral) \quad . \quad . \quad .$$

After the A flip-flop has been reset and the D flip-flop has been set by an appropriate control code, the Dip flip-flop is set by the Sr signal and reset by the T5 signal. The Sop signal, which is generated when Dip is true, sets the So flip-flop. If a TRICE module has been addressed, the So signal causes the Sg flip-flop to be on for one word time from P1 to P1 times. If a converter module has been addressed, the So signal permits the Sg signal to be on for one word time from P16 to P16 time. During the times that the Sg flip-flop is on, a shift clock pulse is generated and new information is entered into the binary data buffer from the addressed module. Refer to the read operation for further details.

C-2j. Punch Output Mode

During the PUNCH OUTPUT mode, information within the decimal converter scaler is transferred to the paper tape punch. This mode is identified by having the A and D flip-flop both true. Further details describing the transfer of data is contained within subsequent paragraphs within this section.

D. TRICE MODULES

This section describes the theory of the five major computing modules used in the TRICE. The five modules are:

1) Integrator I5
2) Constant Multiplier CM5
3) Variable Multiplier VM5
4) ΔY Summer SU5
5) Servo S5

These modules mechanize digital differential analyzer algorithms. Pulse trains, representing increments of change in a problem variable, transmit information between computing elements. One-word registers in the computing elements accumulate these increments, starting from an initially set value, to represent the instantaneous value of the problem variable. The basic computing process in the computing element consists of adding the contents of this register to a second one-word register in the same computing element. Overflows of this register are considered output increments of the computing element. The maximum rate at which this addition can occur for each computing element is the iteration rate of the digital differential analyzer.

Externally, TRICE computing elements operate in parallel; internally, the computing process operates serially. This makes the iteration rate equal to the word rate (rate at which a one-word register is processed). The digital code used in the registers is straight binary. Negative numbers are represented as two's complement. The effective length of the register is variable — the total register length is constant. The significant part of the register is assumed to start after the least significant non-zero bit stored in the register. This bit (the scaling bit) is inserted as part of the starting value. It is not affected by computation. The position of the scaling bit determines the weight with

which increments are added to the register. This addition occurs at the least significant end of the significant part of the register, i. e., immediately after the scaling bit. The weight of the most significant end is fixed; in machine units the range of the register is $-1 \leq y \leq +1$. Machine units are related to problem units by the scale factor of the register.

Increments in TRICE can be positive, zero, or negative (ternary transfer). They are represented by the state of two lines, the existence line and the sign line. The existence line corresponds to the absolute value of the increment (logic true = absolute value one). The sign line represents the sign of the increment by logic true = positive sign, logic false = negative sign. The logic inverse of the sign line therefore represents the inverted sign. The state of the increment lines can change only once per computing iteration, i. e., the maximum rate at which increments can be generated is equal to the iteration rate. Conversely, if a pair of increment lines stay, for example, in the +1 state for n iterations, this corresponds to the occurrence of +n increments. Because of the serial computation in the computing elements, output increments resulting from computation in one iteration are generated only at the end of that iteration (word time). Therefore, they can only be used during the next iteration.

D-1. INTEGRATOR (Figures 3-18 through 3-22)

The logic equations, timing diagrams and block diagrams are placed together at the conclusion of this section and are intended to be used in conjunction with the following text.

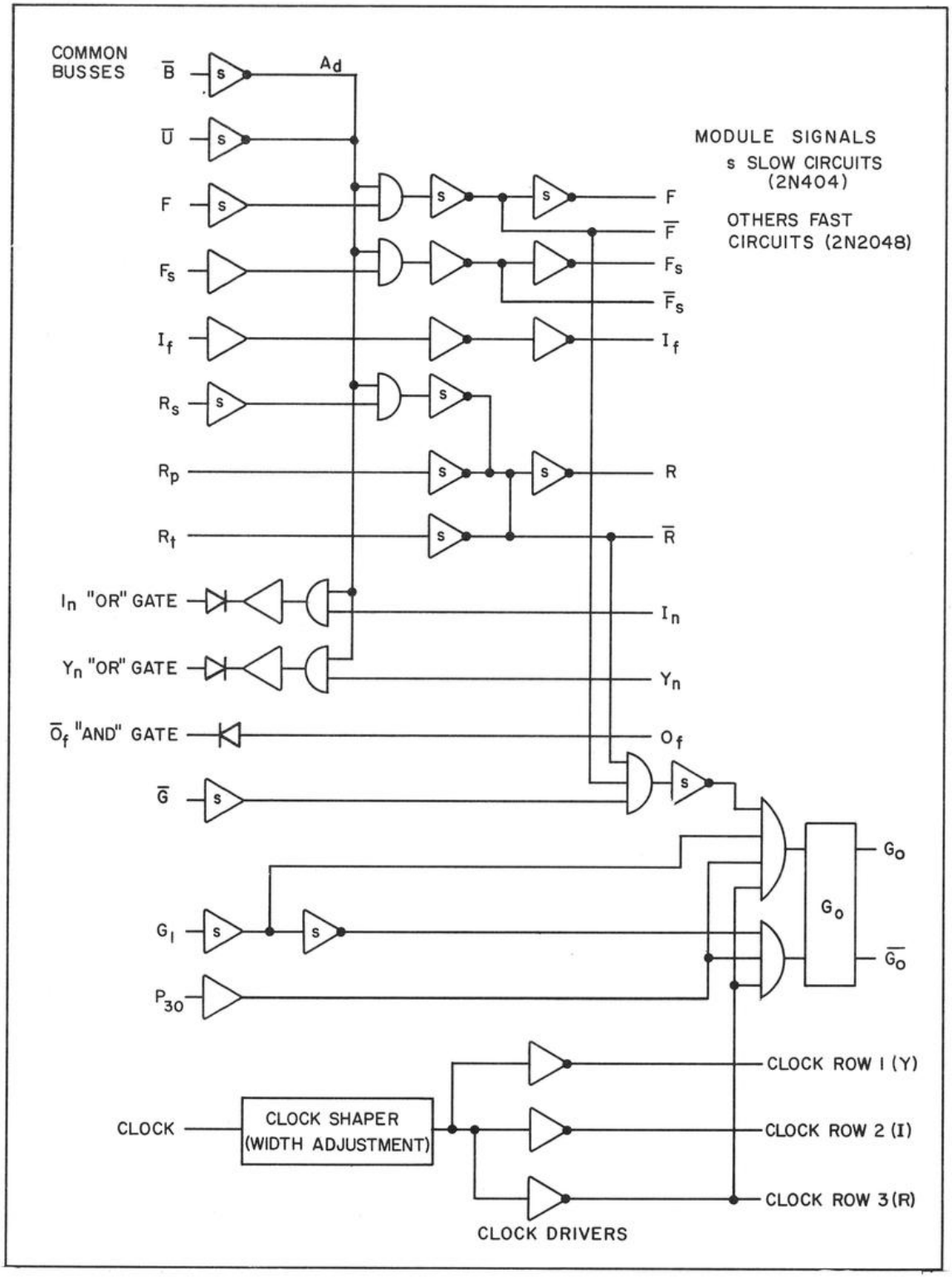


FIGURE 3-18. MODULE CONTROL, FILL, AND READ-OUT

The integrator contains 3 one-word registers. The I (initial condition) register stores the starting value of computation to allow fast access to this value for insertion into the Y (variable or integrand) register.

The I register, as all TRICE module registers, is a recirculating delay line register. Recirculation can be interrupted and new information inserted by their different operations.

a) The normal method used in the TRICE computer operates through logic terms F_s and I_f. F_s, the serial fill gate, goes true for one word time (one recirculation period). As it enters the module, F_s is gated by the address terms U and B, so only a module selected by its address can be filled. While F_s is true in the module, the I-register receives serial fill data signal I_f instead of recirculating its former contents.

b) The I register of the integrator can exchange its contents with that of the Y-register by term I_s. I_s interrupts recirculation in both I- and Y- registers and gates through I read flipflop into the Y write flipflop and the Y read flipflop into the I write flipflop. After one recirculation period the contents has changed places and I_s going false enables recirculation again.

c) The octal fill logic (terms F, I_x, I_y, I_z in conjunction with G_1) can insert one three bit octal digit at the least significant end of the I-register, move the rest of the register contents three bit positions towards the most significant end, shifting out the former three most significant bits. The process consists of two phases.

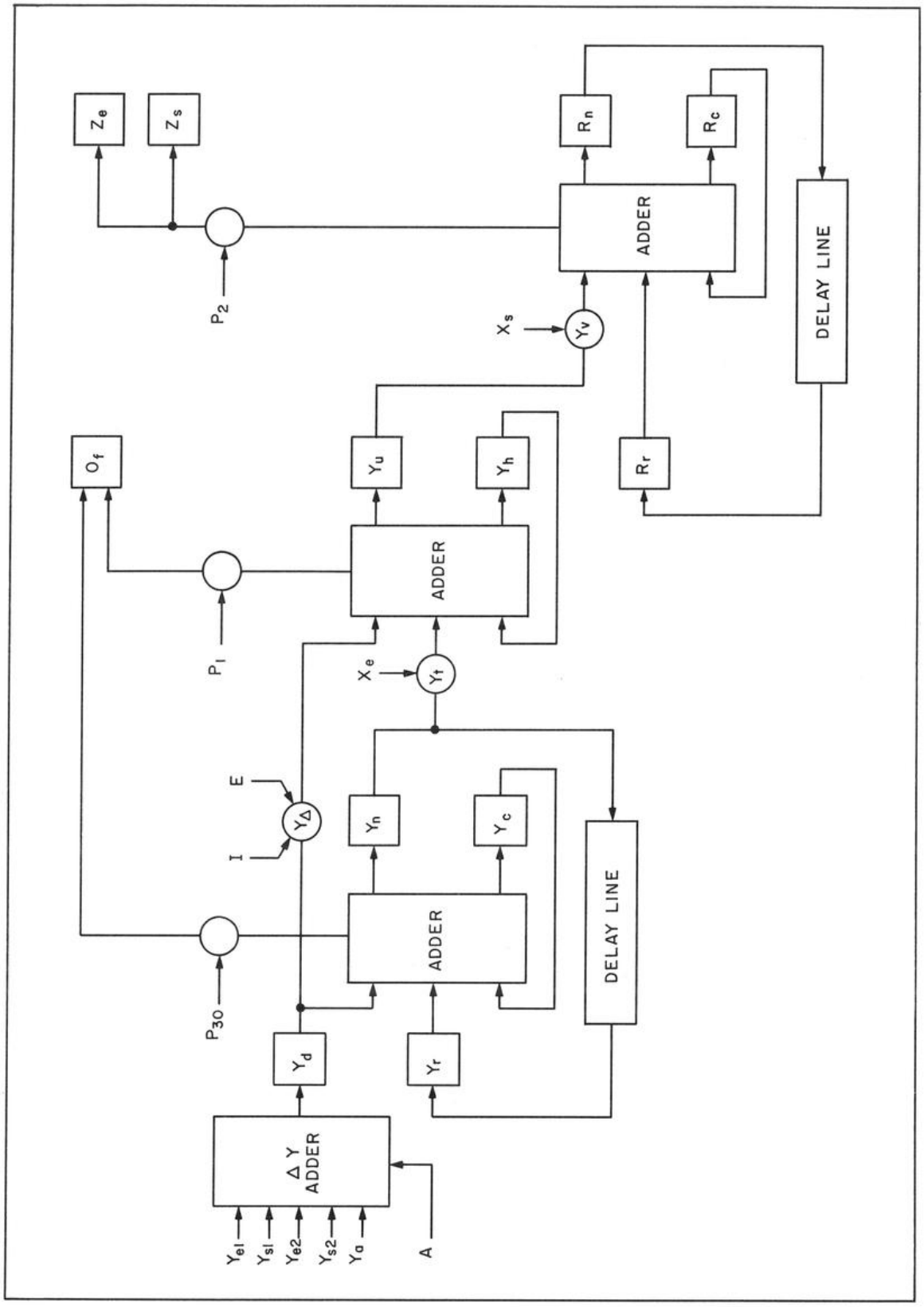


FIGURE 3-19. INTEGRATOR (Y REGISTER AND R REGISTER)

First F is true, but not G_o. During that time input lines I_x, I_y, and I_z are read into flipflops I_4, I_2, and I_1, respectively. When G_1 is found true at P_{30} time G_o is turned on, provided G_1 is found true at P_{30} time, and goes false after exactly one word time. F and G_o during that word time insert I_4, I_2, and I_1, as a three bit register in series with the recirculating I-register. At the end of one word time the three new bits are in the three least significant bit positions, the former three most significant bits are in I_4, I_2 and I_1 and all other bits are shifted three positions. F and G_o going false interrupt the lengthened register and restore normal recirculation. F is gated by the address lines like F_s. This logic is used only in the module tester and in some older, simpler versions of the TRICE computer input logic. It then operates directly from a manual keyboard.

The Y register stores the value of the integrand. The integrator can receive increments for addition to the Y register in either of two ways: (a) Directly from two sets of increment input lines (Ye1, Ys1, Ye2, Ys2) and combine them in the ΔY adder of the integrator into a serial representation of their sum at the output of the Yd flip-flop; (b) Indirectly from a separate ΔY summer computing module. This module performs a similar operation as the ΔY adder on six sets of increment input lines, and feeds the serial representation of the sum as signal Ya to the integrator, which then shapes and clocks it in the Yd flip-flop. This second input is qualified by the gateline A, which selects the ΔY summer for operation with the integrator on the patchboard.

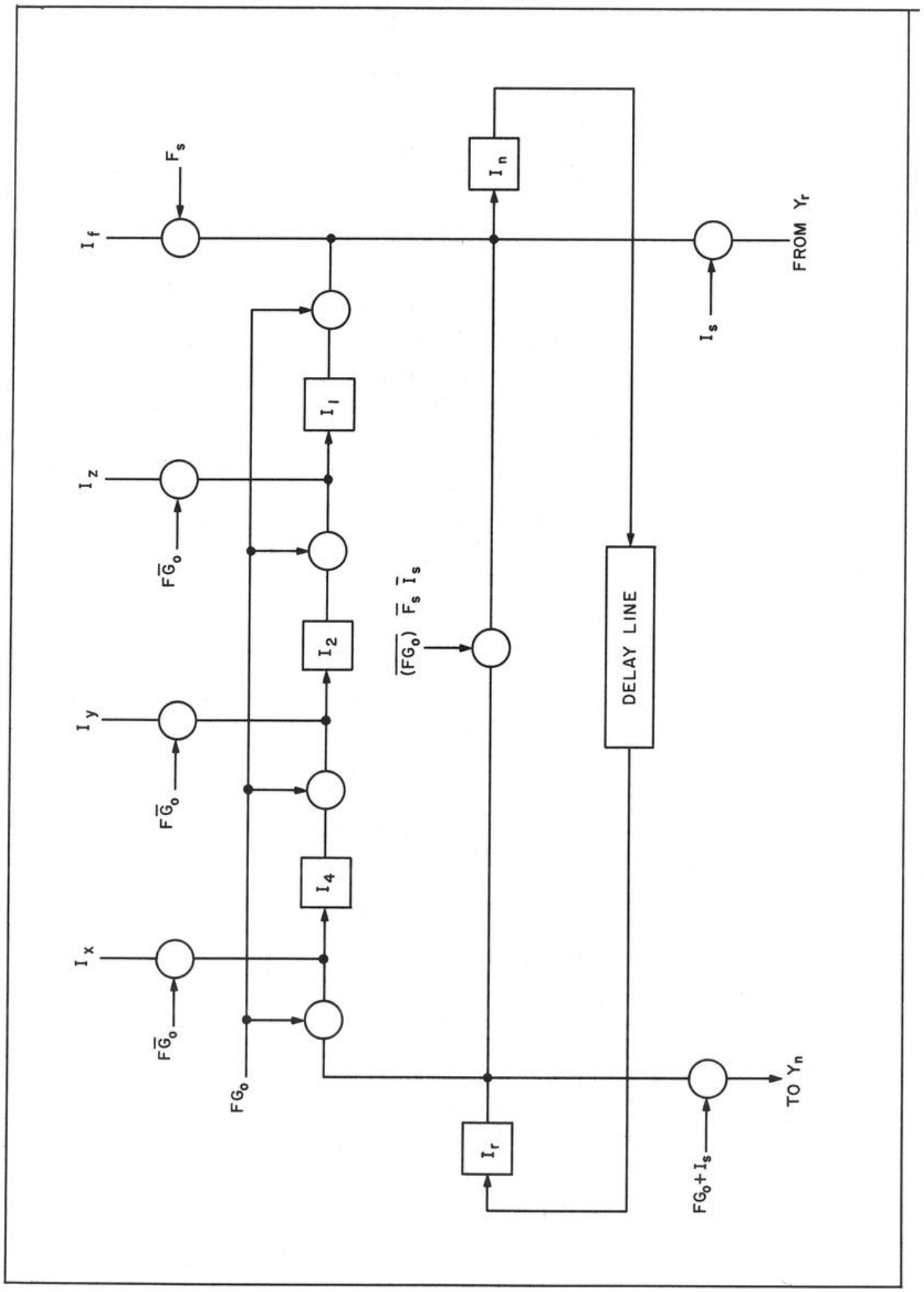


FIGURE 3-20. INTEGRATOR (I REGISTER)

In either case, the scaling bit in the Y register initiates serializing the sum of increments. Flip-flops I4, I2, and I1 are used during computation to sense the scaling bit, and to form timing signals to gate the significant part of the registers. At the most significant end of the register, I4, I2, and I1 form timing signals for sensing overflows of the registers. The scaling bit in the Y register flip-flop (Yr) turns on I4. Therefore, Yr $\overline{I4}$ is true only for the scaling bit.

I2 and I1 are turned on one pulse time after I4. I4 is turned off at the end of the word by the end-of-word pulse P30. I2 follows one pulse time later than I4, and I1 follows one pulse time after I2. Thus, I4 is on for the significant part of the Y register in Yr. It is used in the Y adder, which adds Yr and Yd and the carry Yc of this addition, to prevent the carry from extending beyond the sign bit of the Y register. I4 qualifies the $\overline{Yr}$ terms of this adder. It prevents one bits, out of Yd or Yd, from being stored in bit positions of the Y register beyond the sign bit, where there were no one bits before.

P30 time is sign bit time in Yr. The adder feeds the sum of Y and ΔY (represented by Yd) to the Y register write flip-flop Yn. In case computation is stopped, Yd does not come on (Go term on "on" trigger), nothing is added to the Y register, and the old value is recirculated by the first two terms of the adder logic: $\overline{Go}\ \overline{Is}$ Yr $\overline{Yd}\ \overline{Yc}$ + $\overline{R}\ \overline{Is}$ Yr $\overline{Yd}\ \overline{Yc}$, equivalent to $(\overline{Go\ R})\ \overline{Is}$ Yr $\overline{Yd}\ \overline{Yc}$. This term, in conjunction with the terms (Go R) Ir and Is Ir, serves to insert the contents of the I register into the Y register during the reset operation (Go R is true then), or the interchange operation (Is true).

The remaining terms of the adder do not interfere, because Yd cannot operate in the reset operation ($\overline{R}$ term on trigger); Yc cannot come true, because Yd does not come true. The interchange operation should not be used when increments are added to Y. No interlock is

provided in the logic for this case. Timing flip-flops I2 and I1 do not operate during the reset operation ($\overline{R}$ on their on triggers), whereas I4 operates as in compute. In this instance, I4 is required to generate an initial value for the R register. I2 and I1 not true inhibit computation in intermediate terms and inhibit the output flip-flop "on" triggers.

The remaining logic of the integrator mechanizes the exact integrating algorithm that leads to the generation of output increments. The new value of Y, with an interpolative or extrapolative correction term derived from Y, has to be added to the third register of the integrator, (the R register) and outputs generated from overflows. The addition of Y to R is qualified by a separate incremental input to the integrator, consisting of lines Xe and Xs. This is the primary input dx, the independent variable of integration. The algorithm to be mechanized is:

$$R_{new} = R_{old} + (Y_{new} \quad dx \quad + 1/2\,\Delta Y)\ \text{sign}\ dx$$

for extrapolative mode

$$R_{new} = R_{old} + (Y_{new} \quad dx \quad - 1/2\,\Delta Y)\ \text{sign}\ dx$$

for interpolative mode

$$R_{new} = R_{old} + (Y_{new} \quad dx \quad + 0)\ \text{sign}\ dx$$

if no special mode is selected.

The first term in the parenthesis is represented by Yt in the logic (Xe is true for dx = 1. I2 is true for the compute mode during the significant part of the Y register in Yn. The scaling bit is therefore suppressed by I2).

The second term in the parenthesis is represented by Y. (E) and I are true if extrapolative or interpolative modes are patched respectively. In case of interpolative mode, YΔ is the one's complement of

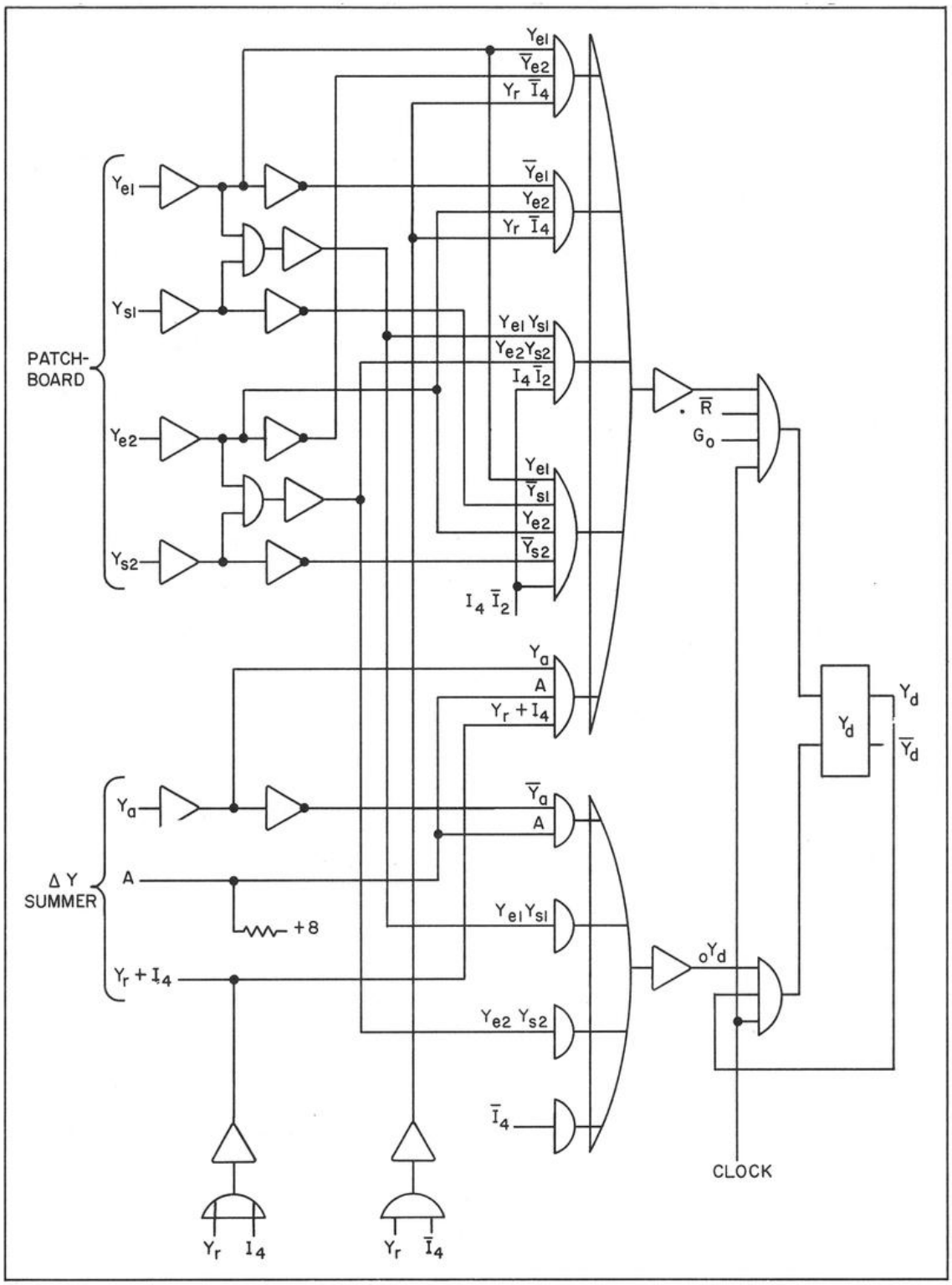


FIGURE 3-21. ΔY ADDER

Yd. The necessary correction to form the two's complement is added in by carry flip-flop Yh ((I) term in its on trigger). The carry in this case is already on for the least significant bit, adding an extra one into that position. Multiplication of the second term by 1/2 is accomplished by the timing difference between Yd representing ΔY, and Yn representing Y. Yd is one bit time early with respect to Yn; therefore, it is one-half as significant as Yn when the two terms are added. The two terms in the parenthesis are added into flip-flop Yu. Yh serves as carry flip-flop in the adder. Multiplication of the sum by the sign of dx occurs at the input to Yv by forming the one's complement, if the sign is negative. The complement correction in this case is added in by the flip-flop Rc of the R register adder.

The R register adder function is similar to the Y register adder. Bits of the same weight appear two pulse times later in R than in Y, to compensate for the delay through flip-flops Yn and Yu in forming the quantity to be added to Rr. This quantity Yv is gated by I1 to suppress the carry of the Yu adder beyond the sign bit. This use of I1 requires it to be turned on at the same time as I2, since the 1/2-increment bit has now been added at the least significant end to Yn (otherwise corresponding bits in Yn are one bit time later in Yu). The R register does not have a sign bit, therefore I2 is used to limit the carry, as I4 was used in the Y adder. The first two terms $\overline{Go}$ Rr $\overline{Yv}$ $\overline{Rc}$ + $\overline{R}$ Rr $\overline{Yv}$ $\overline{Rc}$ equivalent to $(\overline{Go\ R})$ Rr $\overline{Yv}$ $\overline{Rc}$ and the last term (Go R) I4 again are used to insert the initial value into the R register, and to recirculate the R value unchanged, if not in the COMPUTE mode. I1 in the later case does not come on, and so inhibits Yv. This results in nothing being added to R.

The initial value for R is generated by I4. I4 in the reset operation is turned on by the scaling bit in Y, as in the COMPUTE mode. It

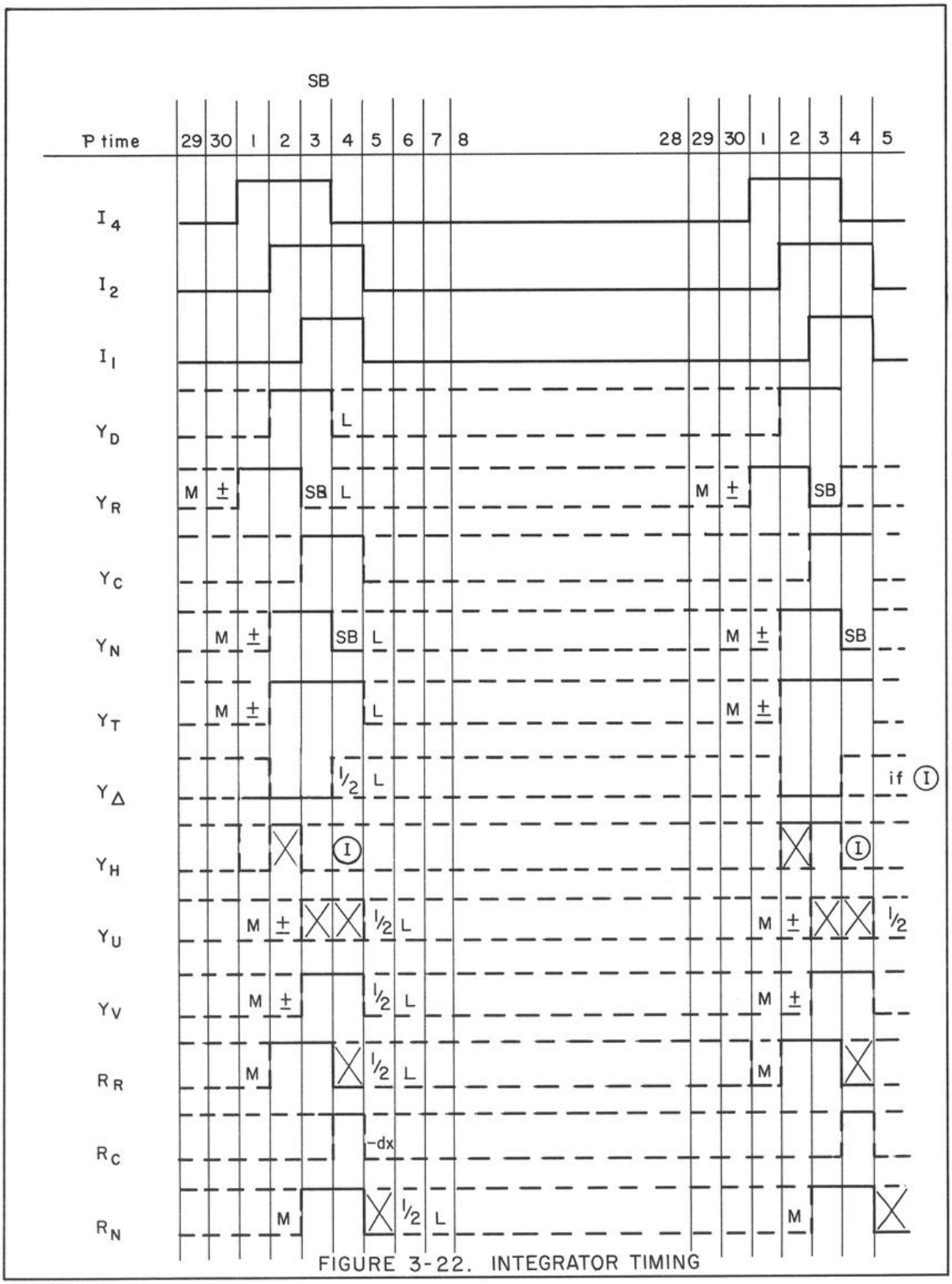


FIGURE 3-22. INTEGRATOR TIMING

is always turned off by P30. A bit pattern of one's extending from two bit times before the least significant bit to one bit time before the most significant bit (P1 time in the R register read flip-flop Rr), is entered by I4 into the R register. This represents a value one increment less than 1/2. It also enters a dummy bit before the 1/2 increment bit at the least significant end, which does not affect computation.

Overflow of the R register is detected by the logic of flip-flops Ze and Zs. P2 selects the sign bit time of the quantity Yv added to R. Rc is the carry of the R register adder into this position. $\overline{Yv}$ Rc means a positive quantity added to R and a carry into the sign position (i.e., positive overflow). Yv $\overline{Rc}$ indicates a negative quantity added to R, and no carry into the sign position (i.e., negative overflow). The two off trigger terms of Ze (the existence) represent the inverse condition. Zs (the sign) can change only when there is a non-zero overflow. The Of flip-flop senses overflow of the two other adders in the integrator. Overflow of the Y register is sensed by the P30 terms. Overflow of the Yu adder, i.e., the quantity (Y new dx $\pm$ 1/2 ΔY), is sensed by the P1 terms.

D-2. CONSTANT MULTIPLIER (Figures 3-23 and 3-24)

The logic equations, timing diagrams and block diagrams are placed together at the conclusion of this section and are intended to be used in conjunction with the following text.

The constant multiplier functions as an integrator with no ΔY input. Separate initial condition and variable registers are not required. The Y register of the constant multiplier contains fill logic similar to the integrator I register. It is selected as an I register by the control console, and is also used for addition to the R register

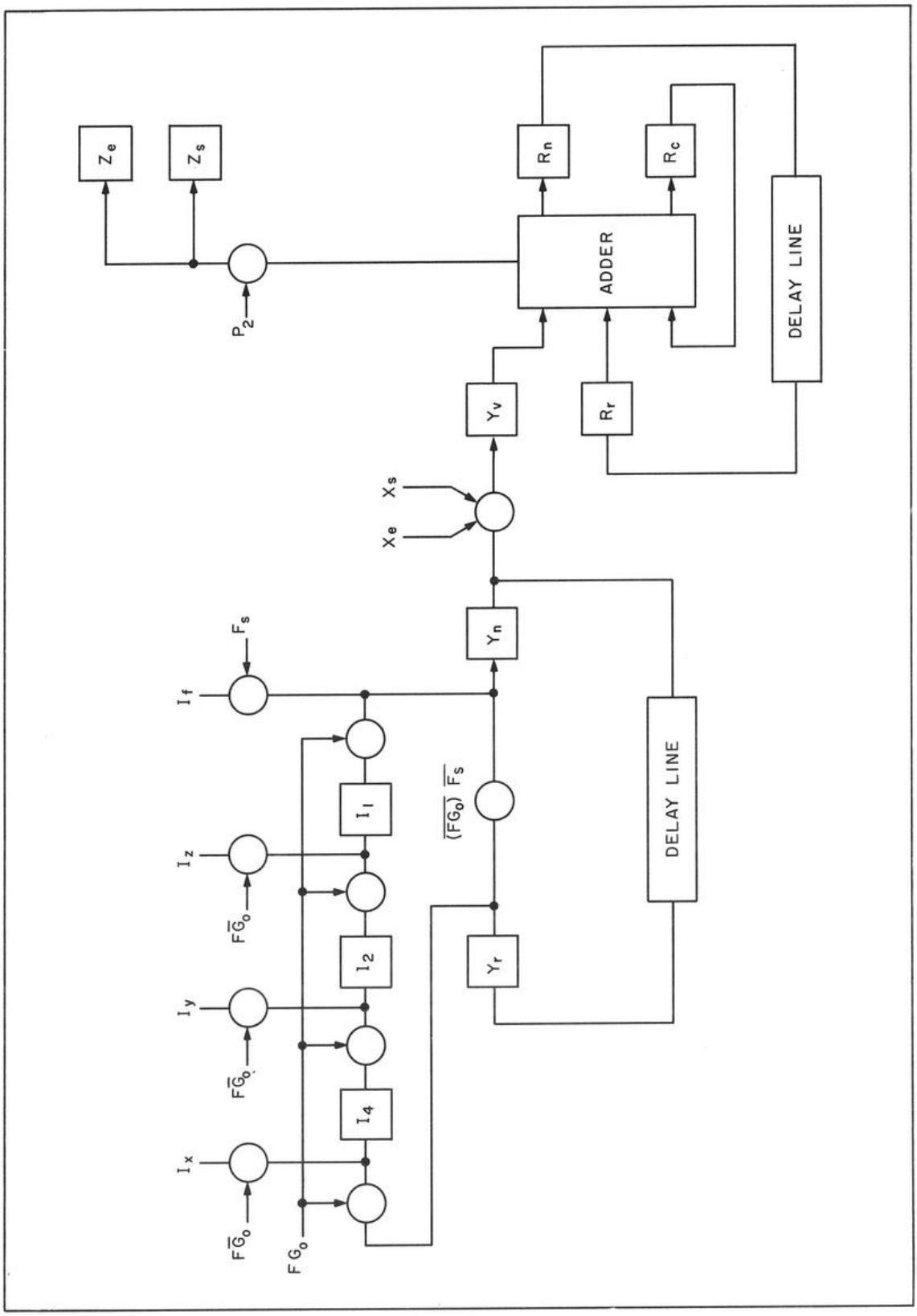


FIGURE 3-23. CONSTANT MULTIPLIER

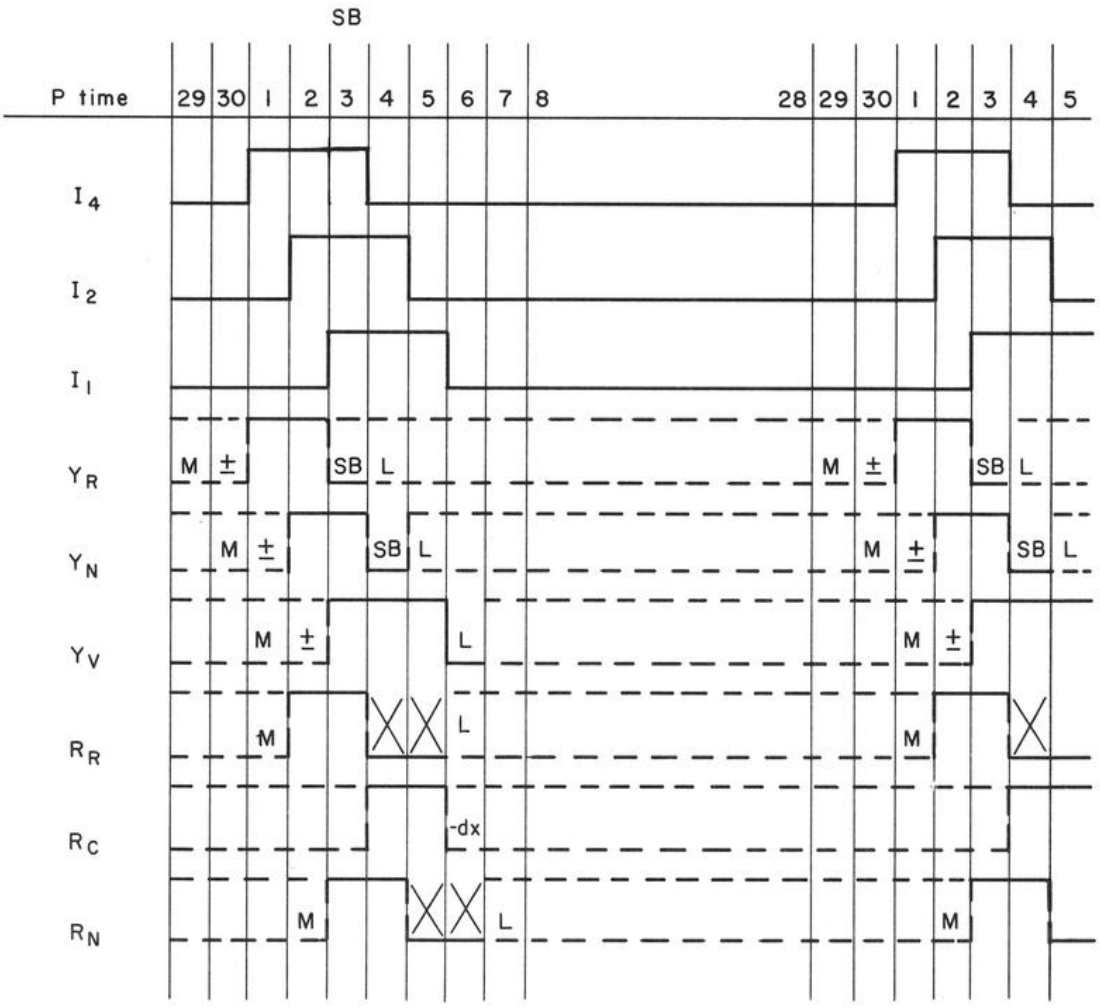


FIGURE 3-24. CONSTANT MULTIPLIER TIMING

similar to the integrator Y register. Since there is no ΔY, no adder for the trapezoidal correction term (Yu adder in the integrator) is required. Yv is in this case a flip-flop to generate a one-bit time delay. This makes the timing of the R register and the output generation the same as in the integrator.

D-3. VARIABLE MULTIPLIER (Figures 3-25 and 3-26)

The logic equations for the variable multiplier are located on pages 3-111 through 3-113 and supplement the following test.

The algorithm to be mechanized in the variable multiplier is the following:

$$R_{new} = R_{old} + Y_{new}\, dx + X_{old}\, dY$$

The logic function of the variable multiplier is similar to two integrators sharing one R register. There are two initial condition registers, Ix and Iy, and two variable registers X and Y. The fill and reset logic of these registers is the same as in the integrator. Only one incremental input is added to each of the variable registers X and Y, because the addition function can make use of only one increment per iteration. Flip-flops Xd and Yd serialize the input increments. Xc and Yc are the carry flip-flops of the X and Y adder. The Yx logic forms the one's complement of the new Y value according to the sign of dx, and gates Y with the existence of dx. The complement correction to form the two's complement is added by the carry flip-flop Yh of the Yv adder. The logic of flip-flop Xy performs the same function for the former X value using dY. A flip-flop is used in this case to compensate for the timing difference between former and new variable register value (read versus write flip-flop timing). The complement correction for this operation

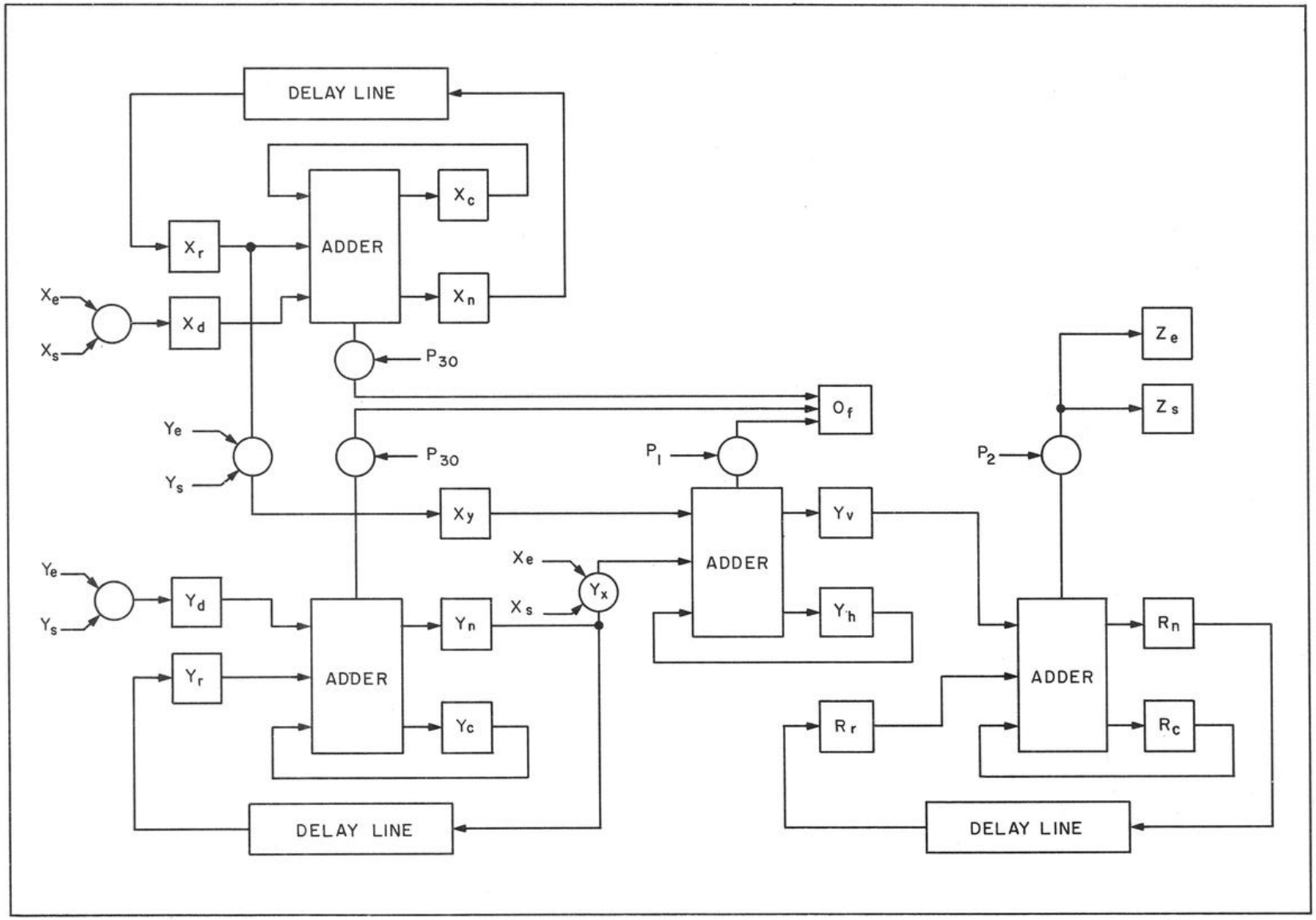


FIGURE 3-25. VARIABLE MULTIPLIER (X, Y, AND R REGISTER

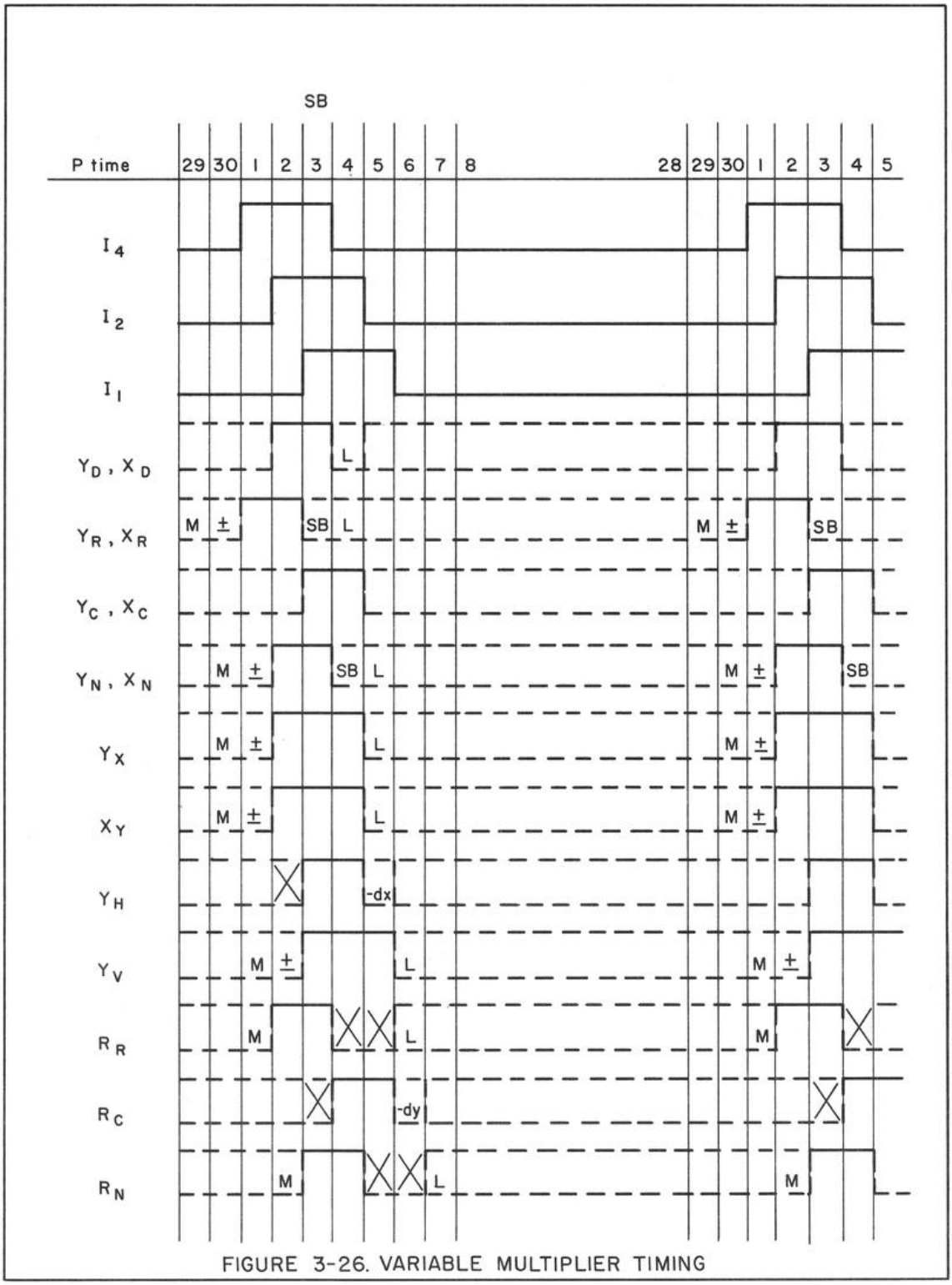


FIGURE 3-26. VARIABLE MULTIPLIER TIMING

is applied by carry flip-flop Yh. The logic of the R register, the R register overflow detection, and the generation of output increments are the same as in the integrator. Overflows of the two variable registers X and Y and of Yv (term added to R) are sensed by the overflow flip-flop Of.

D-4. ΔY SUMMER (Figures 3-27 and 3-28)

The logic equations, timing diagrams and block diagrams are placed together at the conclusion of this section and are intended to be used in conjunction with the following text.

The ΔY Summer is an auxiliary computing module, used to increase the number of possible incremental inputs to the Y register of an integrator or servo, from two to six. The sum output of the ΔY Summer in serial form is selected for use in one particular integrator or servo by a gateline (logic Ai or As) controlled by a jumper-plug on the patchboard.

The sum of increments is formed in three steps. A timing signal from the control unit (P4) turns on flip-flop P5. Flip-flop P6 follows P5 by one pulse time. The sum is formed in six register flip-flops: A, B, C, D, E, and F. The end-of-word pulse P30 clears all six flip-flops.

During P5 time the incremental input lines, Ye1, Ys1, Ye2, Ys2, Ye3, Ys3 are sensed, and their sum is generated in flip-flops A, B, C, in sign and absolute value form (A on for positive sign, B 2-bit, C 1-bit). Simultaneously, Ye4, Ys4, Ye5, Ys5, Ye6, Ys6 are sensed, and their sum formed in flip-flops D, E, F.

During P6 time, the two sums are combined to form a second sum, in sign and absolute value form, in flip-flops A, F, D, C (A on

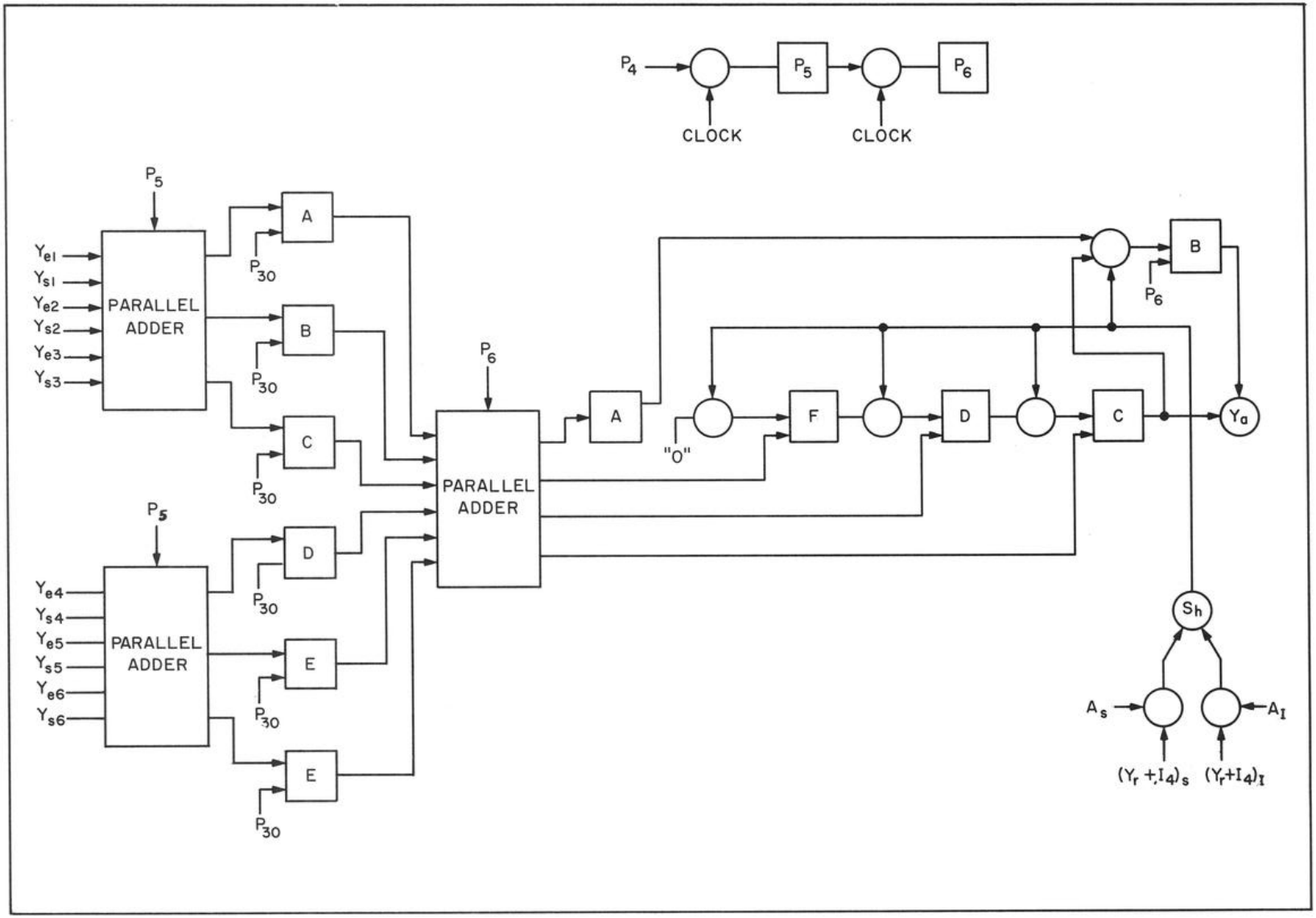


FIGURE 3-27. Δ Y SUMMER

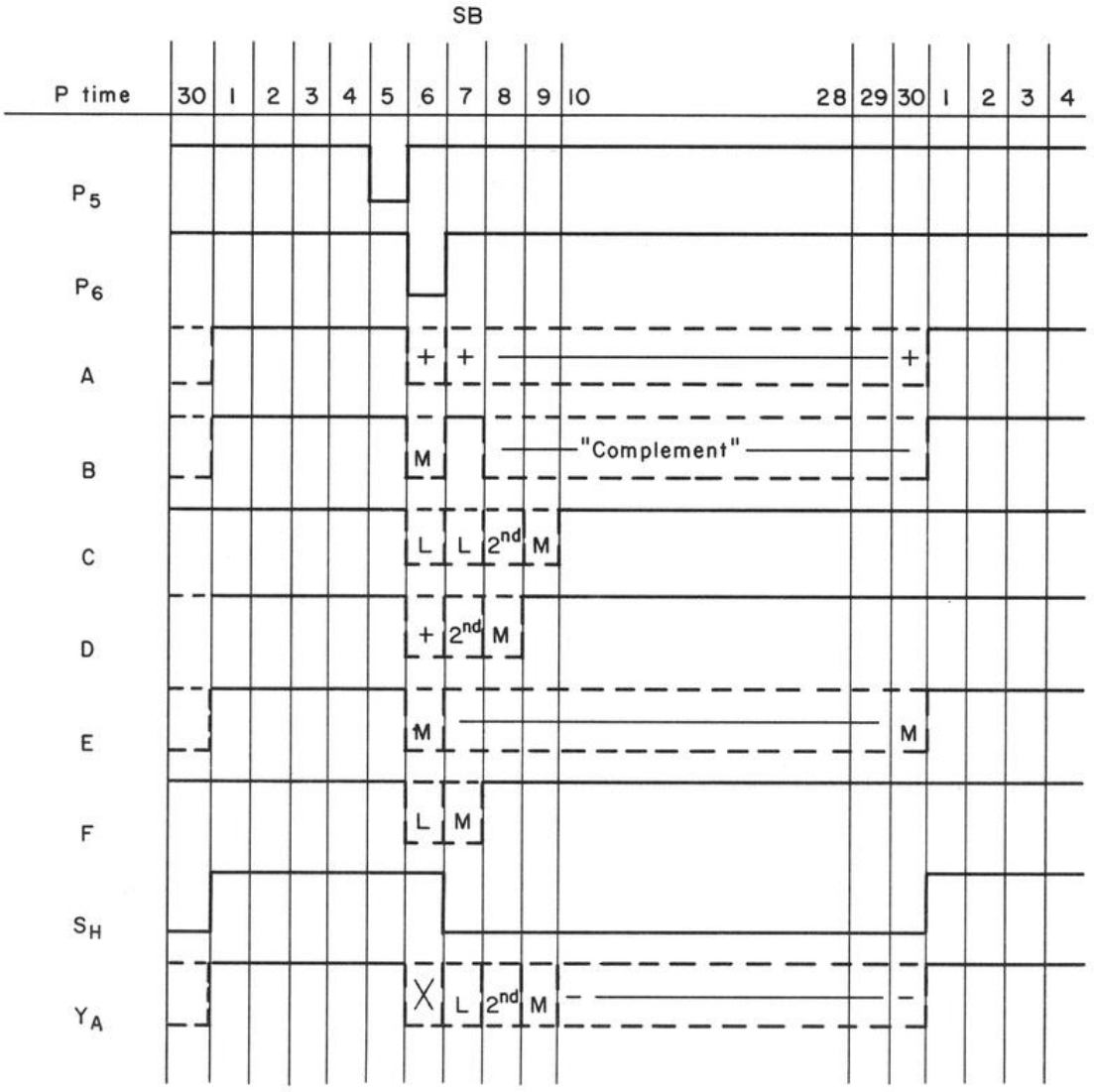


FIGURE 3-28. ΔY SUMMER TIMING

for positive sign, F 4-bit, D 2-bit, C 1-bit). Flip-flop E is not used in the remaining logic. Flip-flop B is always turned off by P6 time to prepare for the conversion of the sum to serial, complement form (Ya in logic).

Signal Sh, which is true for scaling bit through sign bit time of the integrator or servo selected for connection to the ΔY Summer, controls this conversion. The sum in F, D, and C is shifted out through C and replaced by zero. If the sum is negative (A off), B is turned on by the first one bit appearing in C. Any bit appearing in C after that is inverted so that the output Ya forms the true complement. Ya is fed to the Yd flip-flop of the servo or integrator connected to the ΔY Summer. The least significant bit of the sum is entered into Yd at scaling bit time, so as to appear on the output of Yd at the least significant bit time of the Y register read flip-flop Yr.

The formation of the sum in the ΔY Summer occurs independently of the Compute mode of TRICE. If TRICE is not in the Compute mode, signal Sh consists of Yr (Y register contents) only; therefore, serialization and complementation are not executed properly. The timing of formation of the sum in the ΔY Summer leads to a programming restriction. Since the shift and serialization can only start after formation of the sum, the scaling bit in the integrator or servo connected to the ΔY Summer can appear earliest in P7 time (with direct input to the integrator or servo P3 time would be possible). The maximum Y register length is restricted to 22 bits between scaling bit and sign bit.

D-5. SERVO (Figures 3-29 and 3-30)

The logic equations, timing diagrams and block diagrams are placed together at the conclusion of this section and are intended to be used in conjunction with the following text.

The I and Y register logic and function are very similar to those of the integrator. The computing process, i.e., the method of generating output increments, is different and peculiar to the servo. No addition of the Y value to an R register takes place here; instead, the value of Y is sensed by flip-flop I1. If I1 is on at P1 time, (sign bit time of Yn, the new Y value), and there is a primary input increment dx, Ze is turned on. This indicates the existence of an output increment. The sign of the output increment is controlled by flip-flops S and Zs. S follows the product of the sign of the primary input increment (Xs) and the sign of the new Y value (Yn at P1 time). Zs follows S, if an output increment (Ze true) exists. The delay between S and Zs also generates the proper timing of the output sign change, which is required at P2 time.

The functioning of I1 depends on the mode of servo operation (decision mode or normal mode). (D) is patched true on the patchboard for decision operation. In the normal mode I1 is turned on by any nonzero bit in the new Y value (Yn) between scaling bit and sign bit. I4 and I2, which operate identically as in the integrator, select this part of the Y register (I4 eliminates the sign bit, $\overline{I2}$ the scaling bit). I1 is always turned off by the I2 terms among its off triggers, i.e., after P2 time. In the decision mode, the $\overline{(D)P30}$ condition on I1 on trigger prevents I1 from being turned on by the most significant bit of Y. At this same time (P30 time), the (D) P30 terms among the I1 off trigger, implement the decision operation. The sign bit (yn at P30 time) and the most significant bit (Yn at P30 time) of Y are checked to determine if Y is larger than 1/2 in absolute value, in which case I1 is turned off (decision operation). Yn ($\overline{yn}$) is true for $Y \geq + 1/2$; $\overline{Yn}$ (yn) for $Y < - 1/2$. For $Y = + 1/2$ or $-1/2$, all bits to the right of the most significant bit are zero, so I1 has not been turned on before

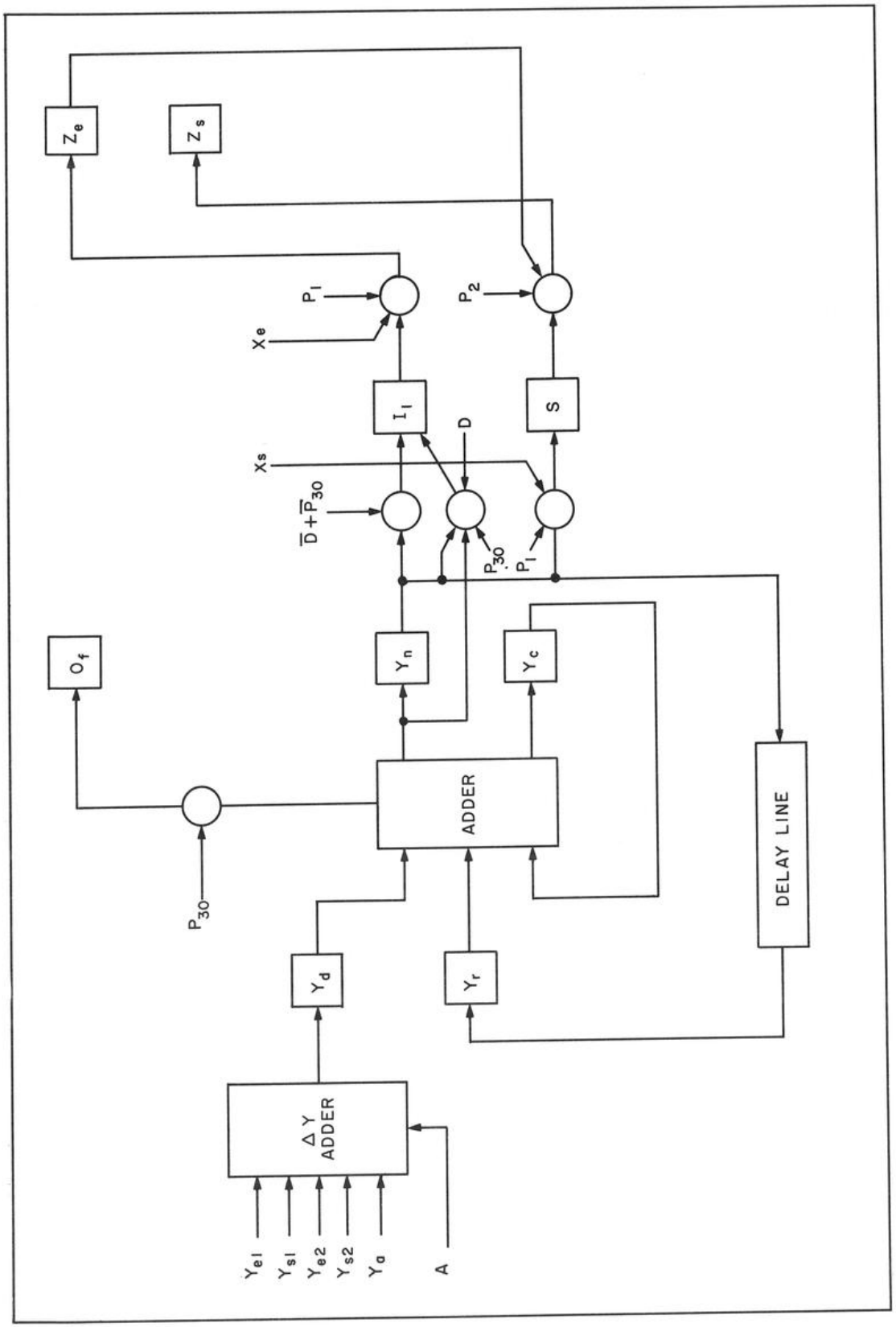


FIGURE 3-29. SERVO (Y REGISTER)

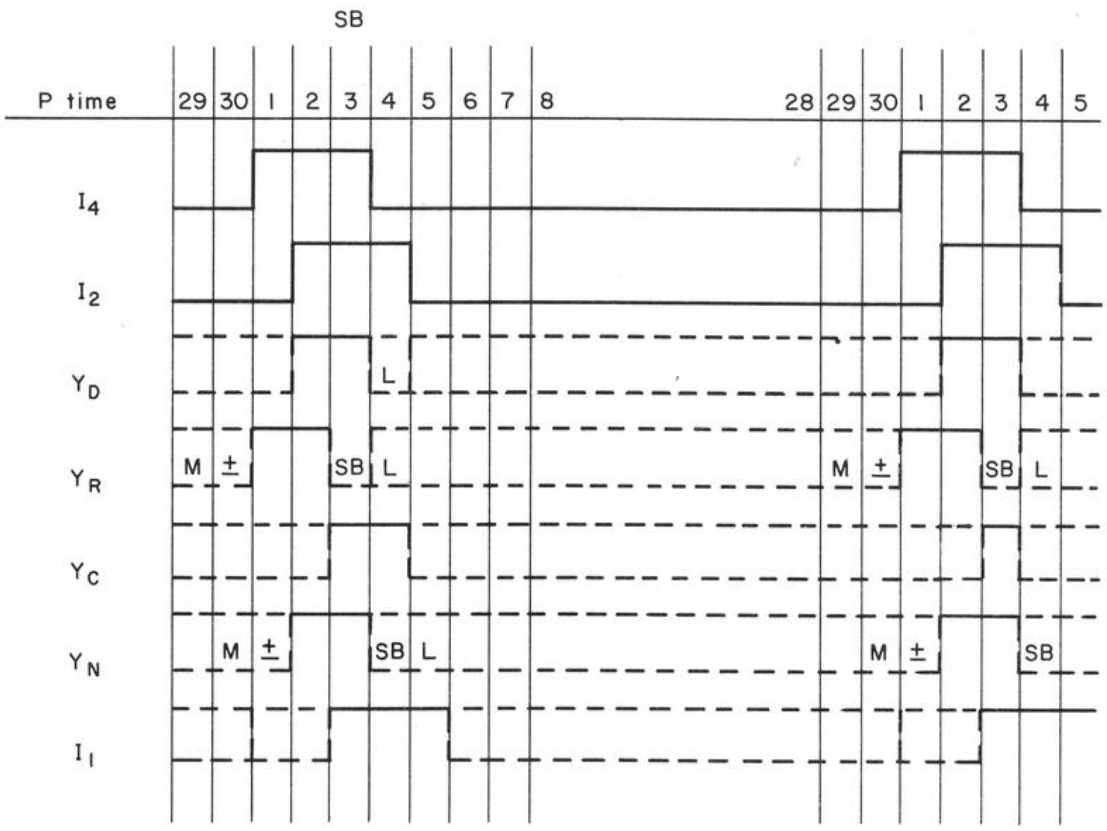


FIGURE 3-30. SERVO TIMING

the most significant bit time. The complete algorithm of the servo operation therefore is:

dz = 1 if dx = 1 and $0 < Y < 1$ for normal operation

or

dz = 1 if dx = 1 and $0 < Y < 1/2$ for decision operation

Sign dx = Sign dx Sign Y new

E. DIGITAL CIRCUITS

E-1. LOGIC CIRCUITS (3-31 through 3-35)

The digital circuitry employed in the TRICE system uses pnp transistors. The logic levels are negative voltages (about -8 v) for true, and zero voltage (ground level) for false. They are represented, for example, by the cutoff state and the saturated state of a grounded emitter pnp transistor switch. Flip-flops consist essentially of two pnp transistor switches crosscoupled. Resistor-capacitor coupling is used. Triggering of flip-flops occurs on the positive-going edge of the trigger pulse. A trigger capacitor is charged during the time the trigger pulse is at negative level. The rise of the trigger pulse then discharges this capacitor into the base of the conducting (saturated) transistor of the flip-flop. An isolating diode with a small dc back bias is used between base and capacitor to prevent noise from triggering the flip-flop. Diode gates implement the logic functions. AND gates consist of diodes, the cathodes of which are joined at a gate resistor that is returned to a negative voltage. Nominally 2 milliamperes are required to hold an AND gate false.

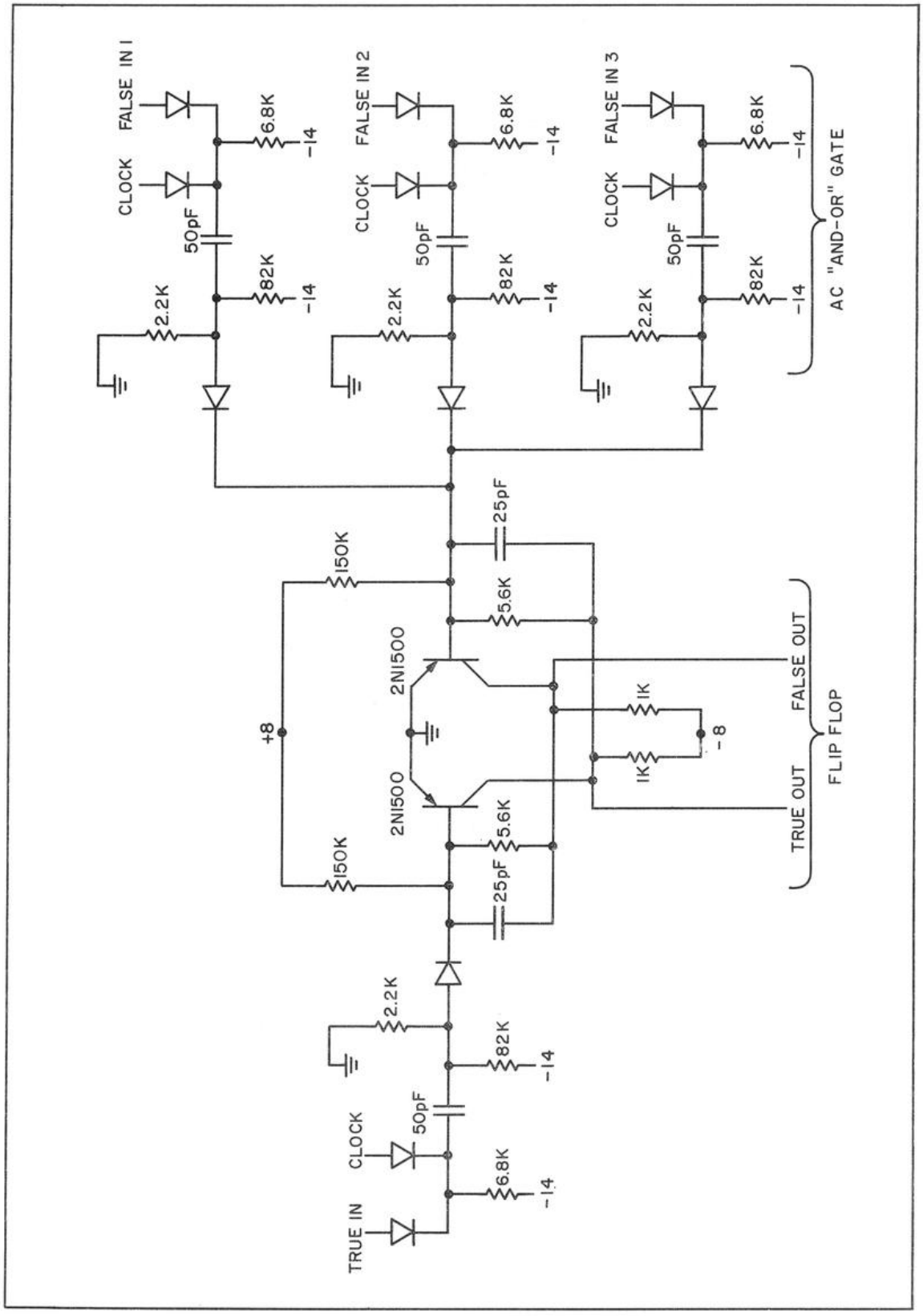


FIGURE 3-31. FLIP-FLOP AND AC AND/OR GATE

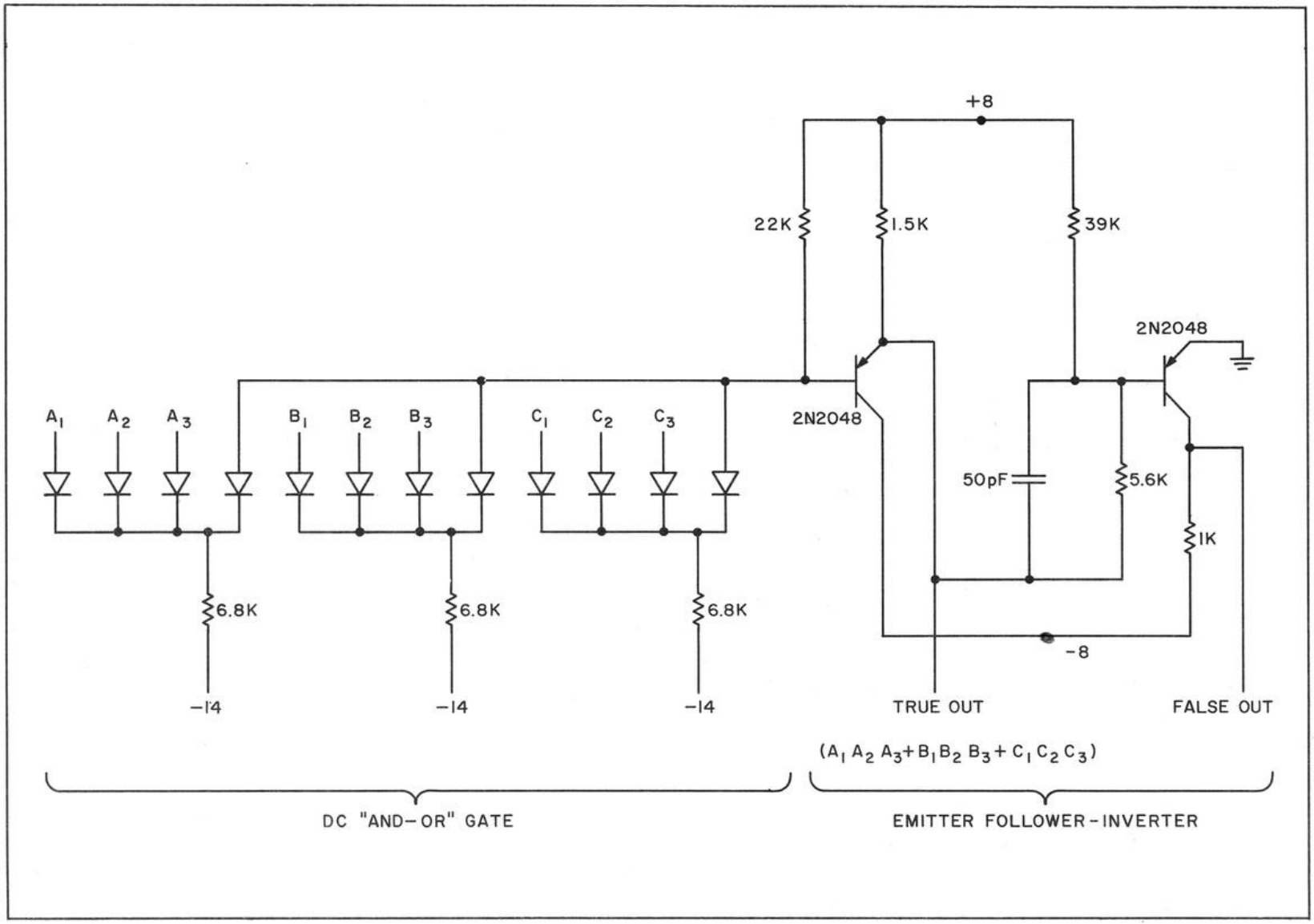


FIGURE 3-32. DC AND/OR GATE AND EMITTER FOLLOWER-INVERTER

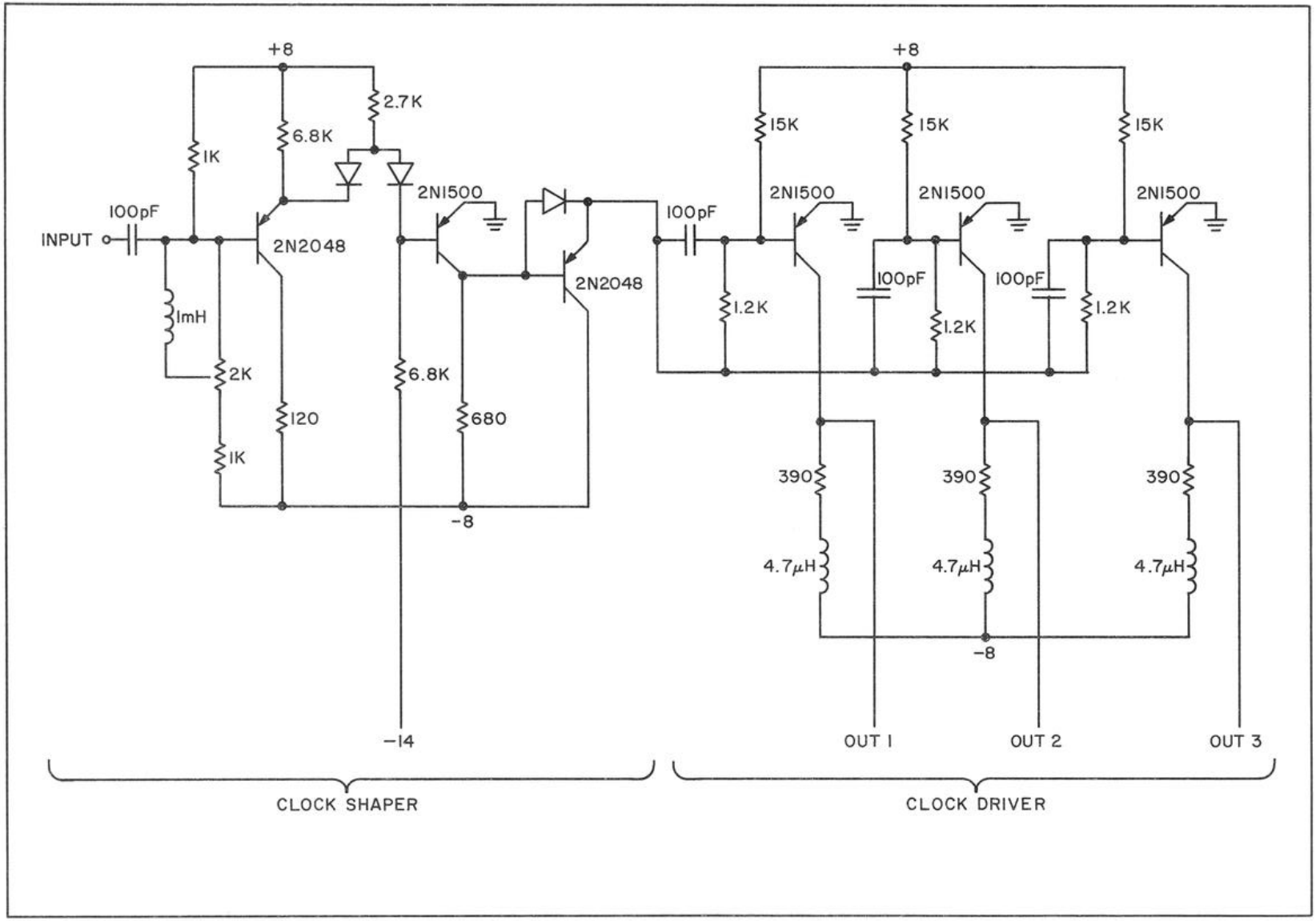


FIGURE 3-33. CLOCK SHAPER AND CLOCK DRIVER

Two types of OR gates are used. One is the counterpart of the diode AND gate, consisting of diodes, the anodes of which are joined at a gate resistor that is returned to a positive voltage (dc OR gate). This type of gate operates with less current than the AND gate (about 1/3 ma), and pnp emitter-follower circuits are used to obtain current gain. The emitter resistor can supply about 5 milliamperes into a load returned to negative voltage at the logic false (ground) level; therefore, a maximum of three AND gates can be driven from an emitter follower circuit. The other type of OR gate used consists of several trigger inputs into one flip-flop base (ac OR gate).

The type of circuitry described is implemented with different component types and values, depending on the frequency of operation and the supply voltages. Nominal 3-megacycle circuits, for operation with +8 volt (switch load supply, emitter follower collectors) and -14 volt (AND gates), are used on the TRICE computing modules. Similar circuits packaged on 15- and 35-pin plug-in modules, and designed for operation with +6 volt and -12 volt, are used in the TRICE control unit and buffer register, and in the PB250 Computer. Nominal 200-kilocycle circuits for +6 volt and -12 volt operation on 15- and 35-pin plug-in modules are also used in the control unit for application where switching is required only at the word rate of TRICE (100 kc) or the PB250 (83 kc).

Because of the trigger method used, the maximum switching rate can be obtained with a symmetrical square wave as clock signal. Up and down time of the clock signal must be at least 2.5 microseconds for the 200-kilocycle circuitry, and 0.16 microseconds for the 3-megacycle circuits.

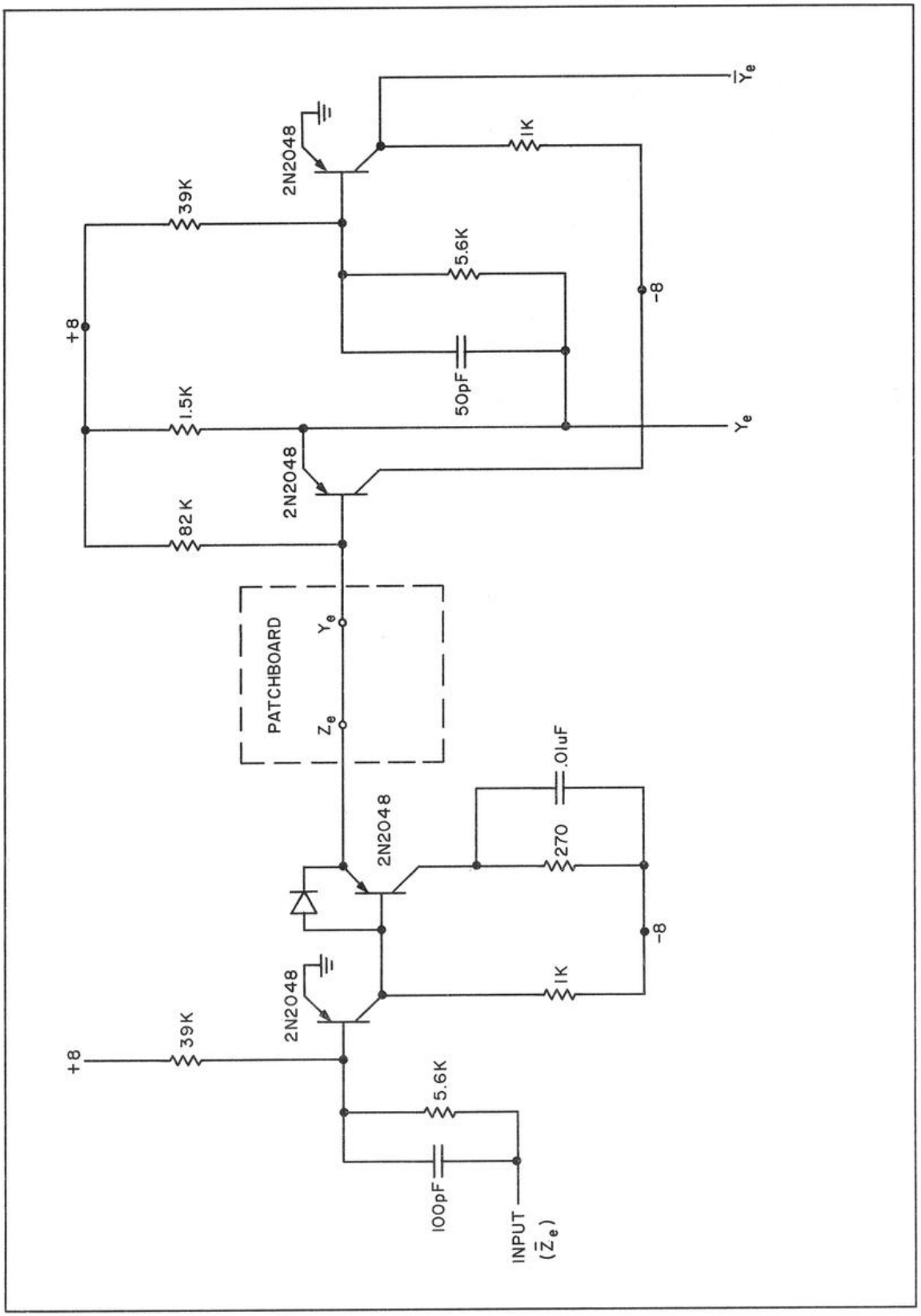


FIGURE 3-34. INPUT-OUTPUT AMPLIFIERS

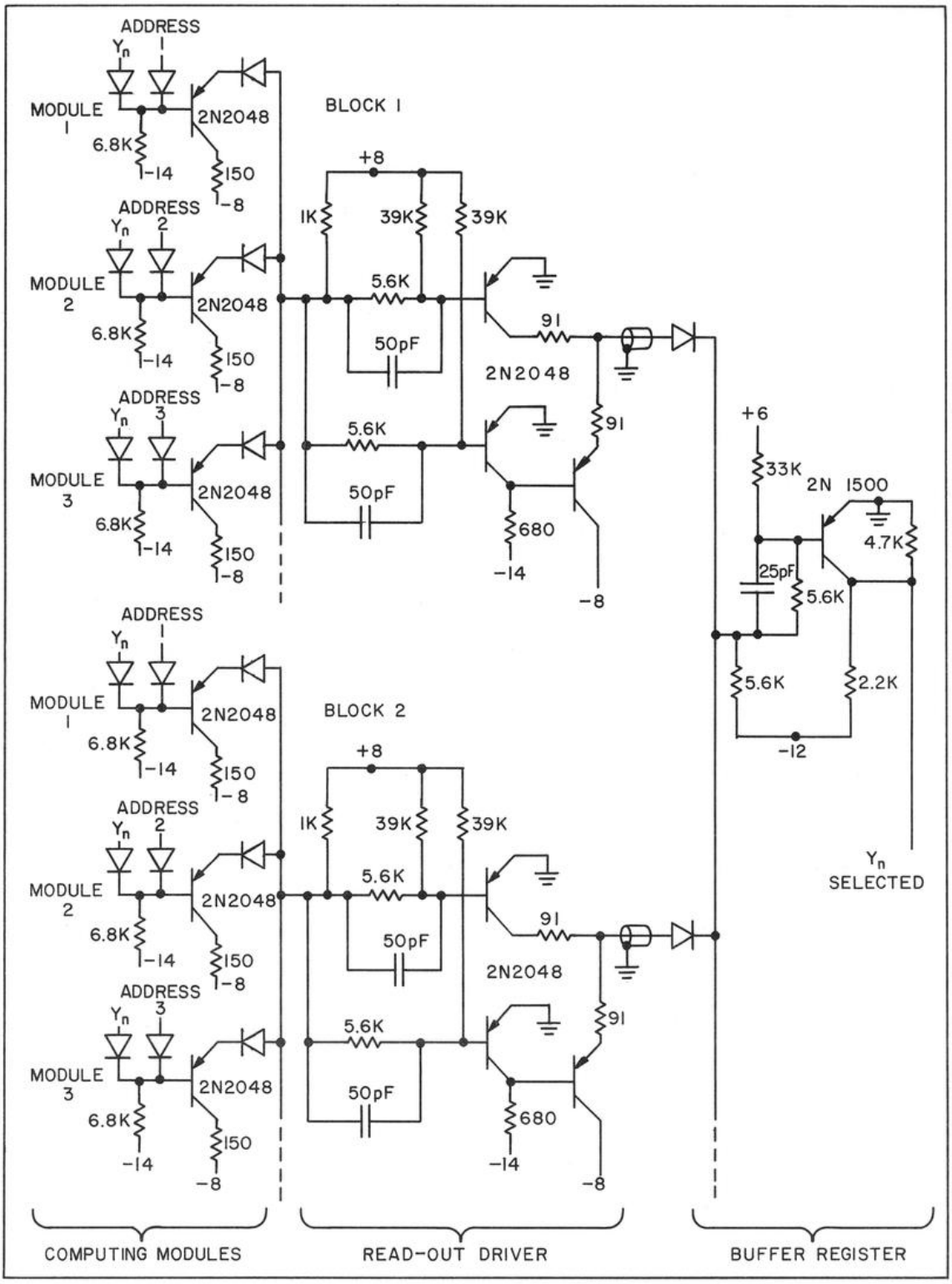


FIGURE 3-35. READ-OUT SELECTION GATE

E-2. MEMORY CIRCUITS (Figure 3-36)

In addition to flip-flop registers, recirculating delay line registers are used as memory elements in both TRICE and the PB250. Generally, a register consists of a write flip-flop driving the delay line input, a delay line, a read amplifier, the read trigger circuit, and a read flip-flop. Logic for changing the contents of the memory register is inserted between the read and write flip-flops. The delay lines are the acoustic type, with wire as the delaying medium, and transducers based on the magnetostrictive effect at the ends. For a longitudinal mode line, the characteristic delay is about 5 microseconds/inch. The circuits and operation of the one-word register lines used in the TRICE computing modules is described in the following paragraphs.

The delay line package, containing the wire used as a delaying medium, the read -- write coils with electrical terminations, the read amplifier, read trigger circuit, read flip-flop, and write circuit, are mounted on theMSR-5 printed circuit assembly. This assembly plugs into the main module board on the circuit side (inside the module chassis). The write flip-flop, and associated input gates, close the recirculating loop. The write flip-flop is located on the main board.

A clocked, non-return-to-zero digital pattern, with the levels 0 and -7 volt, is fed to the write RC from the write flip-flop collector. This write RC, in series with the write coil and coil termination, represents the collector load of the write flip-flop. Each transition in this waveform initiates a mechanical wave traveling along the wire. (A current change in the write coil causes a change in its magnetic field. This change, in turn, is translated into a change in mechanical tension in the wire by the magnetostrictive effect. This launches a mechanical wave in the wire.) At the receiving end, the mechanical

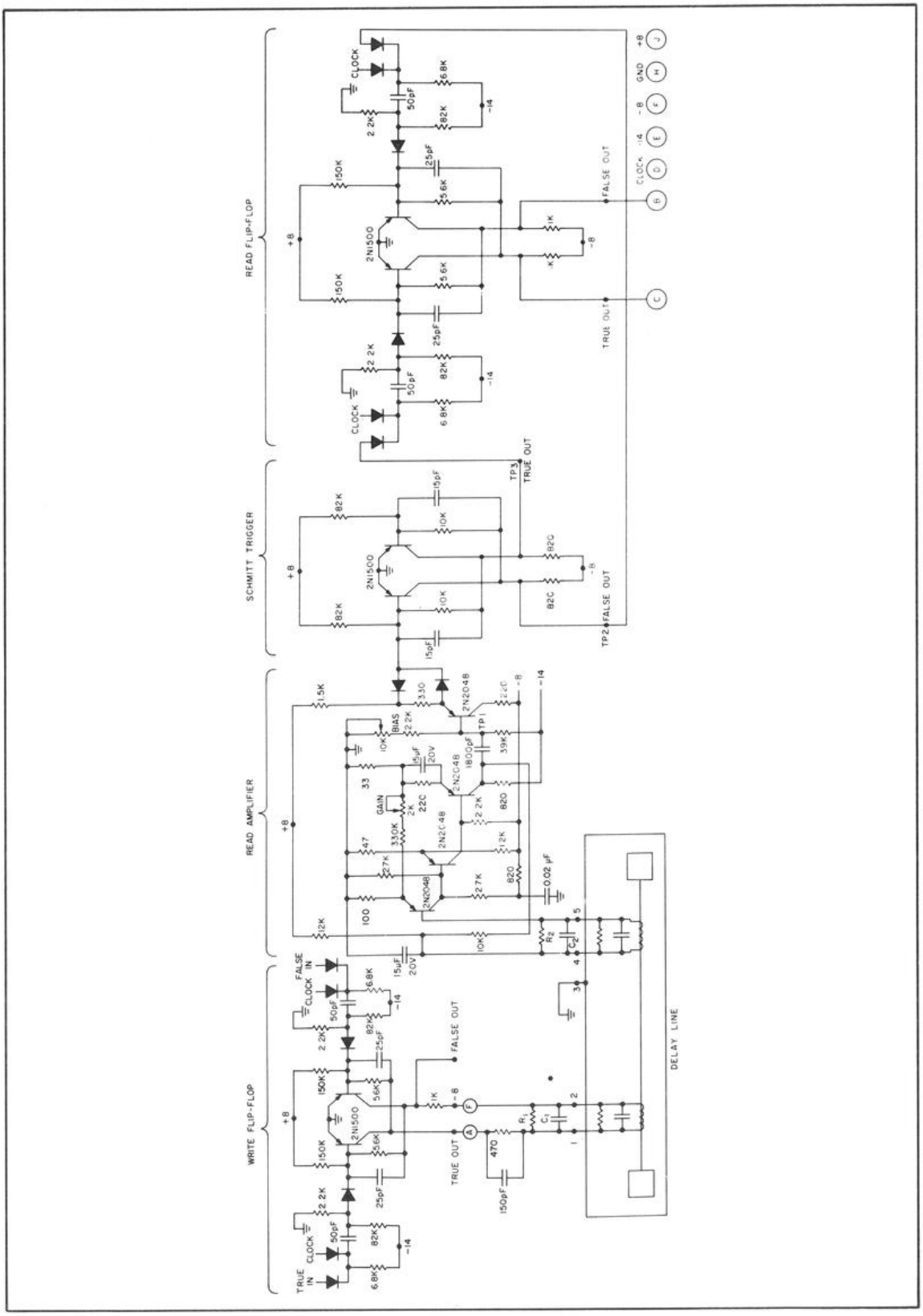


FIGURE 3-36. MAGNETOSTRICTIVE DELAY LINE REGISTER

wave momentarily changes the magnetic reluctance of the wire, which effects a change in the flux distribution of a polarizing magnet. This change in flux is sensed by the read coil, which generates an electrical signal (about 10-millivolt amplitude). The whole process involves two differentiations, so that a step change at the input causes a dipulse at the output. The output signal is amplified by the read amplifier (d-c coupled, gain controlled by negative feedback) to 2.2 volt amplitude. An emitter follower with an a-c coupled signal input allows bias adjustment. Then the signal triggers, by d-c coupling, a flip-flop (read trigger) to restore the non-return-to-zero pattern. Triggering takes place near the peak of the trailing half of the dipulse. The trigger circuit output is fed to the clocked input gate of the read flip-flop to restore synchronization with the module logic.

F. DECIMAL CONVERTER SCALER

The decimal converter scaler accepts decimal information from the character input of the TRICE console (keyboard or paper tape reader), applies a binary scale exponent, truncates the binary register to a specified length, adds a scaling bit and converts to binary form the contents of the decimal converter scaler for subsequent loading of a TRICE module or converter module with an initial value. During an output mode the decimal converter scaler converts a binary number received from a module register to the decimal equivalent, eliminates the scaling bit, applies a binary scaling exponent and a decimal magnitude exponent. The resulting decimal number is either displayed on a decimal readout or processed through the paper tape punch.

Auxiliary quantities such as decimal magnitude exponent, binary scale exponent and register length can be entered in decimal form, converted into binary form and stored until replaced by new values.

These stored quantities are also displayed on the console. A set of control codes, also entered through the character input, determine which operation is to be performed. In the display mode read-out and binary to decimal operations, conversions are initiated automatically at a 100 cps rate.

The decimal converter scaler consists of two logic module cases and a set of decimal and binary indicators on the control console. Input and output connections are made via the control unit to the keyboard, tape reader and tape punch.

The mechanization of the logic of the decimal converter scaler is built around a nine digit decimal register which may be shifted left or right and apply the necessary corrections to implement multiplication and division by 2 and 10. These basic steps permit binary and decimal exponents to be applied and binary to decimal and decimal to binary conversions to be performed. In applying exponents, the register is logically connected between the least and most significant digits and a marker register keeps track of the position of the most significant non-zero digit and separates the two ends of the number. For converting binary to decimal and decimal to binary the register operates open ended and its most significant end is connected to the binary data register which communicates with the computing and converter module registers. Conversion of data into and out of module registers operate on fractions. As a result, a decimal to binary conversion consists of successive multiplications by two in the decimal register. Overflows across the decimal point are the bits of the binary number, which is generated starting with the most significant bit. A binary to decimal conversion consists of successive divisions by 2 in the decimal register any binary bits shifted in across the decimal point until all binary bits are used up and the binary and decimal point coincide. All operations

in the decimal register are counted in an operation counter, which together with a set of control flip-flops starts and stops sequences of operations. This logic also controls the entering of the auxiliary quantities (decimal exponent, scale exponent and register length). All these quantities are entered in decimal form into the least significant end of the decimal register and converted to a fixed number of binary bits as whole numbers in absolute value and sign form. As they are converted, they are shifted into the proper binary register for storage.

F-1. DECIMAL DATA INPUT AND OUTPUT

The simplest mode of operation of the decimal converter scaler is input to and output from the decimal register of decimal digits and sign. For this mode, the control flip-flops (A1 through A5) are off. Digit information to be entered into the register comes from the digit register comprised of flip-flops Db1 through Db4 within the control unit accompanied with a shift clock Mc. Mc becomes the left shift signal Sm of the decimal register (flip-flops D18 through D91). Data is entered into D91 by way of term Ain, which contains Db4. Each digit generates four shift pulses, sequentially the four bits of the digit appear in Db4, most significant bit first, and are shifted into the least significant decade, flip-flops D98 through D91 of the decimal register. The contents of the most significant decade D18, D14, D12 and D11 flip-flops, is shifted out and lost. Information within the other decades is shifted left by one decimal position.

The sign is entered into the sign flip-flop Ds by a Spd clock pulse which is generated whenever a sign character is received during the DATA mode. The B1 signal, the least significant bit of the character input, selects between + and - . A data code entered in this mode appears in the decimal converter as clock pulse Fp and code Bco, combined to

Fpo. (Note: All control codes in the decimal converter scaler are treated in a similar manner. For example, Fp and Bc5 are combined to form Fp5.) Fpo turns on flip-flop A5. If flip-flops A1 and A2 are on, they are turned off. Flip-flop K follows flip-flop A5 and makes left shift signal Sm true. At the same time, $\overline{Us}$ signal is true by its $\overline{A2}$ $\overline{A1}$ term. Operation count signal Uc goes by its $\overline{A1}$ $\overline{A2}$ A5 term and left shifts in the decimal register and counts in the operation counter U1 through U8 occur, until U1 through U8 read a state corresponding to a count of 36 (U6 $\overline{U5}$ $\overline{U4}$ U3 $\overline{U2}$ $\overline{U1}$). Then the count clock Uc is disabled by $\overline{Ur}$. Ur through Uc clears the U counter and resets A5 and K. The details of the sequence are such that counts in the U counter occur for any state from 0 through 35, whereas shifts happen for U between 1 and 36. Since Db4 is cleared after processing each input digit, zero bits are entered into the decimal register during this automatic shift operation. The U counter also counts the shift pulses Mc, when a digit is entered. Since there are four pulses for each digit, U8 - U3 contain the count of digits and U2 and U1 count the bits of each digit. In normal operation the U counter starts at zero (it can be brought to this state by entering a data character). If then "n" digits are filled, the U counter counts to 4 n. Entering a data character then, will continue counting in the U counter and entering zeros until 36 counts, corresponding to 9 digits, have been made. This mechanizes the entering of trailing zeros. If data is entered with zero in the U counter, 9 zeros will be filled into the decimal register, that is it will be cleared to zero.

If a visual readout only is required operation of the decimal counter ceases after converting the number and applying decimal and scale exponents. The result is then held in the decimal register, until replaced by new information. For paper tape punch output, decimal

digits and sign are extracted from the decimal register and formed into complete character codes under control of the control unit and punch unit.

Flip-flop P, which turns the punch on, is turned on by control code PUNCH OUTPUT (Fp Bc7), also flip-flop A4 in the decimal converter. If the control logic is in the KEYBOARD mode ($\overline{U}\ \overline{W}$), Cp will start generating character pulses. The Cp flip-flop is partially controlled by the Rb signal generated by the reader punch unit. The timing circuits are common to both read and punch operations. That is, Cp = $\overline{Rb}$ P A4 $\overline{Kb}$. The $\overline{Kb}$ terms insures that the keyboard key PUNCH OUTPUT has returned to its off position before the punch starts operating. For the reader mode of the control logic punch and read cycles are common and mechanized through the terms $\overline{Rb}$ U $\overline{W}$. The control code Fp Bc7 = Fp7 inserts the proper character for the sign of the decimal number into the output register, comprised of flip-flops E1 through E6, and sets flip-flops A and D of the control unit to the state AD (PUNCH OUTPUT). Therefore, the contents of E1 through E6 appear on the punch input lines, M1 through M6, and the sign will be punched out on the first timing cycle for which the punch is on. Cp in the AD mode generates punch pulse Pp to prepare the next digit from the decimal register for output. Pp turns on K and this causes the U counter to be advanced by Uc signals and the decimal register to shift left whenever Sm signals are generated. When a count of 3 appears in the U counter, flip-flops U1 and U2 are true and flip-flop K is turned off. The digit is shifted out of the decimal register into the output register (E1 through E6) by shift clock pulses Ec. Flip-flop E1 through E4 contain the digit in BCD code. As each shift operation starts, E5 is turned off and E6 is turned on. This is the correct code for a zero, which remains in the E register if no one bits

are contained within the output digit. The first one bit that appears in case of a non-zero digit turns E6 off. Any further one bits in the output digit turns E5 on and off, alternately. This permits an odd parity bit to be generated. The overall sequence is such that as the sign is punched out, the first digit is put into the E register. The count in the U counter is four after that operation. When the eighth digit is punched out, the ninth digit is put into the E register and the count in the U counter is 36. This turns off the A4 flip-flop and resets the U counter. The Ec signal is inhibited and the ninth digit remains in the E register. During the KEYBOARD control mode, with flip-flop A4 off, Cp signals are inhibited and PUNCH OUTPUT is terminated. During the READER control mode, Cp signals are generated as long as the reader is on. Any Cp pulses occuring before the AD state is terminated will cause repeated punch out of the ninth digit from the decimal register. In normal operation punch out from the decimal register is terminated by a DATA code, which changes the mode AD to $\overline{A}\ \overline{D}$ (DATA) and connects the character input B1 through B6 to the punch input lines M1 through M6. Input codes will be duplicated on the output tape until an ADDRESS code (EpBc1) turns off flip-flop P which inhibits the punch out logic.

F-1a. Arithmetic Operation of the Decimal Converter Scaler

The decimal register consists of nine decades and each decade stores a decimal digit represented by four binary bits. Multiplication and division by 10 in this register consists simply in shifting the contents of one decade into the position of the next decade, that is, four shifts left or right. In the logic equations, signal Sm causes left shifts and signal Sd causes right shifts. Multiplication and division by 2 is required for binary to decimal and decimal to binary conversion and

multiplication and division by powers of 2 for scaling. It can be mechanized by shifting and correcting the results. A method that operates on each digit separately is used in the decimal converter scaler. In multiplication by 2, it is necessary to shift out at the most significant end of a decade a one bit if the contents of the decade is 5 or more. In this case, a value of 3 is added to the contents of the decade. After the shift, this added 3 acquires the value of 6. This is subtracted automatically because a bit shifted out at the most significant end has a weight of 16 but is entered into the next decade with a weight of 10. The logic for this change (addition of 3 in case the contents of decade is 5 or more) is controlled by signal Cm. The relationship of the decade for values of 0 through 9 before and after the addition of 3 and shift are illustrated in Table 3-6.

In case of division by 2 a right shift is made first and the correction second. When a one bit is shifted into the next lower decade (to the right), it enters it as if it had a weight of 16 before the shift and acquires a weight of 8 after the shift. It actually had a weight of 10 before the shift and should cause a value of 5 to be added to the next lower decade. To achieve this, a value of 3 is subtracted after the shift, if the contents of the decade is 8 or more. The logic for this operation is controlled by the signal Cd.

Table 3-7 illustrates the contents of two adjacent decades before and after the shift and subtraction.

F-2. DECIMAL TO BINARY CONVERSION OF AUXILIARY DATA (EXPONENTS)

To enter decimal exponents, scale exponents and register length, the value is first filled into the decimal register by the digit input logic. The decimal point is assumed at the least significant end of the

Table 3-6.

BINARY TO DECIMAL CONVERSION

Original Contents of Decade	Corrected Contents of Decade	
	Before Shift	After Shift
0	0	0
1	1	2
2	2	4
3	3	6
4	4	8
5	8	1.0
6	9	1.2
7	10	1.4
8	11	1.6
9	12	1.8

The decimal point indicates the separation of two successive decades.

Numbers larger than 9 before multiplication by 2 are improper.

Table 3-7. (Sheet 1 of 2)

DECIMAL TO BINARY CONVERSION

Original Contents	Contents After Shift	Contents After Subtraction
0.0	0.0	0.0
0.2	0.1	0.1
0.4	0.2	0.2
0.6	0.3	0.3

Table 3-7. (Sheet 2 of 2)

DECIMAL TO BINARY CONVERSION

Original Contents	Contents After Shift	Contents After Subtraction
0.8	0.4	0.4
1.0	0.8	0.5
1.2	0.9	0.6
1.4	0.10	0.7
1.6	0.11	0.8
1.8	0.12	0.9

decimal register. Decimal to binary conversion of this number is initiated by entering one of the control codes Fpl (decimal exponent), Fp2 (scale exponent), or Fp3 (register length). In all cases, flip-flop A3 is turned on and flip-flops Al and A2 will be set as follows:

Al $\overline{A2}$ for decimal exponent

$\overline{A1}$ A2 for scale exponent

Al A2 for register length

Since either Al or A2 is on for any of these states, flip-flop K is turned on and Uc signals are generated for the U counter. Alternately Sd signals, to permit right shifts of the decimal register, and Cd signals, to correct the right shift to a division by 2 in the decimal register, are enabled. During decimal exponent conversions, the Sd and Cd signals are generated until the U counter is advanced to 12. During a scale exponent conversion, these signals are generated until the U counter is advanced to 14 and during a register length operation, these signals are generated until the U counter is advanced to 10. As a

result, 6, 7, or 5 binary bits will be generated, respectively. As the bits appear at the least significant end of the decimal register, they are shifted into the decimal exponent register (flip-flops De1 through De6 by shift clock pulses Dec; shifted into the scale exponent register (Be1 through Be7) by shift clock pulses Bec; or into the register length register (Rℓ1 through Rℓ5). The sign of the decimal register, contained within flip-flop Ds, is transferred into the sign bit flip-flop Des of the decimal exponent register with an Fp1 code or to the sign bit flip-flop Bes of the scale exponent register with an Fp2 code. The register length register does not require a sign bit. Information for the exponent and register length is converted to binary and stored in this form to simplify the logic for comparing during the conversion of data the value of exponent or register length with the count in the U counter.

F-3. DECIMAL TO BINARY CONVERSION OF DATA (INPUT)

The decimal to binary conversion of input data starts by entering the decimal value into the decimal register via the digit input logic. Any exponent or register length information must be stored prior to this operation. The sequence of conversion is initiated by control code CONVERT INPUT (Fp Bc5 = Fp5). Flip-flops A1 and A2 are turned on and flip-flop K follows at one clock pulse later. Uc signals are generated to advance the U counter until such time as the Ur signal becomes true. The Ur signal causes a Ucℓ signal to be generated and flip-flops A1, K, and the U counter are reset. The Ur signal goes true by the $\overline{A3}$ (A2 A1) Ube terms. The Ube term means that the U2 through U8 configuration agrees with the Be1 through Be7 configuration. That is, the count within the U counter equals the count within the binary exponent register. During an A1 A2 mode, the Us term permits the sign

of the exponent register Bes to be read. Depending upon Us, either Cm and Sm for positive sign or Sd and Cd for negative sign are alternately enabled. The Sd, Cd sequence causes division by two in the decimal register; the Sm-Cm sequence causes multiplication by two. There are two steps for each factor of two and the U2 through U8 flip-flops of the U counter count the number of times that a factor of two is applied. The count within the U2 through U8 flip-flops is compared with the stored scale exponent and operation stops when the two values are equal. A Ucℓ signal terminates the application of the scale component, turns off flip-flop A1, which changes the mode of the decimal converter to application of decimal exponent. That is, the mode flip-flops A1 and A2 are changed from a A1 A2 configuration to an $\overline{A1}$ A2 configuration.

The Uc signal is subsequently enabled and flip-flop K is turned on again until the Ur signal goes true. This time Ur goes true by the $\overline{A3}$ (A2 $\overline{A1}$) Ude terms. The Ude signal is true whenever the configuration of the U3 through U8 flip-flops is equal to the configuration of the De1 through De6 flip-flops of the decimal exponent register.

During the $\overline{A1}$ A2 mode, the Us signal permits the sign of the decimal exponent register Des to be read. Depending upon the Us signal, either Sm for positive sign or Sd for negative sign is enabled. The decimal register is shifted left or right, accordingly. There are four shifts for a factor of 10 and flip-flops U3 through U8 count the number of times that a factor of 10 is applied. The contents of the U3 through U8 flip-flops is compared with the contents of the decimal exponent register. When the value within the U counter is equal to the decimal exponent register, the Ur signal becomes true and Ucℓ signal is generated which resets the U counter and the K and A2 flip-flops to terminate the operation.

During the two previous operations, a marker register, comprised of flip-flops C1 through C9, is used in the following manner. At the start of applying the scale exponent, flip-flop C1 is set by the Cin term. This marker then follows the most significant non-zero digit in the decimal register by means of the Cℓ and Ck terms. The Cℓ term shifts the marker to the left to a lower numbered C flip-flop corresponding to a lower numbered decade of the decimal register. The Ck term shifts the marker to the right. The Cℓ term goes true whenever there is a left shift in the decimal register, as indicated by the Sm term, and there is an eight bit in the decade containing the marker. That is, whenever the most significant non-zero digit enters the next decade to the left. The Cℓ term then clears the contents of the 8, 4, and 2 bits of that decade and inhibits shifting into these stages. The one bit receives the bit from the 8 bit stage of the next lower decade at the same time. The Ck term goes true when the 8, 4, and 2 bits of the decade containing the marker are zero and there is a right shift in the decimal register. At that time both the marker and the one bit of the most significant non-zero digit leave the decade. As long as the marker is in a particular decade, only zeros can be shifted in from the next more significant decade. As long as flip-flop A2 is true, that is, during applying scale exponent and decimal exponent, the ends of the decimal register are connected by the $\overline{A3}$ A2 terms of Ain, which goes to the input of D91, the least significant stage of the least significant decade, and the $\overline{A3}$ A2 term of the D18 input, the most significant stage of the most significant decade. After applying the decimal exponent, the marker is still within the C register. The marker has to be moved to the decimal point and clear the least significant end of the scaled number. That is, between the most significant end and the decimal point. For that purpose the Cℓ term is enabled by the $\overline{C0}$ $\overline{C1}$ $\overline{A2}$ terms.

The Cℓ signal remains true as long as the marker is in any stage but C1. As the marker moves toward the most significant end of the register, the decades ahead of the marker are cleared, including the one bit stage of each decade since the Sm signal is not true whenever Cℓ is true. When the marker is in the C1 flip-flop, the Cℓ signal goes false and the ninth decade is not cleared. C1 flip-flop is turned off by the C1 T5 $\overline{A2}$ terms and the marker disappears.

At the same time, the $\overline{A2}$ $\overline{A1}$ C1 terms turn on the A1 flip-flop to start the decimal to binary conversion into the binary data buffer register. The Uc signal is generated and the U counter is advanced and the K flip-flop is turned on. These conditions prevail until the U counter reaches a count of 58 (U6 U5 U4 $\overline{U3}$ U2 $\overline{U1}$). At that time the Ur signal becomes true and the subsequent Uc signal resets the U counter and the K and A1 flip-flops. The operation is terminated and the decimal converter scaler returns to the idle state. During the time that the K and A1 flip-flops are on, Cm and Sm signals are enabled alternately ($\overline{Us}$ is true by the $\overline{A3}$ $\overline{A4}$ ($\overline{A2}$ A1) terms). The data is multiplied by two for each Cm and Sm sequence. Every Sm signal shifts a new binary bit of the converted number out of the most significant end of the decimal register. These bits or their complements, if flip-flop Ds is on, are gated to form a Coc signal. Note: If Ds flip-flop is on, the sign of the decimal register is negative. A clock pulse Cop is generated for each bit simultaneously with the Sm signal. Coc and Cop signals are fed to the binary data register by means of the Bic and Bip signals. The first Cop pulse appears before the K flip-flop is set true. That is, before any binary bits have been generated. At that time the sign of the decimal register appears in the Coc signal to be entered into the binary data register preceding the bits of the number. A bit is generated for each two counts of the U counter until the configuration of the

U2 through U6 flip-flops agrees with the configuration of the Rℓ1 through Rℓ5 flip-flops of the register length register. At that time the Urℓ signal goes true and the K flip-flop is turned off to inhibit any further outputs from the decimal register. At the same time, an Sb flip-flop is turned on for one clock pulse time to permit a scaling bit to be generated. Thereafter only zeros appear on the Coc line to fill the least significant end of the binary data register with zeros.

F-4. BINARY TO DECIMAL CONVERSION OF DATA (OUTPUT)

The mode, in which information from the binary data register is converted for decimal read-out or punch-out, is selected by flip-flop A4. This flip-flop is turned on by control code CONVERT OUTPUT (Fp6 = Fp Bc6). The Fp6 signal also turns on flip-flop A1 to start the binary to decimal conversion. The Uc signal is enabled, the U counter starts to count and the K flip-flop is turned on. This condition prevails until the Ur signal becomes true when the U counter has been advanced to a count of 58. A subsequent Ucℓ signal resets the U counter, turns off the K flip-flop and turns on the A2 flip-flop. The scale exponent is applied after the A2 flip-flop is turned on. During the time that flip-flops A1 and K are on, Sd and Cd signals are generated alternately ($\overline{\text{Us}}$ is false for output operations). Each sequence of Sd and Cd signals divides the contents of the decimal register by 2. Binary bits from the binary data register are obtained with a Bop clock pulse. Each time the Bop signal is true, an Sg signal is turned on for one 3 megacycle clock time at P16 time and the binary data register is shifted one position to the right. The least significant end of the register is connected to the most significant end of the register. Output bits are read from the most significant stage or flip-flop Rd1 of the binary data register. Before the first Bop pulse is generated, the Rd1

flip-flop contains the sign of the binary number. The sign bit is transferred by a control code Fp6 into the Ds flip-flop of the decimal register. Depending upon Ds, a Boc signal or its complement appears on Bin and is shifted into the most significant end of the decimal register during the time that its content is being divided by 2 by the Sd and Cd sequence. Initially flip-flop Sb is off and no bits are entered into the decimal register. Sb is turned on by the first true bit appearing on Boc, the scaling bit. All bits thereafter are entered into the decimal register until the conversion process in terminated by the Ur signal. Excluding the sign bit, 29 bit positions of the binary register are scanned. However, 30 shifts are performed so the contents of the binary register retains its original configuration. Following the binary to decimal conversion the scale exponent and the decimal exponent are applied by the same logic and sequence as during the input conversion. The sign of the exponents are inverted in the Us equations, this effectively reverses the scaling done on the input information. At the end of the operation applying the decimal exponent, when the marker bit reaches flip-flop C1, flip-flop A4 is turned off and the decimal converter scaler returns to the idle state.

In the DISPLAY mode flip-flop Dip is true for one 100 kc clock pulse time every 10 milliseconds as controlled by the free running multivibrator Sr. The Dip signal causes a Fpo signal to be generated to produce a simulated control code DATA (FpBco). This initiates a clear pulse cycle of the decimal register. During the clear cycle the binary data buffer register reads the contents of the selected module register. At the end of the clear cycle, signal Fp6 is generated to produce a simulated control code CONVERT OUTPUT (FpBc6) which starts the convert output sequence.

G. PB250 CONNECTIONS

The connections between TRICE and a PB250 computer are accomplished by permitting the following PB250 commands to be executed; PTU, BSO, BSI, and TES.

G-1. PTU COMMANDS

Five code lines (L1 through L5) enter the control unit of the TRICE as B1 through B5 in the computer control mode (UW). An additional code signal B6 is always true in this mode. Cpg is the synchronizing clock pulse generated by the computer. It takes the place of the internal clock pulse Cp and becomes Bp. Signals B1 through B6 and Bp are used in the same manner as control codes originating in Keyboard or Reader.

G-2. BSO COMMANDS

PTU signals are not sufficient to control the TRICE. BSO signals are used to enter data and addresses into the control section. For this operation, address and data registers are connected in series. The TRICE has to be in the Computer control and Address modes. Signal Es enables the input from the computer into the address register. Shift mask Gsg controls the shift clock Cℓ2. Data input to the register is signal Gdg.

G-3. BSI COMMANDS

Information from the data register is fed to the computer through BSI commands. Signal Es must be true, and Hsg is the shift mask controlling clock pulse Cℓ2. Data output comes from the least significant end of the data register as signal Hdg.

G-4. TES COMMANDS

TES signals are divided in four groups. The first two groups (TES 00 through 07 and 10 through 17) are connected to the patchboard. All four groups (TES 00 through 07, 10 through 17, 20 through 27, and 30 through 37) can be connected to switches. (Switchbox mounted near the Flexowriter on the table). No TES signal is connected to the TRICE control.

H. CONVERTERS

The converters operate on an incremental basis. Their inputs and outputs are connected as Ye, Ys and Ze, Zs respectively to the patchpanel.

Conversion process is synchronized with the TRICE operation by means of pulse Cvc (100 K cps or 131 · 072 K cps depending on TRICE word length). The pulse covers pulse-times P23 and P24 and is turned on in the Integrate and Halt modes. Each converter contains an input-output buffer. Data input to this buffer register is signal If; data output signal is CV. Fill and read operations are synchronized by shift pulse Csc and a converter address must be selected. A transfer of contents of the converter counter into the buffer register takes place upon command Cro. Signal Cro comes automatically with each read-out.

Setting the converter counters from the buffer register is executed upon signal Cri. A signal Cri is generated whenever a total reset (Rt) is activated in the TRICE control unit and a converter address is selected. A signal Cre, generated simultaneously with Cri, resets the overflows in the converters.

Refer to CSP159 for further details on the converter modules.

I. READER PUNCH UNIT TRP1

I-1. GENERAL

The reader punch unit consists of a 60 character per second paper tape reader, a 60 character per second paper tapepunch, a timing and control logic chassis and power supplies. These components are mounted within a desk height cabinet on casters. The reader punch unit is self contained and is used on line with the TRICE console to allow paper tape inputs and outputs; or used off line to duplicate paper tapes; or used on line with the PB250 computer. In the latter case, the signal cable of the reader punch unit is connected to J18 of the PB250 and a special input-output program is used within the PB250. Table 3-8 lists and describes the various controls and indicators of the reader punch unit.

I-2. TIMING AND CONTROL

The reader and punch unit is an asynchronous device. As such, each operation must be automatically synchronized in respect to the associated input or output device. Successive operations may be initiated at any time providing the time interval between successive operations does not exceed 60 characters per second rate.

The reader cycle requires a 4.5 millisecond pulse to energize the reader forward step coil. The reader contacts change state beginning 7 milliseconds and ending 14 milliseconds after the beginning of the step pulse. Although the state of the reader contacts can be read into the logic circuits at any time outside of the time interval of change, the state of the reader contacts are read just preceding the step pulse by the clock pulse that initiates the step pulse.

Table 3-8.

READER PUNCH UNIT CONTROLS AND INDICATORS

Power Light	On	
Punch	On	Turns on punch motor and logic, enables external code inputs to punch
	Ext	Places punch motor and logic under external control
Motor	On	Turns on punch motor (overriding punch switch)
	Ext	Places punch motor under control by punch switch or external input
Leader		Turns on punch motor and enables punch logic to punch blank tape, starts timing cycle
Clear		Turns on punch motor and enables punch logic to punch blank tape, sets up one "all one" character and starts timing cycle
Reader	On	Turns on reader motor and logic, enables code outputs from reader
	Ext	Places reader motor and logic under external control
Motor	On	Turns on reader motor (overriding reader switch)
	Ext	Places reader motor under control by reader switch or external input
Clock	On	Enables selfsustaining timing cycle
	Off	Disables selfsustaining timing cycle
	Ext	Connects external input to start timing cycle
Start		Starts Timing Cycle

The punch cycle requires simultaneous or parallel pulses of 4.5 millisecond duration to energize the desired code level coils and sprocket and step switch coil. Note: Tape movement is controlled by internal circuits of the punch unit which insure an adequate delay after each character is punched.

The timing logic of the reader punch unit is common to the reader and to the punch. Each cycle of operation is comprised of three phases: A clock pulse phase of 10 to 20 microseconds during which information is read from the reader contacts or from the punch input lines into the punch register, an energizing pulse phase of 4.5 milliseconds during which the reader step coil or the punch code coils are energized, and a delay pulse phase of 12.5 milliseconds. A busy signal is generated during the latter two phases to prevent a new cycle of operation from being initiated until the previous operation is properly terminated. The clock pulse is obtained from an external source such as TRICE control unit or PB250 computer or generated internally immediately after the delay pulse.

The punch and reader are turned on manually by switches on the reader punch control panel or automatically in response to signals received from associated equipment. The motor of either unit can be turned on separately by a manual switch without turning on the logic of the unit. Whenever a motor is turned on, a delay is inserted into the timing cycle to allow the motor to reach operating speed. During this delay, the busy signal is generated to inhibit external inputs.

Depressing the CLEAR pushbutton causes the punch to be turned on, initiates a timing cycle and inserts a character into the punch

register in which all the bits are true. The CLEAR switch is depressed whenever the punch mechanism has been mechanically tripped but unable to complete the operating cycle.

Depressing the LEADER button turns the punch on and initiates a timing cycle. This operation is comparable to the CLEAR operation with the exception that no character is inserted into the punch register.

During CLEAR or LEADER operations, timing cycles will continue if the clock switch is in the ON position. Timing cycles are also initiated by the START button.

The timing cycle is generated by three one-shots, designated as Nc, Np, and Nd. During EXTERNAL clock mode operations, the Np one-shot is triggered by the character clock pulse Cp of the TRICE control unit or a Cog (WOC command execute signal of PB250) pulse if the reader punch unit is connected to a PB250 computer. During self sustaining clock modes of operation (when clock switch is in the ON position), the Np one-shot is triggered by the Nc signal, which takes the place of Cp in the logic. During the latter case, timing cycles are started by the CLEAR, START or LEADER pushbuttons, all of which trigger the Np one-shot. Note: The symbol for the signal generated by the CLEAR button is (Ns). The symbol for the signal generated by the START button is (S).

The resulting Np signal is gated with a Mo' or a Ro signal to generate a Nr signal which produces an energizing pulse for the reader or punch coil. The Ro signal, which enables the reader logic, is true when the READER switch is ON or due to Rℓ or Fℓ signals received from an external unit. When the reader punch unit is connected to the TRICE, the Rℓ signal is true whenever the READER mode ($\overline{UW}$) is selected. When the reader punch unit is used with the PB250 computer,

the Rℓ signal is controlled by the fast reader enable line (RfTf). This line is made true by a RFU command and made false by a DIU command. The Fℓ term permits the reader punch unit to work in conjunction with the bootstrap logic of the PB250. The Mo' signal, which enables the punch logic, is true during normal punch operations, during the time that the LEADER switch is depressed and during the times that the CLEAR switch is depressed. During normal punch operations, the Mo' signal is true if the PUNCH switch is in the ON position or upon receipt of a Mℓ signal from the TRICE. Note: The Mℓ signal is an output from the P flipflop.

Reader and punch motors are turned on by Rm and Mn signals, respectively. The Rm and Mn signals, in turn, are controlled by the enabling signals Ro and Mo' or by corresponding motor switches independently. Whenever Rm or Mm signals go true, the Nm oneshot is triggered and stays on for about 200 milliseconds. This delay allows the motors to reach operating speed.

The trailing edge of the Np oneshot pulse triggers the Nd oneshot to generate a delay until the reader or punch is ready to execute another cycle of operation. Signals from the Np, Nd and Nm oneshots are gated together to form a busy signal Rb which appears on senseline 32_8. The PB250 checks the status of the reader punch unit by executing TES commands. The trailing edge of the Nd oneshot pulse always triggers the Nc oneshot. The trailing edge of the Nc oneshot pulse triggers the Np oneshot to start a new timing cycle only if the clock switch is in the ON position.

The reader code output lines R1 through R8 are generated by the reader contacts and enable line Ro. The punch code coils are energized from punch register N1 through N8 and punch pulse Nr (where

Nr = NpMo'). The Nr signal also directly energizes the sprocket and feed coils of the punch unit. External input codes are entered into the punch register from lines M1 through M8 with clock signal Mp, which is generated by an internal clock Nc or an external clock Cp in conjunction with a punch enable signal Mσ. The Mo signal is true when the PUNCH switch is in the ON position or if the external input line Mℓ is true. (The Mo signal is comparable to the Mo' signal with the exception the Mo signal is not made true by the CLEAR or LEADER switches). The punch register N1 through N8 is cleared by the trailing edge of the Np oneshot pulse. During CLEAR operations, the punch register is loaded with all ones when the CLEAR switch is pressed. (Signal (Ns)).

I5 LOGIC

$$yd = Go\ \overline{R}\,[(Yr\ \overline{I4})\ Ye1\ \overline{Ye2} + (Yr\ \overline{I4})\ \overline{Ye1}\ Ye2 + (I4\ \overline{I2})\ (Ye1\ Ys1)\ (Ye2\ Ys2) + (I4\ \overline{I2})\ Ye1\ \overline{Ys1}\ Ye2\ \overline{Ys2} + A\ (Yr + I4)\ Ya]$$

Yd

$$oyd = Yd\,[(Ye1\ Ys1) + (Ye2\ Ys2) + A\overline{Ya} + \overline{I4}]$$

$$yn = \overline{Go}\ \overline{I_s}\ Yr\ \overline{Yd}\ \overline{Yc} + \overline{R}\ \overline{Is}\ Yr\ \overline{Yd}\ \overline{Yc} + I4\ \overline{Yr}\ Yd\ \overline{Yc} + I4\ \overline{Yr}\ \overline{Yd}\ Yc + Yr\ Yd\ Yc + Go\ R\ Ir + Is\ Ir$$

Yn

$$oyn = (\overline{yn})$$

$$yc = Yr\ Yd$$

Yc

$$oyc = \overline{Yr}\ \overline{Yd}$$

$$Y\Delta = (E)\ Yd + (I)\ \overline{Yd}$$

$$Yt = I2\ Xe\ Yn$$

$$yu = Yt\ \overline{Y\Delta}\ \overline{Yh} + \overline{Yt}\ Y\Delta\ \overline{Yh} + \overline{Yt}\ \overline{Y\Delta}\ Yh + Yt\ Y\Delta\ Yh$$

Yu

$$oyu = (\overline{yu})$$

$$yh = I4\ Yt\ Y\Delta + (I)\ (Yr\ \overline{I4})$$

Yh

$$oyh = \overline{Yt}\ \overline{Y\Delta}\ Yh + \overline{I4}\ Yh$$

$$Yv = I1\ Xs\ Yu + I1\ \overline{Xs}\ \overline{Yu}$$

$$rn = \overline{Go}\ Rr\ \overline{Yv}\ \overline{Rc} + \overline{R}\ Rr\ \overline{Yv}\ \overline{Rc} + I2\ \overline{Rr}\ Yv\ \overline{Rc} + I2\ \overline{Rr}\ \overline{Yv}\ Rc + Rr\ Yv\ Rc + Go\ R\ I4$$

Rn

$$orn = (\overline{rn})$$

$$rc = Rr\ Yv + (I4\ \overline{I2})\ \overline{Xs}$$

Rc

$$orc = \overline{Rr}\ \overline{Yv}\ Rc$$

$$P2 = \overline{I2}\ I1$$

$$P1 = \overline{I4}\ I2$$

$$ze = P2\ \overline{Yv}\ Rc + P2\ Yv\ \overline{Rc}$$

Ze

$$oze = P2\ \overline{Yv}\ \overline{Rc} + P2\ Yv\ Rc + R$$

$$zs = P2\ \overline{Yv}\ Rc$$

Zs

$$ozs = P2\ Yv\ \overline{Rc} + R$$

$$of = P30\ \overline{Yr}\ \overline{Yd}\ Yc + P30\ Yr\ Yd\ \overline{Yc} + P1\ \overline{Yt}\ \overline{Y\Delta}\ Yh + P1\ Yt\ Y\Delta\ \overline{Yh}$$

Of

$$oof = R$$

$$in = \overline{F}\ \overline{Fs}\ \overline{Is}\ Ir + \overline{Go}\ \overline{Fs}\ \overline{Is}\ Ir + Go\ F\ I1 + Fs\ If + Is\ Yr$$

In

$$oin = \overline{(in)}$$

$$i4 = (Yr\ \overline{I4})\ Go\ \overline{F} + Go\ F\ Ir + \overline{Go}\ F\ Ix$$

I4

$$oi4 = P30\ \overline{F} + Go\ F\ \overline{Ir}$$

$$i2 = Go\ \overline{R}\ I4 + \overline{Go}\ F\ Iy$$

I2

$$oi2 = Go\ \overline{I4} + \overline{F}\ \overline{I4}$$

$$i1 = Go\ \overline{R}\ \overline{F}\ I4 + Go\ F\ I2 + \overline{Go}\ F\ Iz$$

I1

$$oi1 = Go\ \overline{I2}\ I1 + \overline{F}\ \overline{I2}\ I1$$

$$go = P30\ G1\ \overline{\overline{F}\ \overline{G}\ \overline{R}}$$

Go

$$ogo = P30\ \overline{G1}$$

$$yv = I2\ Xe\ Xs\ Yn + I2\ Xe\ \overline{Xs}\ \overline{Yn}$$

Yv

$$oyv = (\overline{yv})$$

$$rn = \overline{Go}\ Rr\ \overline{Yv}\ \overline{Rc} + \overline{R}\ Rr\ \overline{Yv}\ \overline{Rc} + I2\ \overline{Rr}\ Yv\ \overline{Rc} + I2\ \overline{Rr}\ \overline{Yv}\ Rc + Rr\ Yv\ Rc + Go\ R\ I4$$

Rn

$$orn = (\overline{rn})$$

$$rc = Rr\ Yv + I2\ \overline{I1}\ Xe\ \overline{Xs}$$

Rc

$$orc = \overline{Rr}\ \overline{Yv}\ Rc$$

$$P2 = \overline{I2}\ I1$$

$$ze = P2\ \overline{Yv}\ Rc + P2\ Yv\ \overline{Rc}$$

Ze

$$oze = P2\ \overline{Yv}\ \overline{Rc} + P2\ Yv\ Rc + R$$

$$zs = P2\ \overline{Yv}\ Rc$$

Zs

$$ozs = P2\ Yv\ \overline{Rc} + R$$

$$yn = \overline{F}\ \overline{Fs}\ Yr + \overline{Go}\ \overline{Fs}\ Yr + Go\ F\ I1 + Fs\ If$$

Yn

$$oyn = (\overline{yn})$$

$$i4 = Yr\ \overline{I4}\ Go + \overline{Go}\ F\ Ix$$

I4

$$oi4 = P30\ \overline{F} + Go\ F\ \overline{Yr}$$

$$i2 = Go\ \overline{R}\ I4 + \overline{Go}\ F\ Iy$$

I2

$$oi2 = Go\ \overline{I4} + \overline{F}\ \overline{I4}$$

$$i1 = Go\ \overline{R}\ I2 + \overline{\overline{Go}\ F\ Iz}$$

I1

$$oi1 = Go\ \overline{I2} + \overline{F}\ \overline{I2}$$

$$go = P30\ G1\ (\overline{\overline{F}\ \overline{G}\ \overline{R}})$$

Go

$$ogo = P30\ \overline{G1}$$

$$xd = Go\ \overline{R}\ (Yr\ \overline{I4})\ Xe$$

Xd

$$oxd = Xd\ Xs + Xd\ \overline{I4}$$

$$xn = \overline{Go}\ Xr\ \overline{Xd}\ \overline{Xc} + \overline{R}\ Xr\ \overline{Xd}\ \overline{Xc} + I4\ \overline{Xr}\ Xd\ \overline{Xc} + I4\ \overline{Xr}\ \overline{Xd}\ Xc + Xr\ Xd\ Xc + Go\ R\ Irx$$

Xn

$$oxn = (\overline{xn})$$

$$xc = Xr\ Xd$$

Xc

$$oxc = \overline{Xr}\ \overline{Xd}$$

$$yd = Go\ \overline{R}\ (Yr\ \overline{I4})\ Ye$$

Yd

$$oyd = Yd\ Ys + Yd\ \overline{I4}$$

$$yn = \overline{Go}\ Yr\ \overline{Yd}\ \overline{Yc} + \overline{R}\ Yr\ \overline{Yd}\ \overline{Yc} + I4\ \overline{Yr}\ Yd\ Yc + I4\ \overline{Yr}\ \overline{Yd}\ Yc + Yr\ Yd\ Yc + Go\ R\ Iry$$

Yn

$$oyn = (\overline{yn})$$

$$yc = Yr\ Yd$$

Yc

$$oyc = \overline{Yr}\ \overline{Yd}$$

$$xy = I4\ \overline{R}\ Ye\ Ys\ Xr + I4\ \overline{R}\ Ye\ \overline{Ys}\ \overline{Xr}$$

Xy

$$oxy = (\overline{xy})$$

$$Yx = I2\ Xe\ Xs\ Yn + I2\ Xe\ \overline{Xs}\ \overline{Yn}$$

$$yv = (Yx\ \overline{Xy}\ \overline{Yh} + \overline{Yx}\ Xy\ \overline{Yh} + \overline{Yx}\ \overline{Xy}\ Yh + Yx\ Xy\ Yh)\ I2$$

Yv

$$oyv = (\overline{yv})$$

$$yh = Yx\ Xy + I4\ \overline{I2}\ Xe\ \overline{Xs}$$

Yh

$$oyh = \overline{Yx}\ \overline{Xy}\ Yh$$

$$rn = \overline{Go}\ Rr\ \overline{Yv}\ \overline{Rc} + \overline{R}\ Rr\ \overline{Yv}\ \overline{Rc} + I2\ \overline{Rr}\ Yv\ \overline{Rc} + I2\ \overline{Rr}\ \overline{Yv}\ Rc + Rr\ Yv\ Rc + Go\ R\ I4$$

Rn

$$orn = (\overline{rn})$$

$$rc = Rr\ Yv + I2\ \overline{I1}\ Ye\ \overline{Ys}$$

Rc

$$orc = \overline{Rr}\ \overline{Yv}\ Rc$$

$$P2 = \overline{I2}\ I1$$

$$P1 = \overline{I4}\ I2$$

$$ze = P2\ \overline{Yv}\ Rc + P2\ Yv\ \overline{Rc}$$

Ze

$$oze = P2\ \overline{Yv}\ \overline{Rc} + P2\ Yv\ Rc + R$$

$$zs = P2\ \overline{Yv}\ Rc$$

Zs

$$ozs = P2\ Yv\ \overline{Rc} + R$$

$$of = P30\ \overline{Xr}\ \overline{Xd}\ Xc + P30\ Xr\ Xd\ \overline{Xc} + P30\ \overline{Yr}\ \overline{Yd}\ Yc + P30\ Yr\ Yd\ \overline{Yc} + P1\ \overline{Yx}\ \overline{Xy}\ Yh + P1\ Yx\ Xy\ \overline{Yh}$$

Of

$$oof = R$$

$$go = P30\ G1[\overline{\overline{(\overline{Fx}\ \overline{Fy})}\ \overline{G}\ \overline{R}}]$$

Go

$$go = P30\ \overline{G1}$$

$$inx = \overline{Fx}\ \overline{Fsx}\ Irx + \overline{Go}\ \overline{Fsx}\ Irx + Go\ Fx\ I1 + Fsx\ I_f$$

Inx

$$oinx = (\overline{inx})$$

$$iny = \overline{Fy}\ \overline{Fsy}\ Iry + \overline{Go}\ \overline{Fsy}\ Iry + Go\ Fy\ I1 + Fsy\ I_f$$

Iny

$$oiny = (\overline{iny})$$

$$i4 = (Yr\ \overline{I4})\ Go\ (\overline{Fx}\ \overline{Fy}) + Go\ Fx\ Irx + Go\ Fy\ Iry + \overline{Go}\ (Fx + Fy)\ Ix$$

I4

$$oi4 = P30\ (\overline{Fx}\ \overline{Fy}) + Go\ Fx\ \overline{Irx} + Go\ Fy\ \overline{Iry}$$

$$i2 = Go\ \overline{R}\ I4 + \overline{Go}\ (Fx + Fy)\ Iy$$

I2

$$oi2 = Go\ \overline{I4} + (\overline{Fx}\ \overline{Fy})\ \overline{I4}$$

$$i1 = Go\ \overline{R}\ I2 + \overline{Go}\ (Fx + Fy)\ Iz$$

I1

$$oi1 = Go\ \overline{I2} + (\overline{Fx}\ \overline{Fy})\ \overline{I2}$$

SU5 LOGIC

P5

$$p5 = \overline{P5}\ P4$$

$$op5 = P5$$

P6

$$p6 = P5$$

$$op6 = \overline{P5}$$

$$Sh = A_i\,(Yr + I4)_i + As\,(Yr + I4)\,s$$

$$Ya = \overline{(CB + \overline{C}\,\overline{B})}$$

A

$$a = P5\,(Ys1\ Ye2\ Ys2 + Ye1\ Ys1\ \overline{Ye2} + Ye2\ Ys2\ Ys3 + \overline{Ye2}\ Ye3\ Ys3 + Ye2\ Ys2\ \overline{Ye3} + Ys1\ Ye3\ Ys3) + P6\ \overline{A}\,(\overline{B}\ D\ E + \overline{B}\ D\ F + B\ D\ E\ F)$$

$$oa = P6\ A\,(\overline{B}\ \overline{D}\ E + \overline{B}\ \overline{D}\ F + B\ \overline{D}\ E\ F) + P30$$

B

$$b = P5\,(Ys1\ Ye2\ Ys2\ Ye3\ Ys3 + Ye1\ Ys1\ \overline{Ye2}\ Ye3\ Ys3 + \overline{Ye1}\ Ye2\ Ys2\ Ye3\ Ys3 + \overline{Ys1}\ Ye2\ \overline{Ys2}\ Ye3\ \overline{Ys3} + Ye1\ \overline{Ys1}\ \overline{Ye2}\ Ye3\ \overline{Ys3} + \overline{Ye1}\ Ye2\ \overline{Ys2}\ Ye3\ \overline{Ys3} + Ye1\ Ys1\ Ye2\ Ys2\ \overline{Ye3} + Ye1\ \overline{Ys1}\ Ye2\ \overline{Ys2}\ \overline{Ye3}) + Sh\ \overline{A}\ \overline{B}\ C$$

$$ob = P6 + P30$$

C

$$c = P5\,(Ye1\ Ye2\ Ye3 + Ye1\ \overline{Ye2}\ \overline{Ye3} + \overline{Ye1}\ Ye2\ \overline{Ye3} + \overline{Ye1}\ \overline{Ye2}\ Ye3) + P6\ \overline{C}\ F + Sh\ D$$

$$oc = P6\ C\ F + Sh\ \overline{D} + P30$$

D

$$d = P5\,(Ys4\ Ye5\ Ys5 + Ye4\ Ys4\ \overline{Ye5} + Ye5\ Ys5\ Ys6 + \overline{Ye5}\ Ye6\ Ys6 + Ye5\ Ys5\ \overline{Ye6} + Ys4\ Ye6\ Ys6) + P6\ \overline{D}\,(B\ \overline{E}\ \overline{F} + \overline{B}\ \overline{C}\ E + A\ \overline{B}\ C\ E\ F + \overline{A}\ B\ C\ E\ F + \overline{A}\ \overline{B}\ E\ \overline{F} + \overline{A}\ B\ \overline{C}\ \overline{E}\ F + A\ B\ C\ \overline{E}\ F + \overline{A}\ \overline{B}\ C\ \overline{E}\ F) + Sh\ F$$

$$od = P6\ D\,(B\ E\ \overline{F} + \overline{A}\ C\ E\ \overline{F} + \overline{B}\ \overline{E}\ \overline{F} + \overline{A}\ B\ E\ F + A\ B\ \overline{C}\ E\ F + A\ \overline{B}\ C\ E\ F + \overline{A}\ \overline{B}\ \overline{E}\ F + \overline{B}\ C\ \overline{E}\ F + \overline{A}\ \overline{C}\ \overline{E}\ F + A\ B\ C\ \overline{E}\ F) + Sh\ \overline{F} + P30$$

E

$$e = P5\,(Ys4\ Ye5\ Ys5\ Ye6\ Ys6 + Ye4\ Ys4\ \overline{Ye5}\ Ye6\ Ys6 + \overline{Ye4}\ Ye5\ Ys5\ Ye6\ Ys6 + \overline{Ys4}\ Ye5\ \overline{Ys5}\ Ye6\ \overline{Ys6} + Ye4\ \overline{Ys4}\ \overline{Ye5}\ Ye6\ \overline{Ys6} + \overline{Ye4}\ Ye5\ \overline{Ys5}\ Ye6\ \overline{Ys6} + Ye4\ Ys4\ Ye5\ Ys5\ \overline{Ye6} + Ye4\ \overline{Ys4}\ Ye5\ \overline{Ys5}\ \overline{Ye6})$$

$$oe = P30$$

F

$$f = P5\,(Ye4\ Ye5\ Ye6 + Ye4\ \overline{Ye5}\ \overline{Ye6} + \overline{Ye4}\ Ye5\ \overline{Ye6} + \overline{Ye4}\ \overline{Ye5}\ Ye6) + P6\ \overline{F}\,(\overline{A}\ B\ \overline{D}\ E + A\ B\ D\ E)$$

$$of = P6\ F\,(A\ \overline{D} + \overline{A}\ D + \overline{B}\ \overline{C} + \overline{B}\ \overline{E} + \overline{C}\ \overline{E}) + Sh\ F + P30$$

$$yd = Go\ \overline{R}\,[(Yr\ \overline{I4})\ Ye1\ \overline{Ye2} + (Yr\ \overline{I4})\ \overline{Ye1}\ Ye2 + (I4\ \overline{I2})\ (Ye1\ Ys1)\ (Ye2\ Ys2) + (I4\ \overline{I2})\ Ye1\ \overline{Ys1}\ Ye2\ \overline{Ys2} + A\ (Yr + I4)\ Ya]$$

Yd

$$oyd = Yd\,[(Ye1\ Ys1) + (Ye2\ Ys2) + A\ \overline{Ya} + \overline{I4}]$$

$$yn = \overline{Go}\ Yr\ \overline{Yd}\ \overline{Yc} + \overline{R}\ Yr\ \overline{Yd}\ \overline{Yc} + I4\ \overline{Yr}\ Yd\ \overline{Yc} + I4\ \overline{Yr}\ \overline{Yd}\ Yc + Yr\ Yd\ Yc + Go\ R\ Ir$$

Yn

$$oyn = \overline{(yn)}$$

$$yc = Yr\ Yd$$

Yc

$$oyc = \overline{Yr}\ \overline{Yd}$$

$$P1 = \overline{I4}\ I2$$

$$ze = P1\ I1\ Xe$$

Ze

$$oze = P1\ \overline{I1} + P1\ \overline{Xe} + R$$

$$s = P1\ \overline{Yn}\ Xs + P1\ Yn\ \overline{Xs}$$

S

$$os = P1\ \overline{Yn}\ \overline{Xs} + P1\ Yn\ Xs$$

$$zs = S\ Ze\ \overline{Zs}$$

Zs

$$ozs = \overline{S}\ Ze\ Zs + R$$

$$of = P30\ \overline{Yr}\ \overline{Yd}\ Yc + P30\ Yr\ Yd\ \overline{Yc}$$

Of

$$oof = R$$

$$in = \overline{F}\,\overline{Fs}\,Ir + \overline{Go}\,\overline{Fs}\,Ir + Go\,F\,I1 + Fs\,If$$

In

$$oin = \overline{(in)}$$

$$i4 = (Yr\,\overline{I4})\,Go\,\overline{F} + Go\,F\,Ir + \overline{Go}\,F\,Ix$$

I4

$$oi4 = P30\,\overline{F} + Go\,F\,\overline{Ir}$$

$$i2 = Go\,\overline{R}\,I4 + \overline{Go}\,F\,Iy$$

I2

$$oi2 = Go\,\overline{I4} + \overline{F}\,\overline{I4}$$

$$i1 = Go\,F\,I2 + \overline{Go}\,F\,Iz + I4\,I2\,(\overline{\textcircled{D}\ P30})\,\overline{F}\,Yn$$

I1

$$oi1 = Go\,\overline{I2} + \overline{F}\,\overline{I2} + \textcircled{D}\ P30\,\overline{F}\,(\overline{yn})\,Yn + \textcircled{D}\ P30\,\overline{F}\,(yn)\,\overline{Yn}$$

$$go = P30\,G1\,\overline{(\overline{F}\,\overline{G}\,\overline{R})}$$

Go

$$ogo = P30\,\overline{G1}$$

4. MAINTENANCE AND TROUBLESHOOTING

A. SCOPE OF SECTION

This section contains general maintenance instructions and troubleshooting information for maintenance personnel having a thorough knowledge of the TRICE system.

B. MAINTENANCE

The use of solid-state and precision electronic components minimizes the maintenance requirements of the TRICE system to periodic inspections to detect corrosion, excessive dust accumulation, loose connectors, etc.

C. TROUBLESHOOTING

Malfunctions within the TRICE system are located in the following manner:

1) Isolate malfunction to TRICE proper or to associated input/output device.

2) If malfunction is within TRICE proper, isolate malfunction to control circuits or to computing modules.

3) Isolate malfunction to specific control circuit or to specific computing module.

C-1. ISOLATING MALFUNCTION TO TRICE

Select and run a proven program (or diagnostic routine), which uses all of the operating modes of the TRICE system and of which the computed results are known, first using a PB250 computer and then the reader/punch unit. If malfunctions are encountered only when using the computer, the malfunction may be attributed to the control circuits of the TRICE or to the PB250 computer. If malfunctions are encountered only when using the reader/punch unit, the malfunction may be attributed to the control circuits of the TRICE or to the reader punch unit. If malfunctions occur when using the PB250 and the reader/punch unit, the malfunction is within the TRICE proper.

C-2. CHECKING CONTROL CIRCUITS

Once it has been ascertained that the malfunction exists within the TRICE proper, operate the TRICE manually via the keyboard and observe the appropriate visual indicators on the console control panel. Refer to TRICE OPERATING AND PROGRAMMING MANUAL, CSP-150 for further details on manual operations.

If the control circuits of the TRICE are working properly but the results of computation are wrong, locate the defective computing module as described in subsequent paragraphs.

C-3. CHECKING COMPUTING MODULES

C-3a. Integrator Test (See Figure 4-1)

All Integrators are programmed in pairs to generate sine-cosine functions. One Servo per module rack generates sequences of positive and negative output increments which are reduced in rate to less than the iteration rate by one constant multiplier per block of modules.

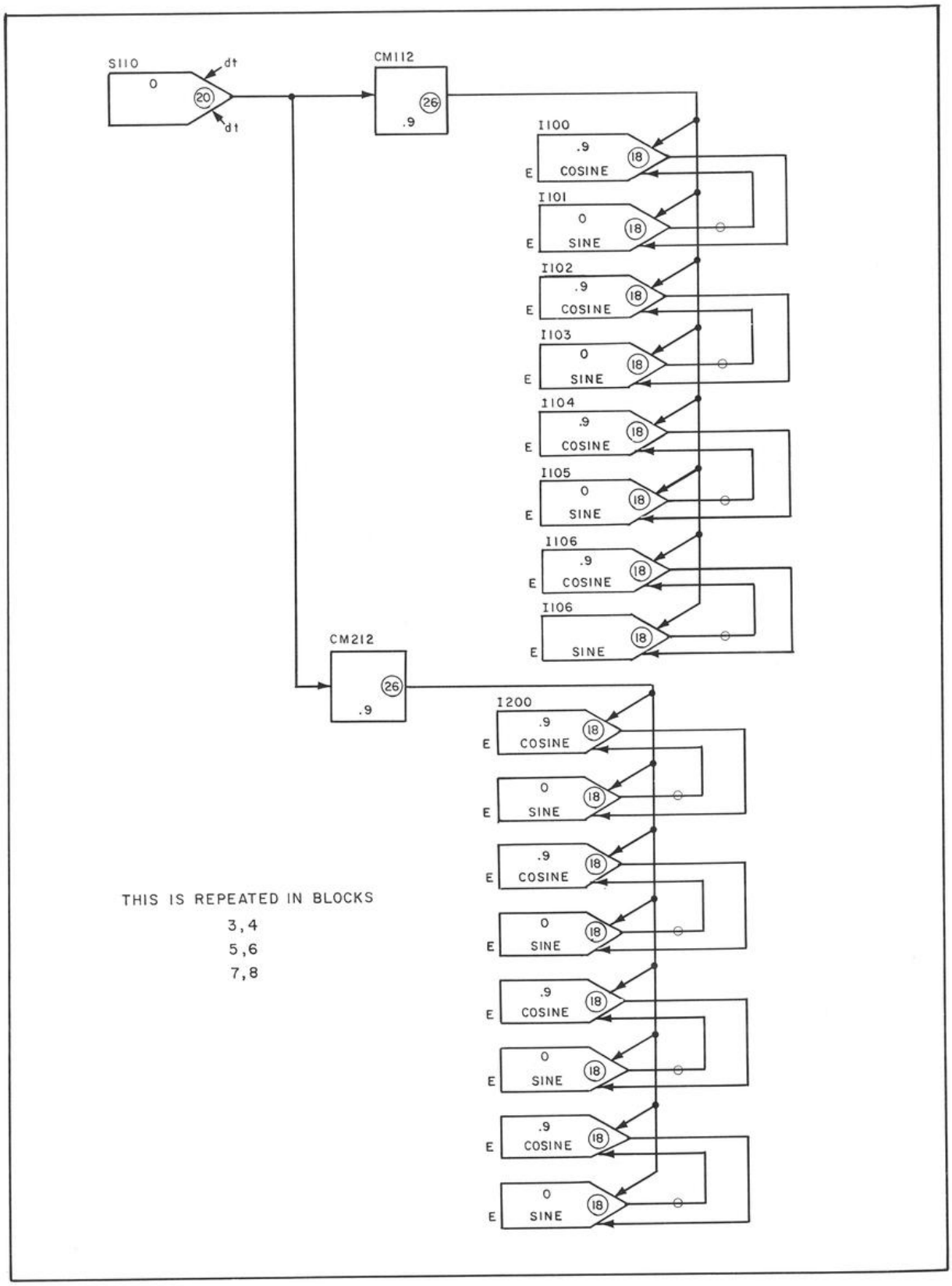


FIGURE 4-I. INTEGRATOR TEST

Its output is the independent variable input to the sine-cosine generators. All Integrator registers performing the same function e.g. the Y registers of all odd numbered Integrators should track which can be verified by type out through the PB250. For proper operation as sine-cosine generators the Integrators should be in the extrapolative mode, but the test can also be run in the other two modes (rectangular and interpolative).

C-3b. Variable Multiplier, Servo and Constant Multiplier Test (See Figure 4-2)

One pair of Integrators per module rack generate sine-cosine. Their outputs are fed to all Variable Multipliers to form the product of sine and cosine. Their outputs are accumulated in one Integrator for each Variable Multiplier. All Constant Multipliers receive the increments of the sine function and send them at a rate reduced by the value of their constants to the Servos. The Servos form the absolute value of this sine function. Their outputs are accumulated in Integrators. The test can be run in both the normal and decision modes of Servo operation. The Y register of the accumulating Integrators should track in groups of those accumulating Variable Multiplier outputs and those accumulating Servo outputs, which can be verified by typeout through the PB250.

C-3c. Summer Test (See Figure 4-3)

Six servos operating in the decision mode in the first two racks (block 1-4) generate sequences of positive, negative and zero increments of different length determined by their register length. These are patched into the six inputs of the first eight summers; they are connected to work with the adjacent Integrator. All Integrator Y registers non

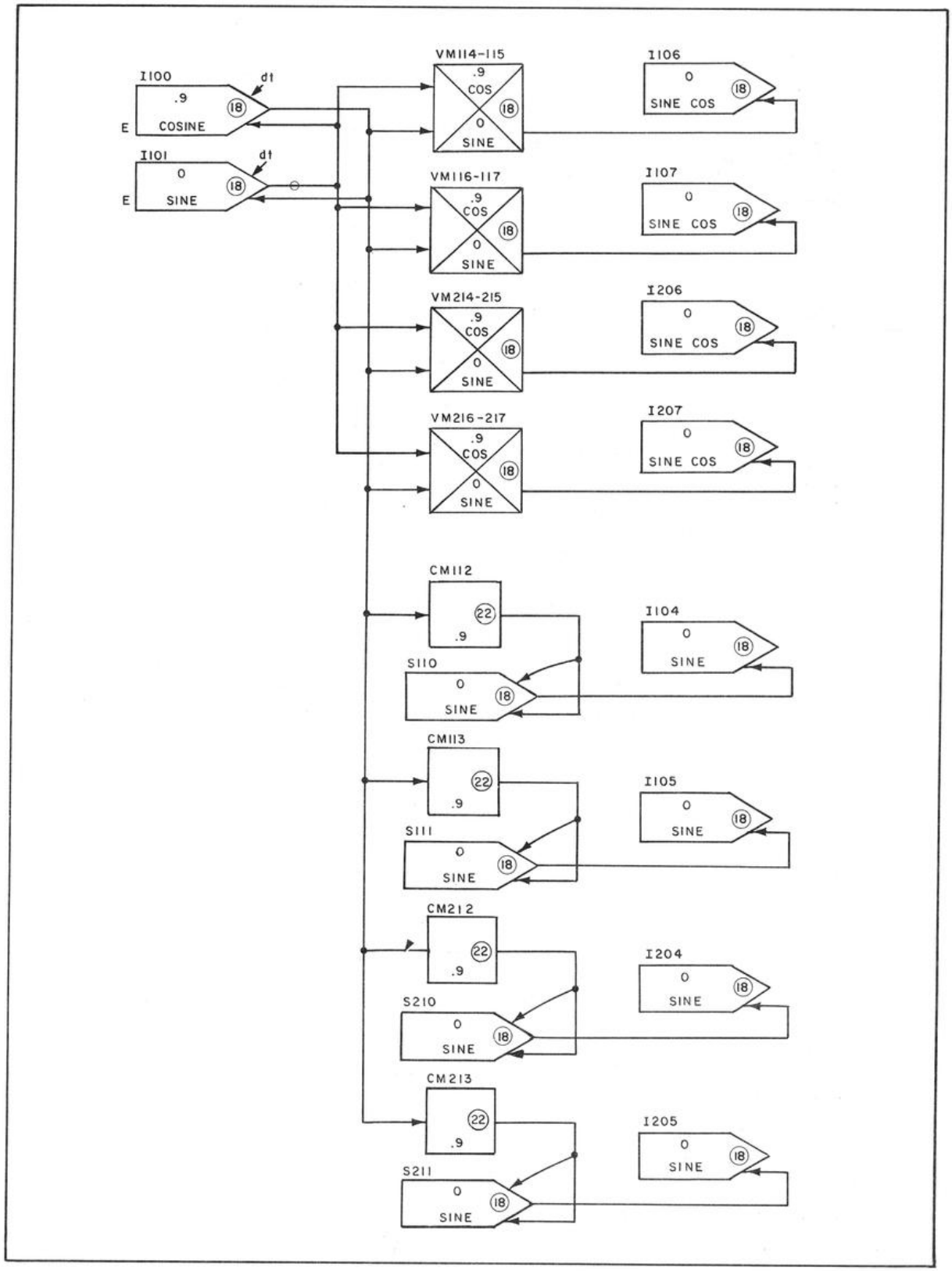


FIGURE 4-2. VARIABLE MULTIPLIER, SERVO AND CONSTANT MULTIPLIER TEST

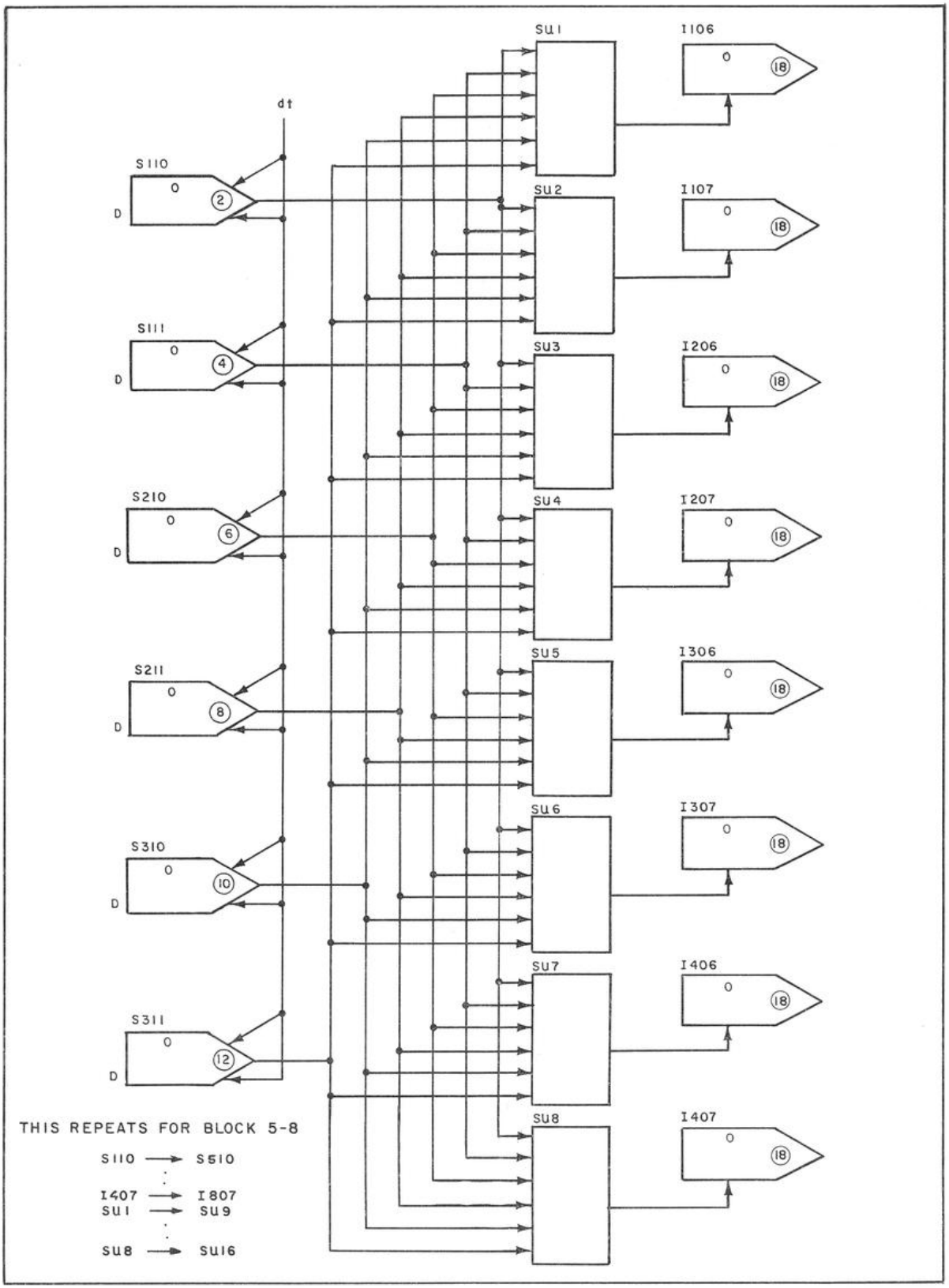


FIGURE 4-3. SUMMER TEST

should track which can be verified by typeout through the PB250. The setup is repeated in block 5-8. Since the longest Servo Y register is 12 bits, the sequence of input combinations is repeated about 12 times per second.

C-3d. PB250 Input-Output to TRICE and TRICE I Register Test

The PB250 generates pseudo random numbers, selects and fills all addressable TRICE modules sequentially. After each fill operation it reads back the number just filled and compares it to the number sent out. In case of error the module address is typed out and the test continues. In case of no error each module fill and verify cycle requires one PB250 memory cycle (3 msec). A similar test checks the read and fill operation of the A-D and D-A converters.

C-3e. A-D/D-A Converter Test (See Figure 4-4)

One pair of integrators per eight D-A converters generates sine-cosine and feeds the increments of the sine function to the D-A converters. Their analog outputs are connected to analog computer amplifier inputs, amplified to the 100V full scale level (nominal gain of 15) and sent back to the A-D converter inputs. The incremental outputs of the A-D converters are accumulated in TRICE Integrators. All registers participating in the test can be typed out through the PB250. The test should be run at about half scale amplitude. The Integrators last in the circuit (the ones connected to A-D Converters) will not track digitally with the original sine-cosine but will deviate by the analog errors in the circuit (approximately ±2 increments max.). The test also can be used to set up zero and gain of all conversion channels, if fixed digital values are filled into the D-A converter registers and the sine-cosine is not started (halt mode of TRICE).

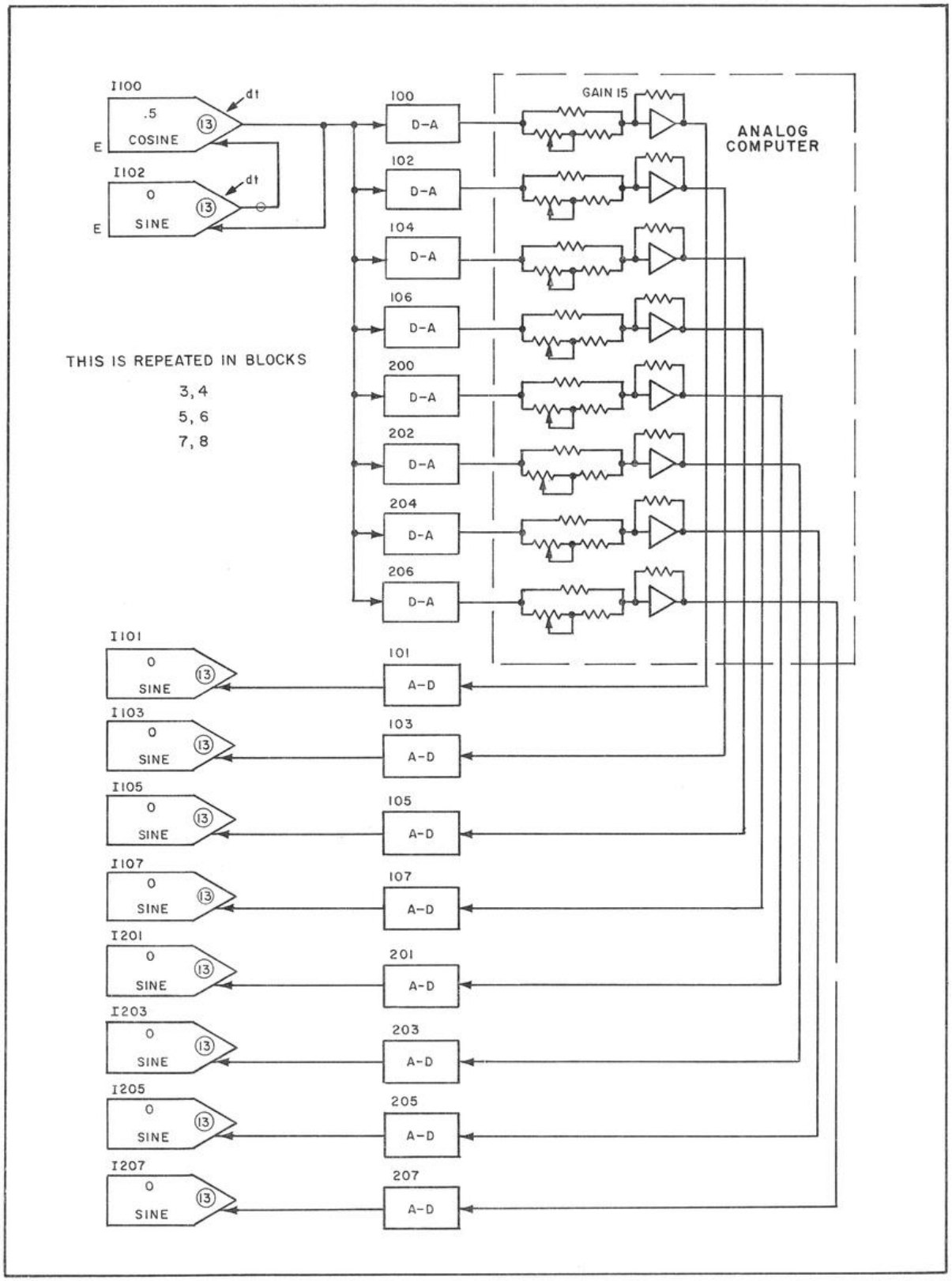


FIGURE 4-4. A-D/D-A CONVERTER TEST

C-3f. Digital-to-Analog Test

Increments of the sine output of sine-cosine generators of 13-bit register lengths are fed to all converters which are connected to operate in the d-a mode. All d-a registers should track.

C-3g. Analog-to-Digital Test

All converters are connected to operate in the a-d mode. Voltages of 0 v, + 50 v and -50 v are fed to their a-d inputs. With zero input, both unipolar and bipolar zero adjustment can be checked and set. With + 50 v or -50 v input, the input gain is set and checked at the opposite polarity.

5. PARTS LISTS

A. SCOPE OF SECTION

This section contains lists of modules used within the TRICE system, excluding the modules of the digital-to-analog and analog-to-digital converts and of the PB250 computer, and lists of replaceable components, excluding hardware, structural and bulk items.

B. DESCRIPTION OF TABLES

B-1. TABLE 5-1

This table lists the name of module, part number and reference designator of the computing TRICE modules. No quantity is indicated for these modules since the exact amount of modules varies from one system to another.

B-2. TABLE 5-2

This table is a composite listing of the standard digital modules used within the TRICE system, exclusive of the computing modules listed in Table 5-1. The table lists the module designator, part number and quantity of module cards used within the various sub-assemblies including the reader punch unit.

B-3. TABLE 5-3

This table is a composite listing of the replaceable components of the computing TRICE modules.

B-3a. Parts Description

A brief descriptive title of each part and pertinent values are given in this column to identify the part properly.

B-3b. Part Number

These numbers identify the part within the Packard Bell part numbering system.

B-3c. Reference Designators

The alpha numeric reference designators permit the parts to be identified in respect to the type of part and to the electrical value. For example, in reference designator R101, the R indicates the part is a resistor and 101 indicates the ohmic value of the resistor. The first two digits indicate the first two significant digits and the last digit indicates the number of zeros which follow the first two significant digits in order to express the value in ohms. That is, R101 indicates a 100 ohm resistor; whereas R100 indicates a 10 ohm resistor. The letter P is used to identify potentiometers.

Reference designators of capacitors are similar to those described for resistors with the exception that the letter C is used and the digits represent the value of the capacitor in micro-micro-farads.

Reference designators associated with transistors correspond with specific types of transistors. That is, Q1 designators on TRICE computing modules always indicates a 2N1500 type of transistor.

Note: The reference designators are silk screened on each TRICE computing module. Therefore, should any of these parts become damaged to the extent that identifying data is obliterated, the part and value may be determined by decoding the corresponding reference designator.

B-3d. Quantity

The five columns (titled I-5 through VM-5) lists the total quantity of replaceable parts for each of the computing modules.

B-3e. MSR-5

This column lists the various components of the magneto strictive register (MSR-5), which is a sub-assembly of all computing modules, except the summer module (SU-5).

B-4. TABLE 5-4

This table is a composite listing of the replaceable parts mounted on digital modules peculiar to TRICE systems. Individual columns of information are the same as described for Table 5-3.

B-5. TABLE 5-5

Parts description, part number and quantity used within digital modules EF-101, GD-100 and TD-101 are listed within this table. Reference designators of these components may be obtained by referring to figures 5-1, 5-2 or 5-3. These three modules are digital modules normally used within the PB-250 computer.

C. FIGURES AND PARTS LISTS

Figures 5-4 through figures 5-20 are combination schematics and parts lists for standard digital modules.

D. HOW TO USE THE PARTS LISTS

The process of obtaining a Packard Bell part number for any component within the TRICE system may be enhanced by using the following procedures. These procedures are based upon the assumption that technical personnel, familiar with the equipment, will perform this task.

1) Isolate the location of the component to a specific module.

2) Ascertain the standard nomenclature and reference designator of the part. This information may be obtained either from a schematic of the module, from the descriptive labelling or markings upon the component, or from the silk screened information on the module.

3) Once a particular component has been identified as to nomenclature and isolated to a particular module, refer to the corresponding table within this section. The individual components are listed in alphabetical sequence by standard nomenclature.

4) When ordering any parts from Packard Bell, use the Packard Bell part number to ensure prompt and accurate service.

Table 5-1.

LIST OF TRICE MODULES (COMPUTING)

Item	Name of Module	Part Number	Reference Designator
1	INTEGRATOR	505657	I-5
2	SUMMER	509589	SU-5
3	CONSTANT MULTIPLIER	505650	CM-5
4	SERVO	505653	S-5
5	VARIABLE MULTIPLIER	505656	VM-5

TABLE 5-2.

LIST OF DIGITAL MODULES

ITEM	MODULE DESIGNATOR	PART NUMBER	CONTROL UNIT	BUFFER REGISTER	DCS-1 REGISTER	DCS-1 CONTROL	READER PUNCH
1	DD-101	509371	3				
2	DG-103	505268	7	6	2	8	
3	DG-104	505312	20		3	21	2
4	DG-106	506440		11			
5	EF-1	500887	4			1	2
6	EF-101	504625		5			
7	GD-1	502359	8	8	3	4	1
8	GD-100	502492		5			
9	HF-3	500422	1				
10	IC-100	505314	4		2	3	1
11	IC-101	506437		3			
12	ND-100	504153			10		
13	TD-101	505789					3
14	TDI-1	502349	4				
15	TF-101	504794	8	1	12	11	2
16	TF-102	504795		14			
17	TI-3	500413	4		1	2	2
18	TI-100	504789		2			
19	TO-3	500416					2
20	XCG-1	502327		1			
21	Coax Driver*		1	6			
22	BDG-1.2*	508869			9		
23	BDG-4.8*	508870			9		
24	Res. Bd*		1				
25	Clock Shaper*			1			

*Normally used in Trice systems only.

TABLE 5-3.

PARTS LIST OF COMPUTING TRICE MODULES (Sheet 1 of 2)

ITEM	PART DESCRIPTION	PART NUMBER	REFER. DESIGNATOR	TOTAL QUANTITY PER EACH COMPUTING MODULES					
				I-5	SU-5	S-5	CM-5	VM-5	MSR-5
1	CAPAC. DISC. 15 uufd	503204-150	C 150						2
2	CAPAC. DISC. 25 uufd	503207-250	C 250	30	16	24	20	40	2
3	CAPAC. DISC. 50 uufd	503207-500	C 500	66	72	55	39	72	2
4	CAPAC. DISC. 100 uufd	503204-101	C 101	7	3	7	6	7	
5	CAPAC. DISC. 150 uufd	503204-151	C 151						1
6	CAPAC. DISC. 500 uufd	503204-501	C 501	10		10	10	16	
7	CAPAC. DISC. .0018 ufd	503204-182	C 182						1
8	CAPAC. DISC. .01 ufd	503203-103	C 103	3		3	3	3	
9	CAPAC. DISC. .02 ufd	503203-203	C 203						1
10	CAPAC. 15 MFD/20V	503840-156		9	9	9	6	9	5
11	CHOKE 4.7 uH	503044-047		3	2	3	2	3	
12	CHOKE 1 mH	503044-102		1	1	1	1	1	
13	CONNECTOR, Buggie 6441	503655		2	2	2	2	2	
14	CONNECTOR, CCC 60-70-3	503639							1
15	CONNECTOR, CCC 60-70-4	503640		3		2	2	5	
16	DELAY LINE	505527							1
17	DIODE	503050		395	462	293	206	459	8
18	INDICATOR 6977	503059		1		1		1	
19	MAGNETO STRICTIVE REGISTER	505644	MSR-5	3		2	2	5	
20	POTENTIOMETER 2 K	503636-202	P 202	1	1	1	1	1	1
21	POTENTIOMETER 10 K	503636-103	P 103						1
22	RESISTOR 1/10 W 33 OHM	503306-330	R 330						1
23	RESISTOR 1/4 W 47 OHM	503100-470	R 470						1
24	RESISTOR 1/4 W 100 OHM	503100-101	R 101						1
25	RESISTOR 1/4 W 120 OHM	503100-121	R 121	2	1	2	2	2	
26	RESISTOR 1/4 W 150 OHM	503100-151	R 151	2		2	1	4	
27	RESISTOR 1/4 W 220 OHM	503100-221	R 221						2
28	RESISTOR 1/4 W 240 OHM	503100-241	R 241	1		1		1	
29	RESISTOR 1/4 W 270 OHM	503100-271	R 271	3		3	3	3	
30	RESISTOR 1/4 W 330 OHM	503100-331	R 331						2

TABLE 5-3.

PARTS LIST OF COMPUTING TRICE MODULES (Sheet 2 of 2)

ITEM	PART DESCRIPTION	PART NUMBER	REFER. DESIGNATOR	TOTAL QUANTITY PER EACH COMPUTING MODULES					
				I-5	SU-5	S-5	CM-5	VM-5	MSR-5
31	RESISTOR 1/4 W 390 OHM	503100-391	R 391	3	2	3	2	3	
32	RESISTOR 1/4 W 470 OHM	503100-471	R 471						1
33	RESISTOR 1/4 W 680 OHM	503100-681	R 681	1	1	1	1	1	
34	RESISTOR 1/4 W 820 OHM	503100-821	R 821						4
35	RESISTOR 1/4 W 1 K	503100-102	R 102	60	59	52	38	75	2
36	RESISTOR 1/4 W 1.2 K	503100-122	R 122	4	2	3	2	4	1
37	RESISTOR 1/4 W 1.5 K	503100-152	R 152	31	15	26	13	26	1
38	RESISTOR 1/4 W 1.8 K	503100-182	R 182	1		1			
39	RESISTOR 1/4 W 2.2 K	503100-222	R 222	45	31	37	31	54	4
40	RESISTOR 1/4 W 2.7 K	503100-272	R 272	1	1	1	1	1	2
41	RESISTOR 1/4 W 3.9 K	503100-392	R 392	1	2				
42	RESISTOR 1/4 W 5.6 K	503100-562	R 562	66	57	57	41	79	2
43	RESISTOR 1/4 W 6.8 K	503100-682	R 682	99	116	74	51	115	2
44	RESISTOR 1/4 W 10 K	503100-103	R 103						3
45	RESISTOR 1/4 W 12 K	503100-123	R 123						1
46	RESISTOR 1/4 W 15 K	503100-153	R 153	4	2	3	2	3	
47	RESISTOR 1/4 W 22 K	503100-223	R 223	20	14	17	14	29	
48	RESISTOR 1/4 W 27 K	503100-273	R 273	2		2		2	
49	RESISTOR 1/4 W 39 K	503100-393	R 393	21	41	18	10	17	1
50	RESISTOR 1/4 W 47 K	503100-473	R 473					40	
51	RESISTOR 1/4 W 82 K	503100-823	R 823	47	31	39	31	14	4
52	RESISTOR 1/4 W 100 K	503100-104	R 104	1		1		1	
53	RESISTOR 1/4 W 150 K	503100-154	R 154	30	16	24	20	40	2
54	TRANSISTOR 2N1500	503003	Q 1	34	19	28	23	44	4
55	TRANSISTOR 2N2048	503525	Q 2	58	59	49	26	52	4
56	TRANSISTOR 2N404	503000	Q 3	14		14	14	21	

TABLE 5-4.

PARTS LIST FOR TRICE DIGITAL MODULES (Sheet 1 of 2)

ITEM	PARTS DESCRIPTION	PART NUMBER	REF DESIGNATOR	BDG 1.2	BDG 4.8	RESISTOR BOARD	COAX DRIVER	CLOCK SHAPER
1	CAPACITOR .02 ufd	503203-203	C 203					2
2	CAPACITOR 15 uufd	503098-150	C 150					2
3	CAPACITOR 39 uufd	503097-390	C 390					2
4	CAPACITOR 50 uufd	503207-500	C 500				2	
5	CAPACITOR 56 uufd	503097-560	C 560					2
6	CAPACITOR 82 uufd	503097-820	C 820					2
7	CAPACITOR 100 uufd	503204-101	C 101				2	2
8	CAPACITOR 500 uufd	503204-501	C 501	2				
9	CAPACITOR, VARIABLE 6-25 uufd	503218	C 218					2
10	CAPACITOR 15 MFD/20V	503840-156	C 156				1	
11	CHOKE 10 uh	503044-100					2	
12	CHOKE 68 uh	503044-680						2
13	DIODE 3050	503050		76	87			6
14	RESISTOR 1/2 W 47 OHM	503101-470	R 470				2	
15	RESISTOR 1/2 W 91 OHM	503101-910	R 910				16	
16	RESISTOR 1/4 W 120 OHM	503100-121	R 121					2
17	RESISTOR 1/4 W 270 OHM	503100-271	R 271					2
18	RESISTOR 1/4 W 470 OHM	503100-471	R 471			12		
19	RESISTOR 1/4 W 1 K	503100-102	R 102					2
20	RESISTOR 1/4 W 1.2 K	503100-122	R 122	4	4			
21	RESISTOR 1/4 W 1.5 K	503100-152	R 152	2				2
22	RESISTOR 1/4 W 2 K	503100-512	R 512					2
23	RESISTOR 1/4 W 2.2 K	503100-222	R 222				2	4
24	RESISTOR 1/4 W 3.3 K	503100-332	R 332					2
25	RESISTOR 1/4 W 3.9 K	503100-392	R 392				2	4
26	RESISTOR 1/4 W 4.7 K	503100-472	R 472	2				
27	RESISTOR, VARIABLE 5 K	503886-502	P 502					2
28	RESISTOR 1/4 W 5.6 K	503100-562	R 562	21	23			
29	RESISTOR 1/4 W 6.8 K	503100-682	R 682					2
30	RESISTOR 1/4 W 15 K	503100-153	R 153	2				
31	RESISTOR 1/4 W 22 K	503100-223	R 223				4	

TABLE 5-4.

PARTS LIST FOR TRICE DIGITAL MODULES (Sheet 2 of 2)

ITEM	PARTS DESCRIPTION	PART NUMBER	REF DESIGNATOR	BDG 1.2	BDG 4.8	RESISTOR BOARD	COAX DRIVER	CLOCK SHAPER
32	RESISTOR 1/4 W 27 K	503100-273	R 273					2
33	RESISTOR 1/4 W 68 K	503100-683	R 683	4	4			
34	TRANSISTOR 2N404	503000	Q 3	6	4			
35	TRANSISTOR 2N1204						4	
36	TRANSISTOR 2N1500	503003	Q 1				2	
37	TRANSISTOR 2N2048	503525					4	
38	TRANSISTOR	503881						4

TABLE 5-5.

PARTS LIST OF PB-250 MODULES

PARTS DESCRIPTION	PART NUMBER	EF-101	GD-100	TD-101
CAPACITOR, .02 uf	503203-203	1		
CAPACITOR, 15 uf, 20V	503220-04-156		1	
CAPACITOR, 25 uuf, ± 10%	503207-250		4	
CAPACITOR, 50 uuf, ± 10%	503207-500		4	
DIODE	503050	6		
RESISTOR, 1/2 W, 82 OHM, ± 5%	503101-272			4
RESISTOR, 1/2 W, 180 OHM, ± 5%	503101-181			4
RESISTOR, 1/4 W, 680 OHM, ± 5%	503100-681		4	
RESISTOR, 1/4 W, 120 OHM, ± 5%	503100-121	6		
RESISTOR, 1/2 W, 1 K, ± 5%	503101-102			4
RESISTOR, 1/4 W, 1.2 K, ± 5%	503100-122	6	4	
RESISTOR, 1/4 W, 1.5 K, ± 5%	503100-152		4	
RESISTOR, 1/4 W, 2.7 K, ± 5%	503100-272		4	4
RESISTOR, 1/4 W, 5.6 K, ± 5%	503100-562	2	8	
RESISTOR, 1/4 W, 15 K, ± 5%	503100-153	12		
RESISTOR, 1/4 W, 18 K, ± 5%	503100-183		4	
RESISTOR, 1/4 W, 27 K, ± 5%	503100-273		4	
TRANSISTOR, 2N404	503600			4
TRANSISTOR, 2N457A	503184			4
TRANSISTOR, 2N604	503002	6		
TRANSISTOR, 2N1500	503003		8	

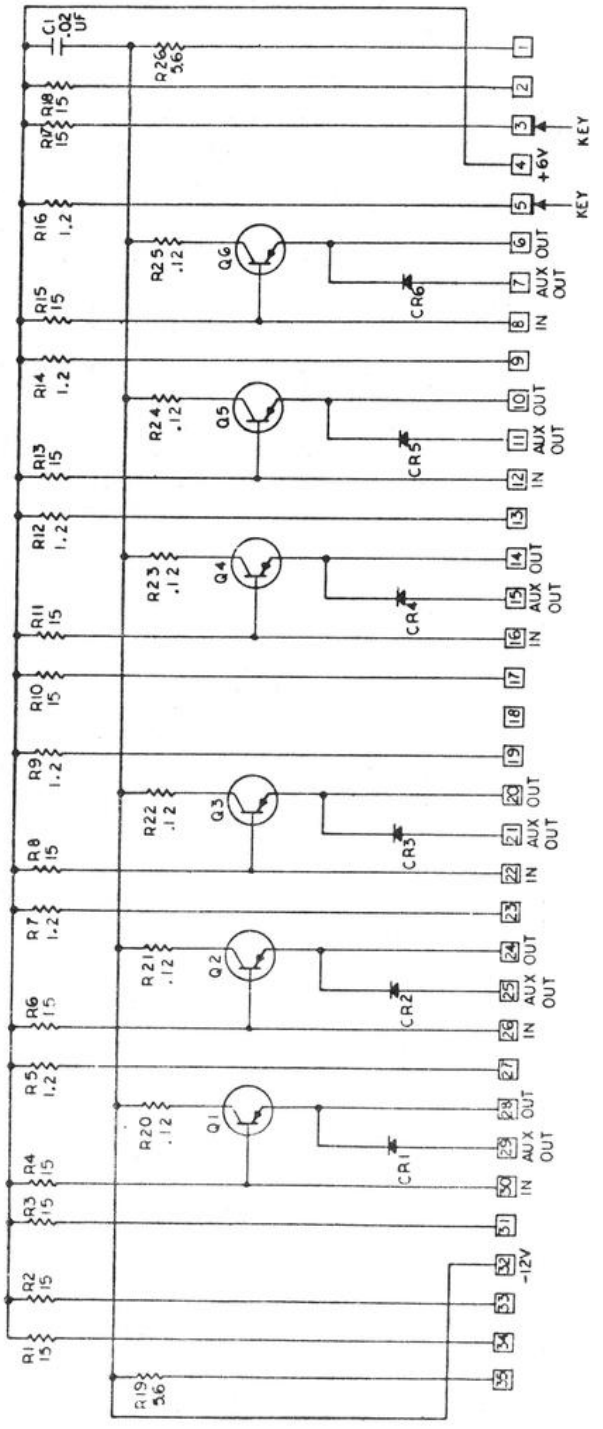


Figure 5-1. EF-101 Schematic

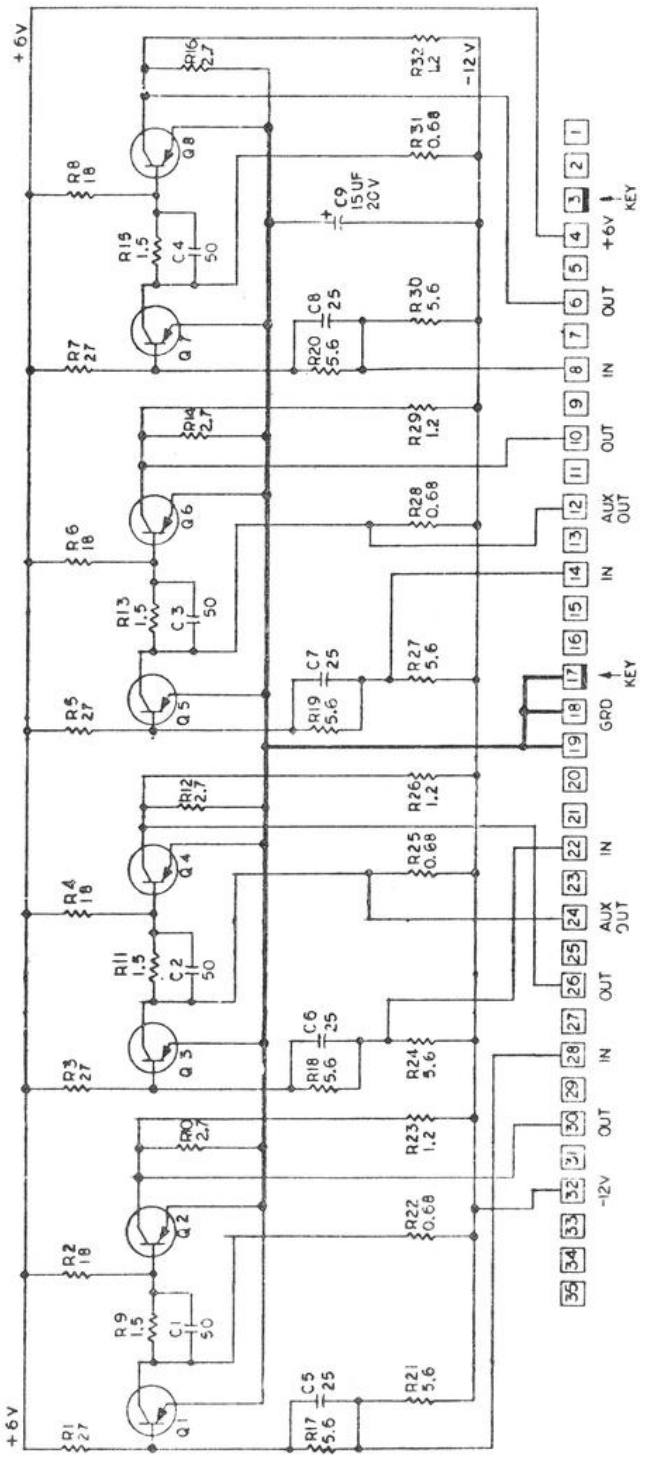


Figure 5-2. GD-100 Schematic

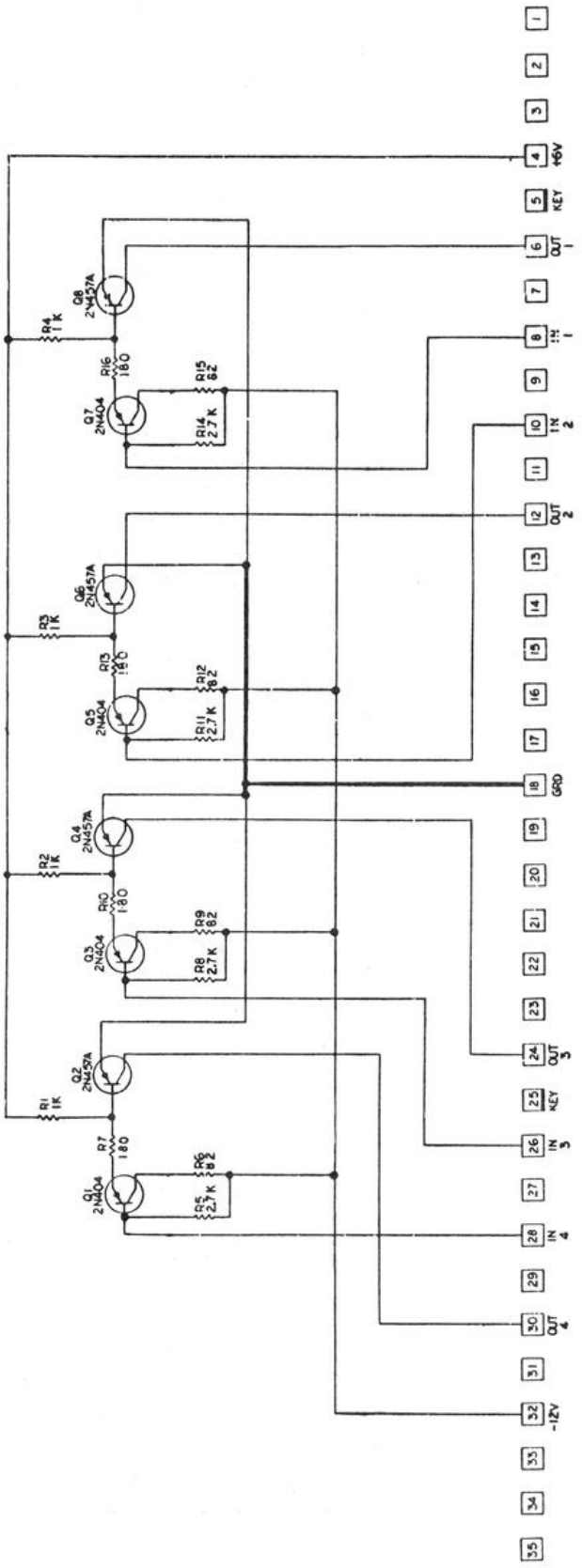


Figure 5-3. TD-101 Module Schematic

Part Description	Reference Designator	PBC Part No.	Qty Per Assy
Diode	CR1 — 24	503051	24*
Resistor, 470Ω ±5%, 1/2w	R13 — 24	503101-471	12
Resistor, 2.7k ±5%, 1/4w	R31 — 36	503100-272	6
Resistor, 5.6k ±5%, 1/4w	R1 — 6, R25 — 30	503100-562	12
Resistor, 15k ±5%, 1/4w	R7 — 12	503100-153	6
Transistor, 2N2374	Q1, 3, 5, 7, 9, 11	503717	6
Transistor, 2N670	Q2, 4, 6, 8, 10, 12	503712	6

*May be replaced in field by 1N770.

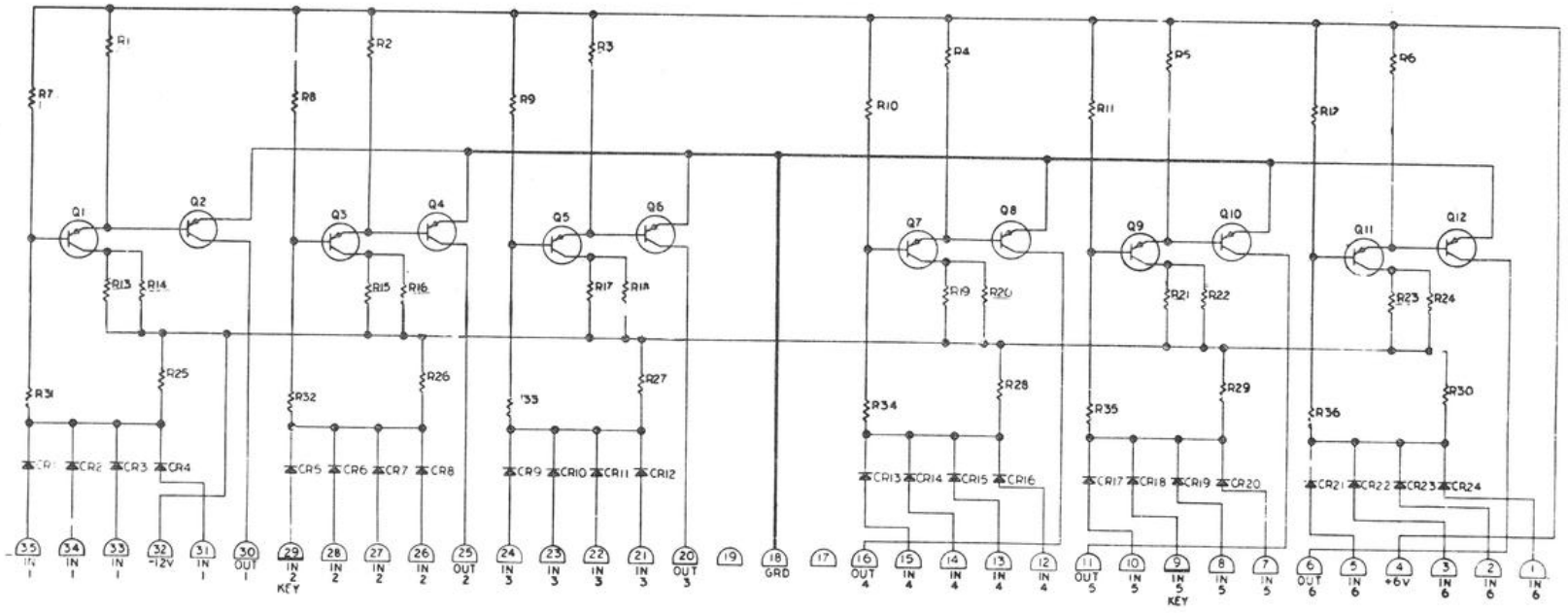


Figure 5-4. DD-101 Schematic and Parts List

Part Description	Reference Designator	PBC Part No.	Qty Per Assy.
Diode	CR1 — 16	503051	16
Resistor, 68 Ω, ±5%, 1/4w	R5 — 8	503100-680	4
Resistor, 1.2k, ±5%, 1/4w	R1 — 4	503100-122	4
Resistor, 6.8k, ±5%, 1/4w	R9 — 12	503100-683	4
Transistor, PNP	Q1 — 4	503748	4

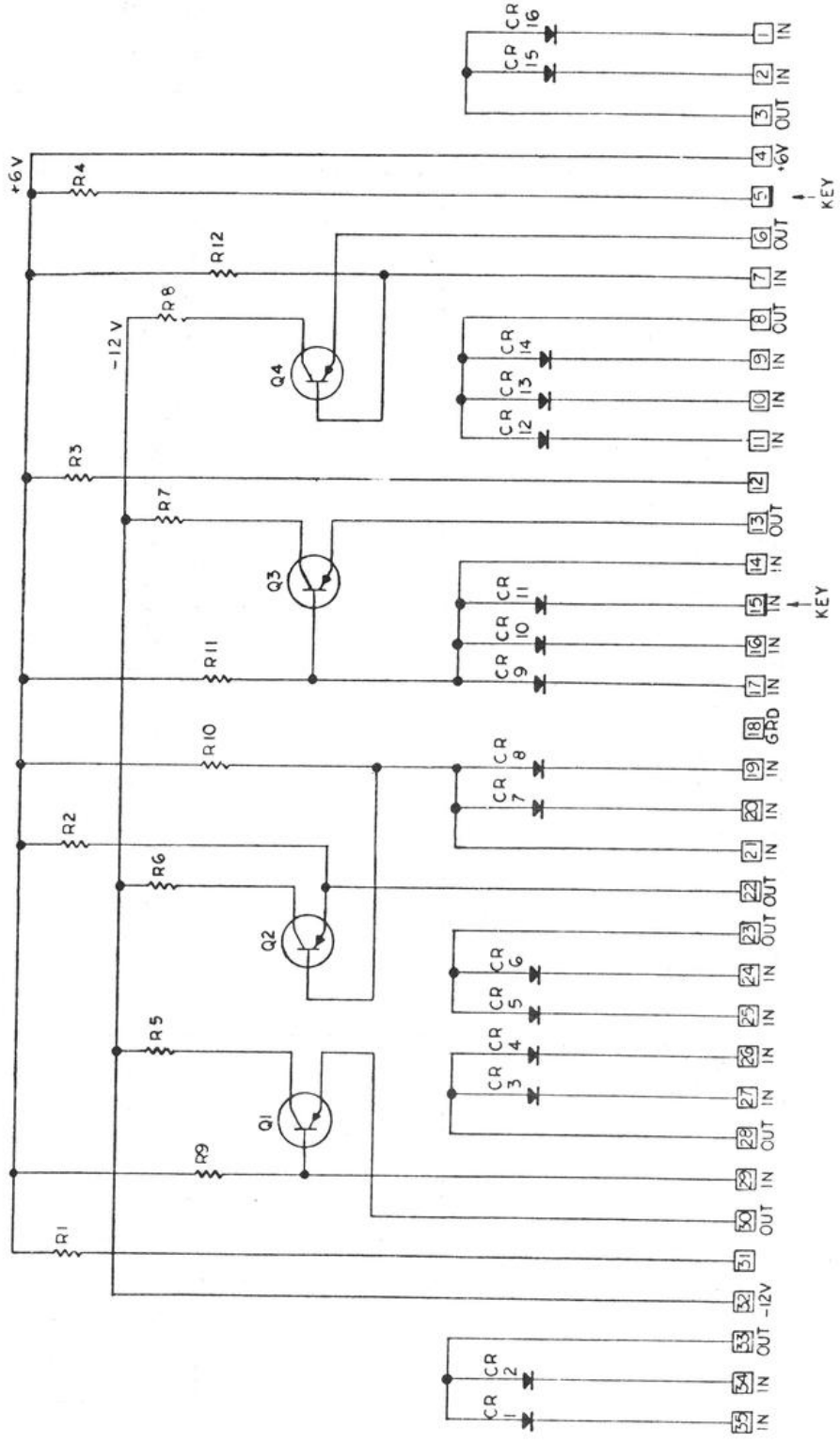


Figure 5-5. DG-103 Schematic and Parts List

Part Description	Reference Designator	PBC Part No.	Qty Per Assy.
Diode	CR1 — 20	503051	20*
Resistor, 5.6k Ω ±5%, 1/4w	R1 — 6	503100-562	6

*May be replaced in field by 1N770.

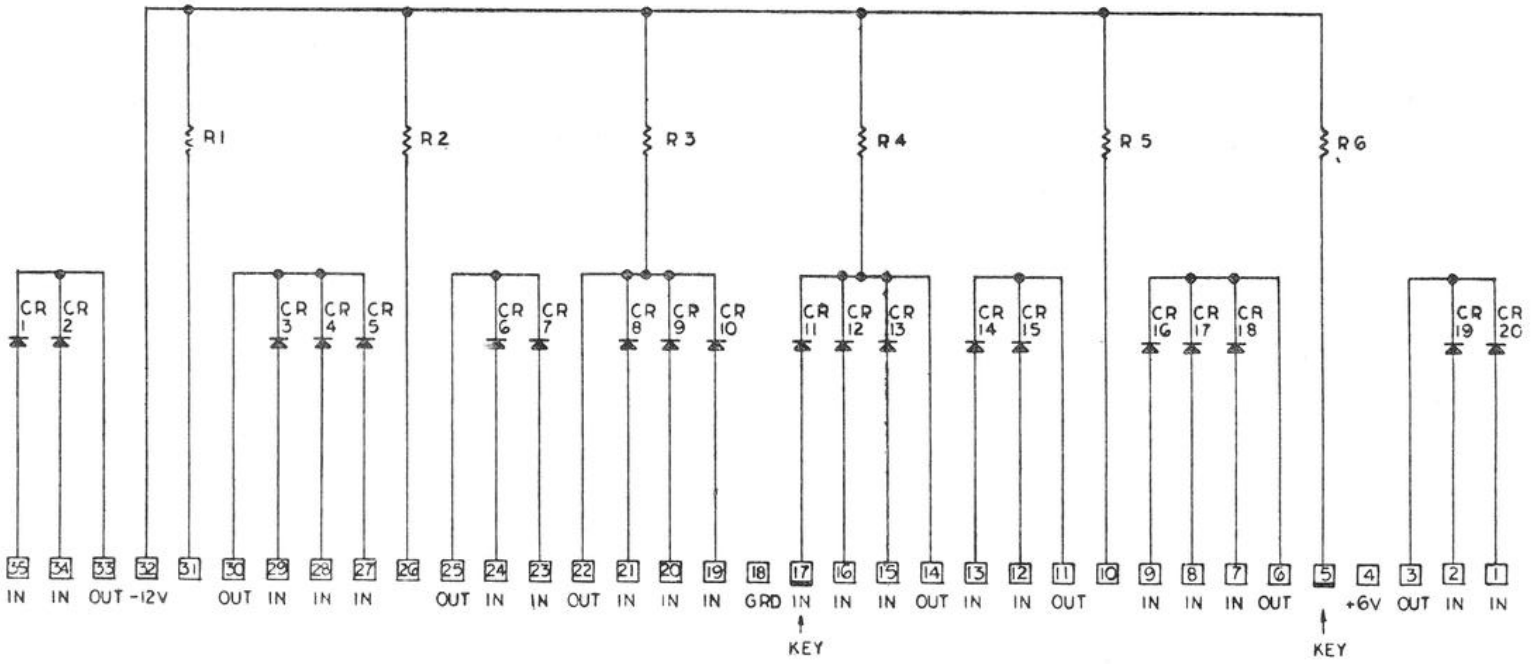


Figure 5-6. DG-104 Schematic and Parts List

Part Description	Reference Designator	PBC Part No.	Qty Per Assy.
Diode	CR1 — 20	503050	20
Resistor, 5.6k, ±5%, 1/4w	R1 — 6	503100-562	6

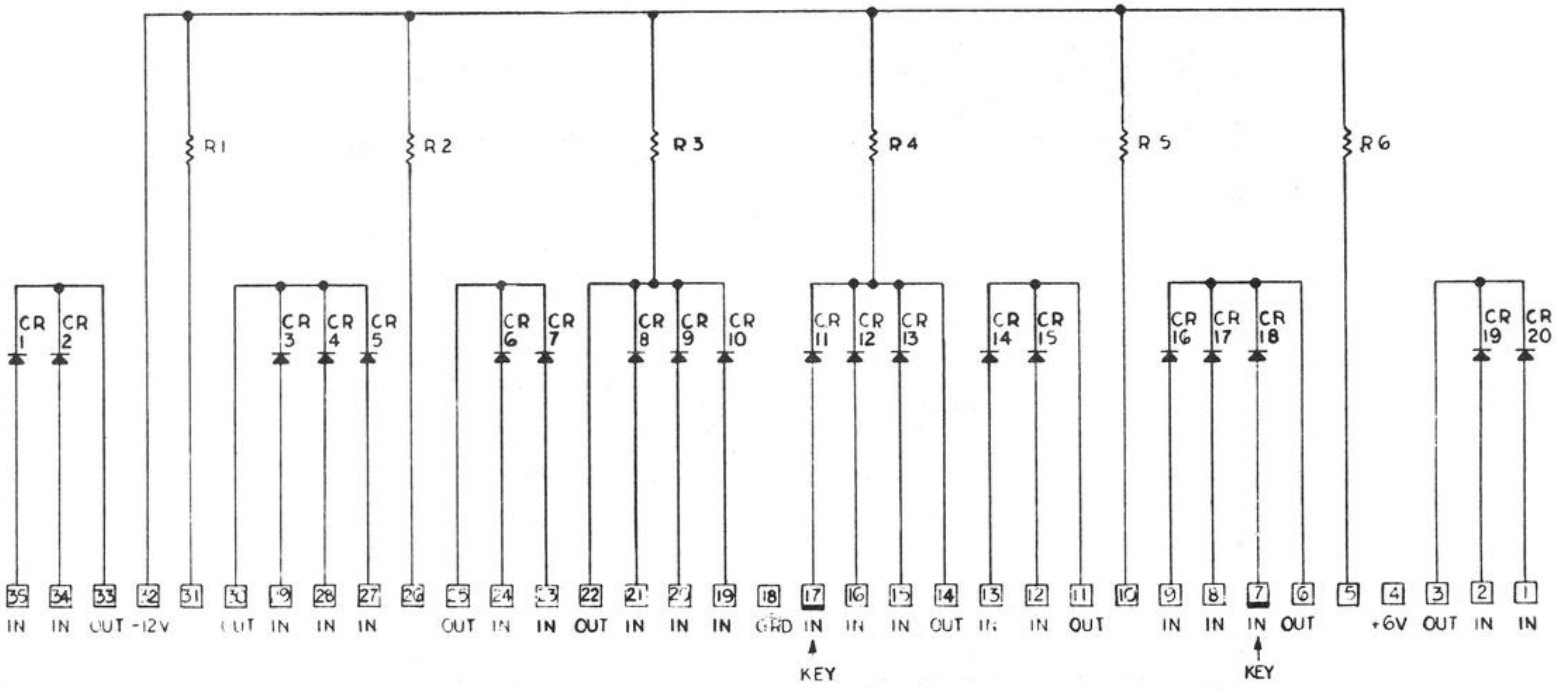


Figure 5-7. DG-106 Schematic and Parts List

Part Description	Reference Designator	PBC Part No.	Qty Per Assy.
Diode	CR1 — 6	503050	6*
Resistor, 68 Ω ±5%, 1/2w	R1 — 6	503101-680	6
Resistor, 1.2k Ω ±5%, 1/2w	R7 — 12	503101-122	6
Resistor, 68k Ω ±5%, 1/2w	R13 — 18	503101-683	6
Transistor, PNP, 2N1305	Q1 — 6	503748	6

*May be replaced in field by 1N770.

ON MODULES STAMPED WITH A CHANGE LETTER "C" OR GREATER, CR1 THRU CR6 AND R13 THRU R18 ARE INCLUDED. FOR EARLY MODULES WITHOUT CHANGE LETTERS, CR1 THRU CR6 ARE OMITTED AND Q1 THRU Q6 COLLECTORS ARE RETURNED DIRECTLY TO -12 VOLTS.

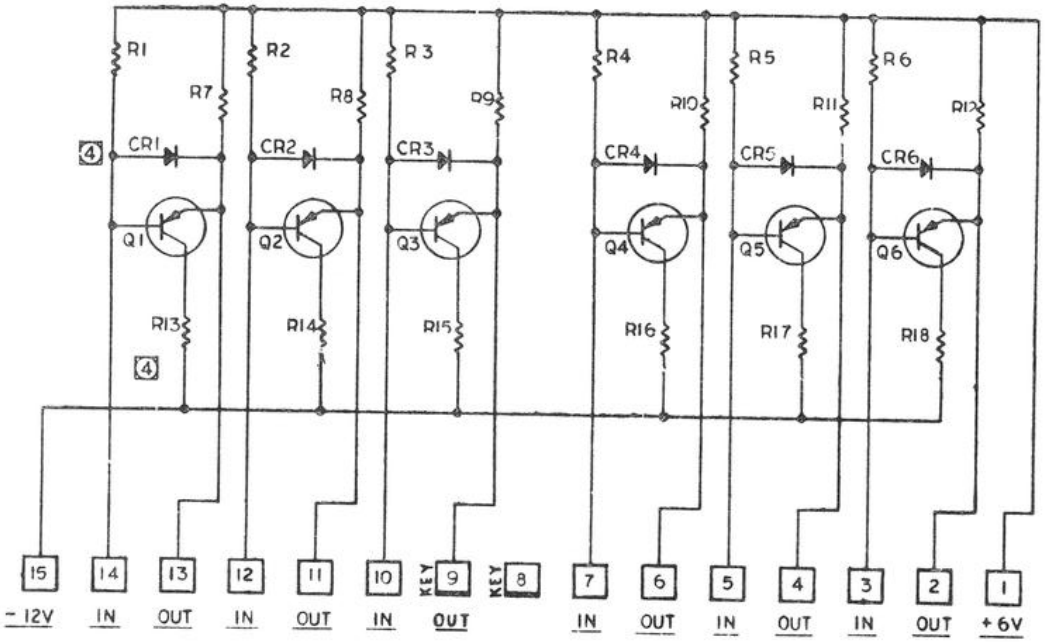
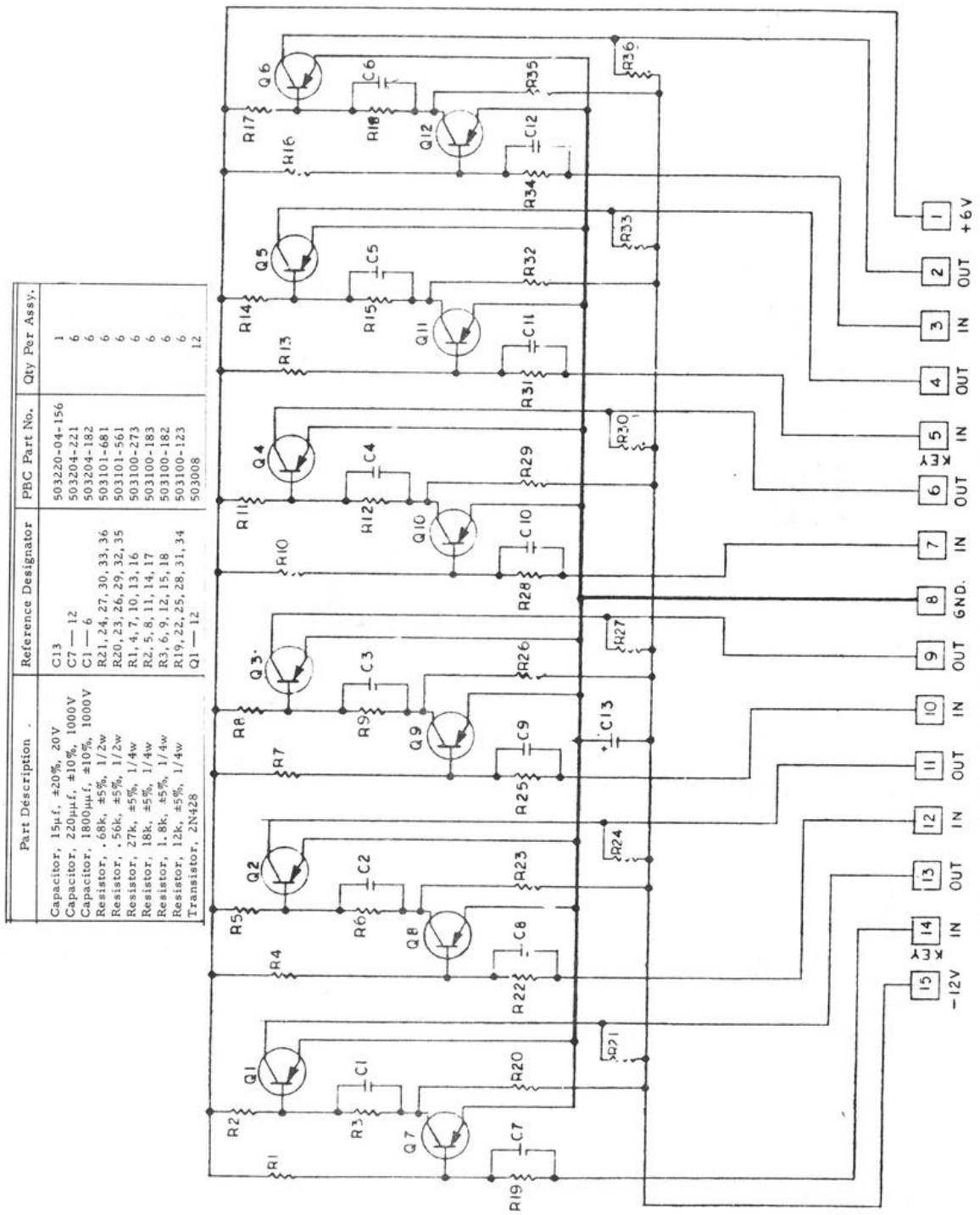


Figure 5-8. EF-1 Schematic and Parts List



Part Description	Reference Designator	PBC Part No.	Qty Per Assy.
Capacitor, 15μf, ±20%, 20V	C13	503220-04-156	1
Capacitor, 220μμf, ±10%, 1000V	C7 — 12	503204-221	6
Capacitor, 1800μμf, ±10%, 1000V	C1 — 6	503204-182	6
Resistor, .68k, ±5%, 1/2w	R21, 24, 27, 30, 33, 36	503101-681	6
Resistor, .56k, ±5%, 1/2w	R20, 23, 26, 29, 32, 35	503101-561	6
Resistor, 27k, ±5%, 1/4w	R1, 4, 7, 10, 13, 16	503100-273	6
Resistor, 18k, ±5%, 1/4w	R2, 5, 8, 11, 14, 17	503100-183	6
Resistor, 1.8k, ±5%, 1/4w	R3, 6, 9, 12, 15, 18	503100-182	6
Resistor, 12k, ±5%, 1/4w	R19, 22, 25, 28, 31, 34	503100-123	6
Transistor, 2N428	Q1 — 12	503008	12

Figure 5-9. GD-1 Schematic and Parts List

Part Description	Reference Designator	PBC Part No.	Qty Per Assy.
Capacitor, 500μμf, 1000V	C2	503204-501	1
Capacitor, 1000μμf, 1000V	C3	503204-102	1
Capacitor, 220μμf, 1000V	C1, 4, 5, 6	503204-221	4
Diode	CR1, 2	503051	2
Resistor, 1k, ±5%, 1/2w	R1, 4	503101-102	2
Resistor, 12k, ±5%, 1/2w	R6	503101-123	1
Resistor, 18k, ±5%, 1/2w	R2, 3	503101-183	2
Resistor, 22k, ±5%, 1/2w	R7	503101-223	1
Resistor, 470 Ω ±5%, 1/2w	R5	503101-471	1
Resistor, 4.7k, ±5%, 1/2w	R9, 10, 11	503101-472	3
Resistor, 5.6k, ±5%, 1/2w	R12	503101-562	1
Resistor, 680 Ω ±5%, 1/2w	R8	503101-681	1
Transistor, PNP 2N1305	Q1, 2	503748	2
Transistor, PNP 2N428	Q3, 4	503008	2

TO VARY REPETITION RATE OR DUTY CYCLE, CAPACITORS MAY BE ADDED AT PINS 9-13 AND 10-14 AS SHOWN.

ALL DIODES PBC 503021 MAY BE REPLACED IN FIELD BY IN770

REMOVABLE LINKS E1 AND E2

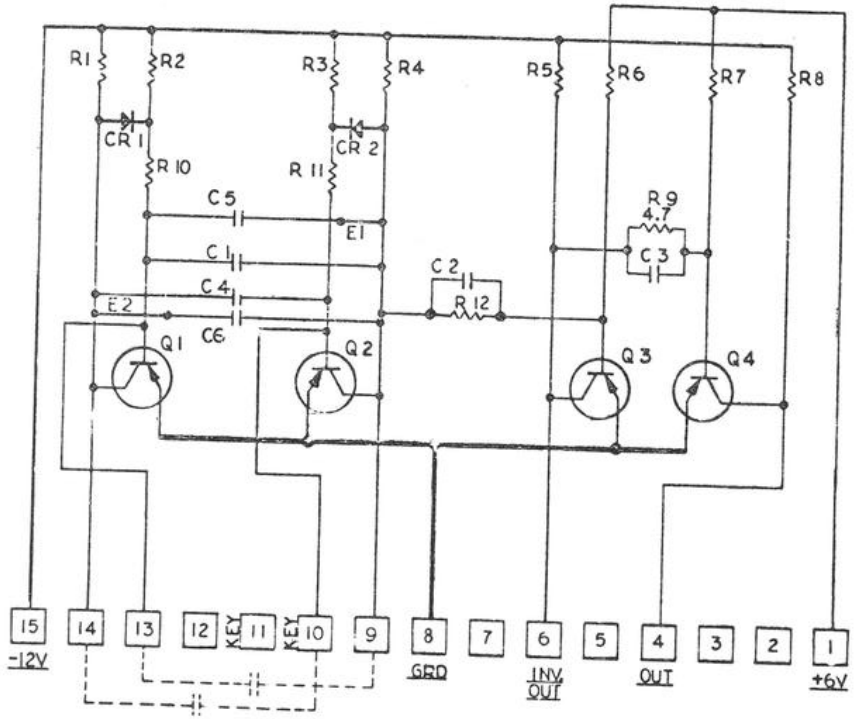


Figure 5-10. HF-3 Schematic and Parts List

Part Description	Reference Designator	PBC Part No.	Qty Per Assy.
Capacitor, 500μμf, ±10%, 1000V	C1 — 22	503204-501	22
Diode	CR1 — 22	503051	22
Resistor, 39k, ±5%, 1/4w	R1 — 22	503100-393	22
Resistor, 1.8k, ±5%, 1/4w	R23 — 44	503100-182	22

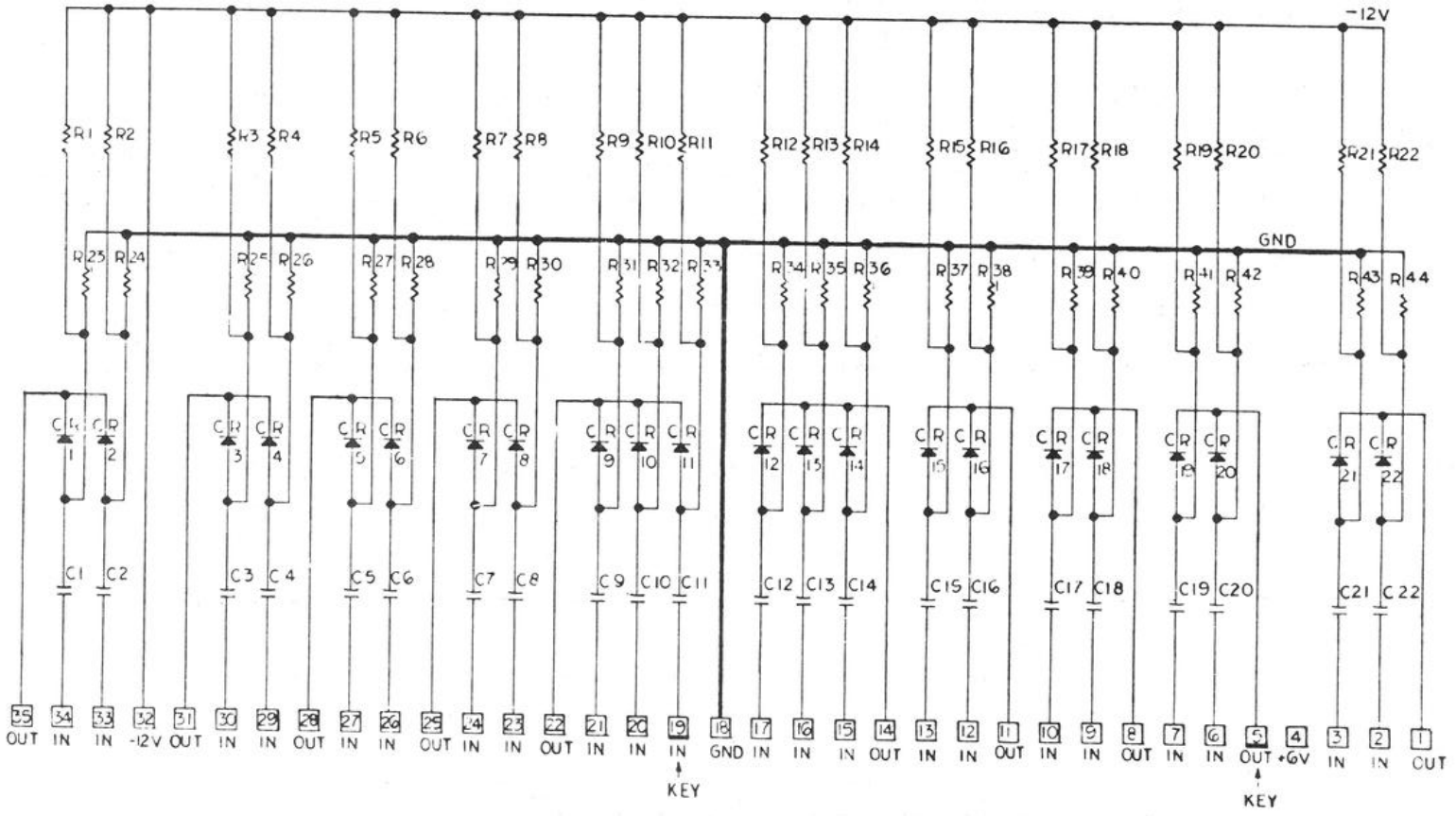


Figure 5-11. IC-100 Schematic and Parts List

Part Description	Reference Designator	PBC Part No.	Qty Per Assy.
Capacitor, 50μμf, ±10%, 1000V	C1 — 22	503204-500	22
Diode	CR1 — 22	503050	22
Resistor, 68k, ±5%, 1/4w	R1 — 22	503100-683	22
Resistor, 2.2k, ±5%, 1/4w	R23 — 44	503100-222	22

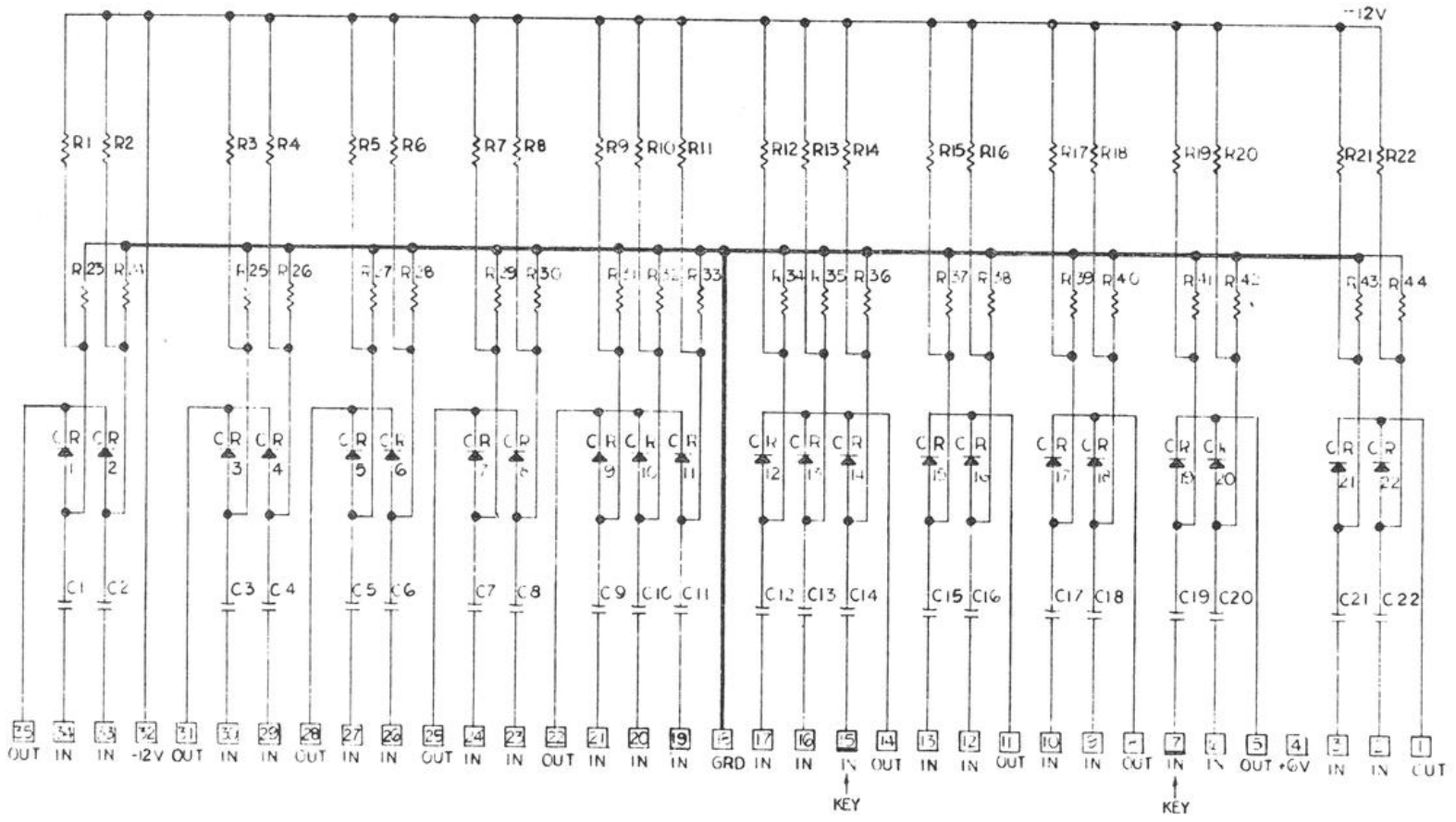


Figure 5-12. IC-101 Schematic and Parts List

Part Description	Reference Designator	PBC Part No.	Qty Per Assy.
Resistor, 2.7k Ω ±5%, 1/4w	R1 — 8	503100-272	8
Resistor, 8.2k Ω ±5%, 1/4w	R9 — 38	503100-822	30
Resistor, 10k Ω ±5%, 1/4w	R39 — 48	503100-103	10
Resistor, 15 meg Ω ±5%, 1/4w	R49 — 58	503100-155	10
Transistor, NPN S3114A	Q1 — 10	503364	10

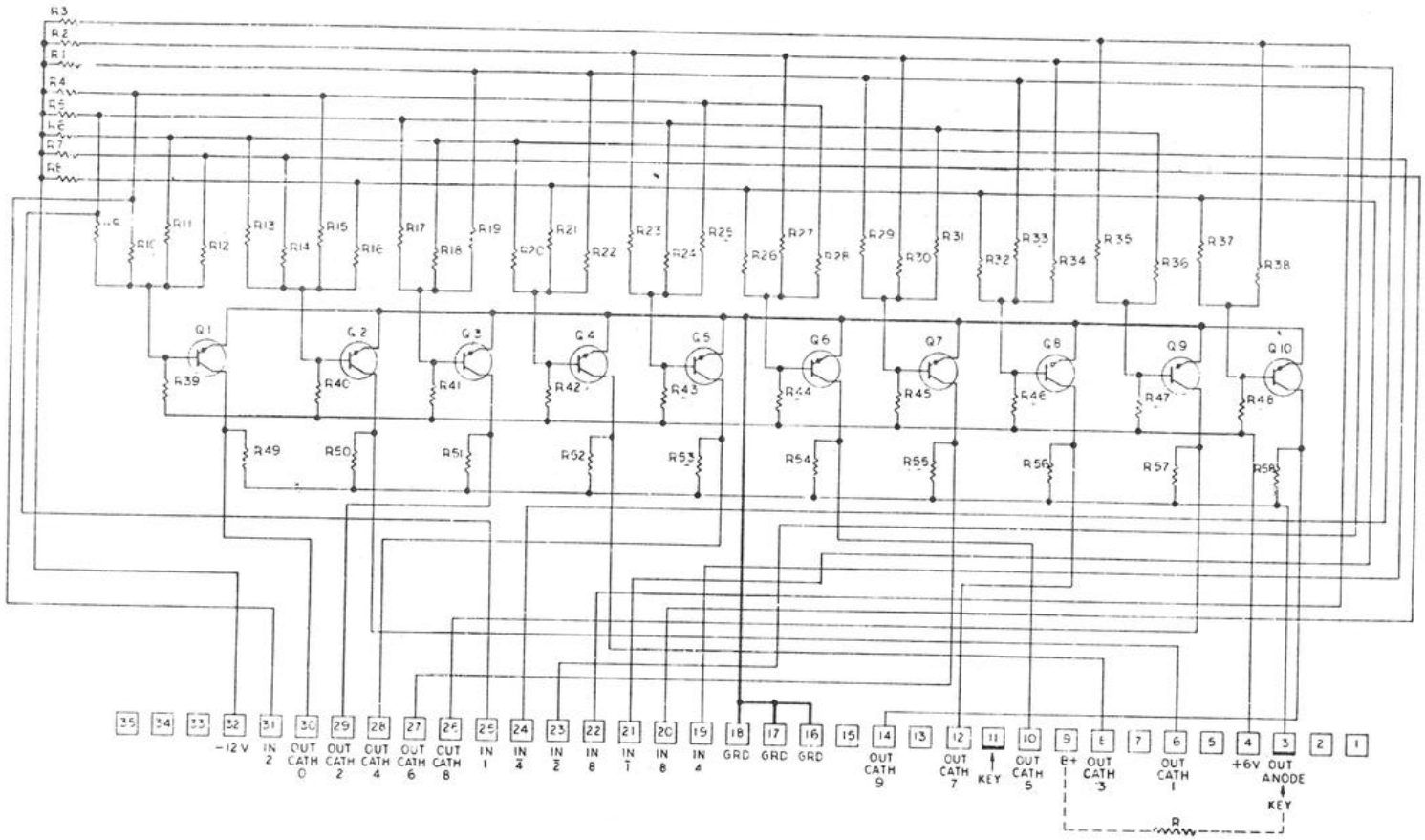
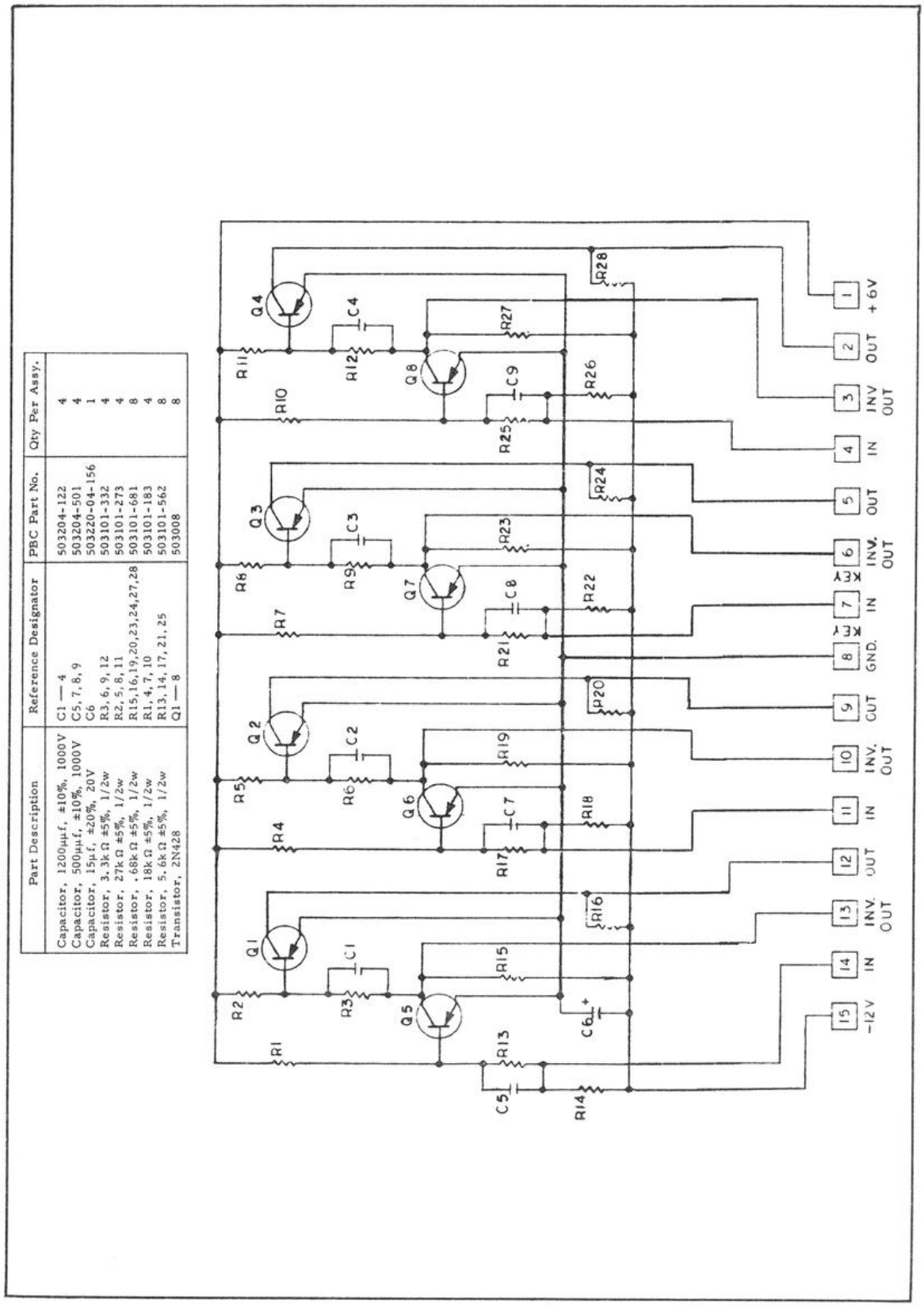


Figure 5-13. ND-100 Schematic and Parts List



Part Description	Reference Designator	PBC Part No.	Qty Per Assy.
Capacitor, 1200μμf, ±10%, 1000V	C1 — 4	503204-122	4
Capacitor, 500μμf, ±10%, 1000V	C5, 7, 8, 9	503204-501	4
Capacitor, 15μf, ±20%, 20V	C6	503220-04-156	1
Resistor, 3.3kΩ ±5%, 1/2w	R3, 6, 9, 12	503101-332	4
Resistor, 27kΩ ±5%, 1/2w	R2, 5, 8, 11	503101-273	4
Resistor, .68kΩ ±5%, 1/2w	R15, 16, 19, 20, 23, 24, 27, 28	503101-681	8
Resistor, 18kΩ ±5%, 1/2w	R1, 4, 7, 10	503101-183	4
Resistor, 5.6kΩ ±5%, 1/2w	R13, 14, 17, 21, 25	503101-562	8
Transistor, 2N428	Q1 — 8	503008	8

Figure 5-14. TD1-1 Schematic and Parts List

Part Description	Reference Designator	PBC Part No.	Qty Per Assy.
Capacitor, 500μμf, ±10%, 1000V	C1 — 16	503204-501	16
Diode	CR1 — 32	503051	32
Resistor, 27kΩ ±5%, 1/4w	R1 — 8	503100-273	8
Resistor, 1.8kΩ ±5%, 1/4w	R9 — 16	503100-182	8
Resistor, 4.7kΩ ±5%, 1/4w	R17 — 24	503100-472	8
Resistor, 5.6kΩ ±5%, 1/4w	R25 — 32	503100-562	8
Resistor, 39kΩ ±5%, 1/4w	R33 — 40	503100-393	8
Resistor, 1kΩ ±5%, 1/4w	R41 — 48	503100-102	8
Transistor, PNP, 2N1305	Q1 — 8	503748	8

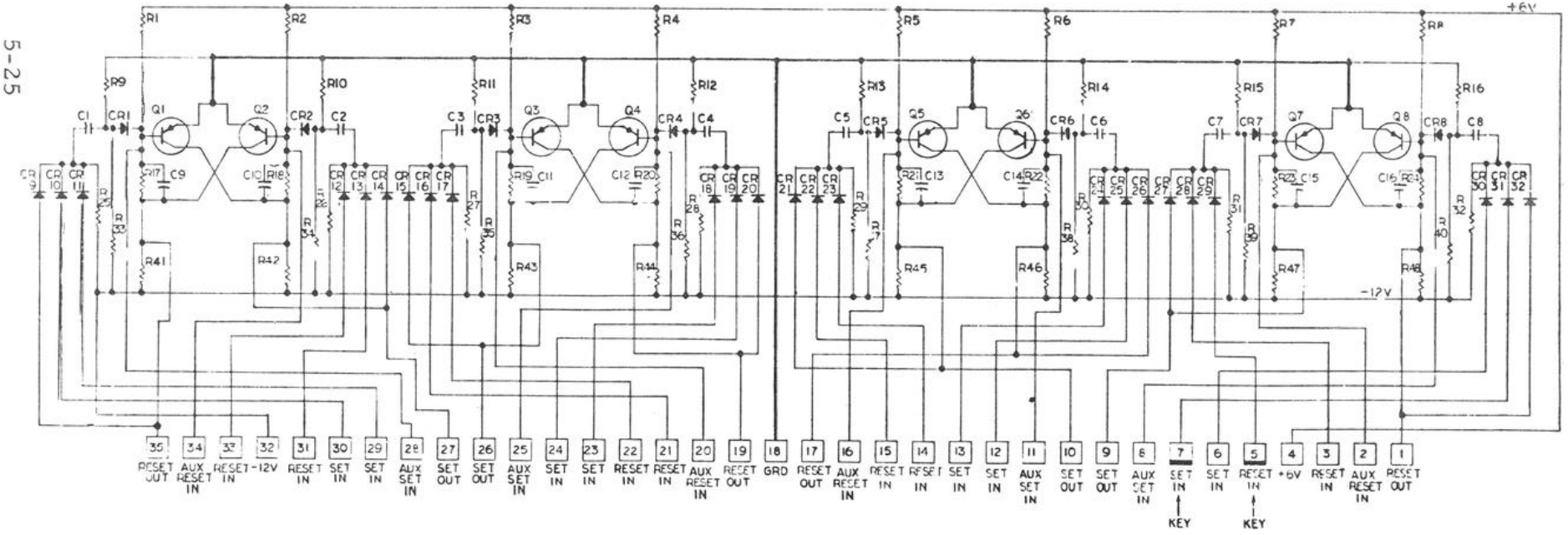


Figure 5-15. TF-101 Schematic and Parts List

Part Description	Reference Designator	PBC Part No.	Qty Per Assy.
Capacitor, .02μf, +60%-40%, 150V	C17	503203-203	1
Capacitor, 25μμf, ±10%, 75V	C9 — 16	503207-250	8
Capacitor, 50μμf, ±10%, 75V	C1 — 8	503207-500	8
Diode	CR1 — 32	503050	32
Resistor, 68k, ±5%, 1/4w	R1 — 8, R41 — 48	503100-683	16
Resistor, 2.2k, ±5%, 1/4w	R9 — 16	503100-222	8
Resistor, 4.7k, ±5%, 1/4w	R17 — 24	503100-472	8
Resistor, 5.6k, ±5%, 1/4w	R25 — 40	503100-562	16
Resistor, 1.5k, ±5%, 1/4w	R49 — 56	503100-152	8
Resistor, 100k, ±5%, 1/4w	R57 — 60	503100-104	4
Transistor, 2N1500	Q1 — 8	503003	8

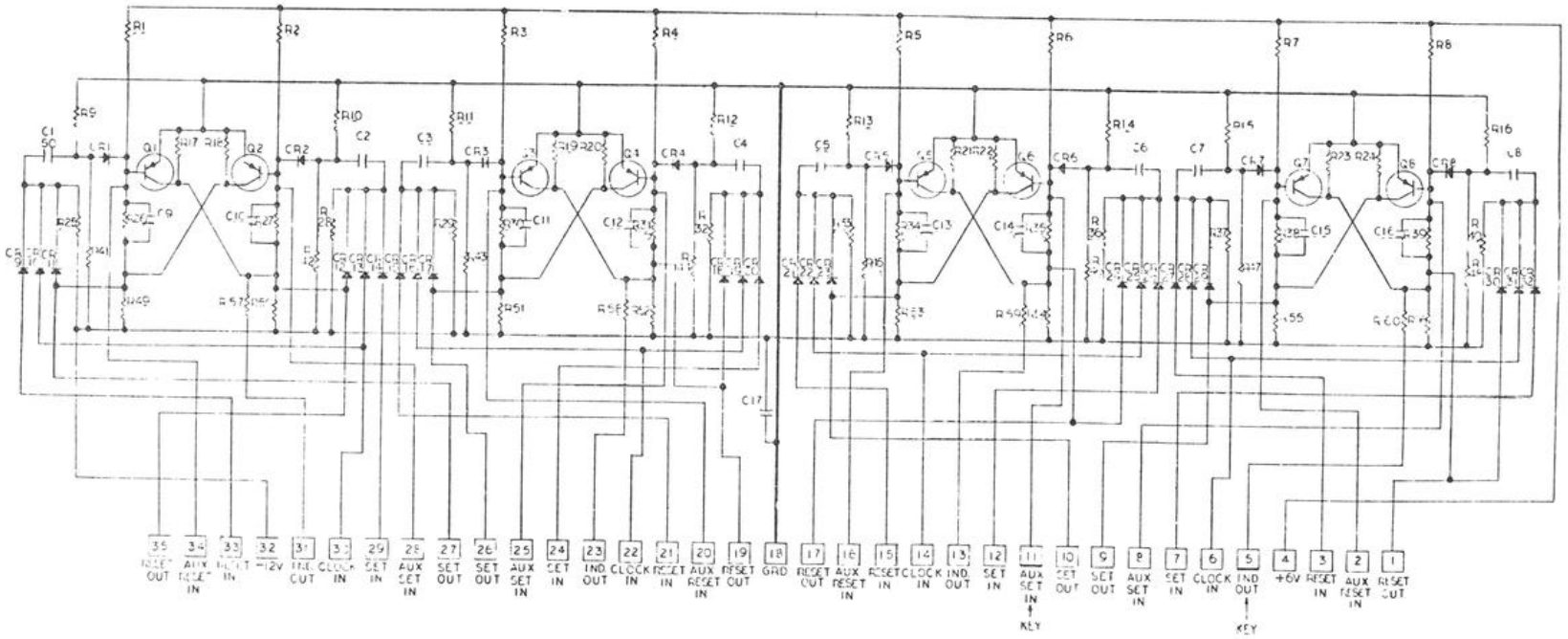


Figure 5-16. TF-102 Schematic and Parts List

Part Description	Reference Designator	PBC Part No.	Qty Per Assy
Capacitor, 500μμf, ±10%, 1000V	C1 — 6	503204-501	6
Resistor, 1.5k, ±5%, 1/4w	R14, 16, 18, 20, 22, 24	503100-152	6
Resistor, 15k, ±5%, 1/4w	R1 — 6	503100-153	6
Resistor, 4.7k, ±5%, 1/4w	R7 — 12	503100-472	6
Resistor, 5.6k, ±5%, 1/4w	R13, 15, 17, 19, 21, 23	503100-562	6
Transistor, PNP 2N1305	Q1 — 6	503748	6

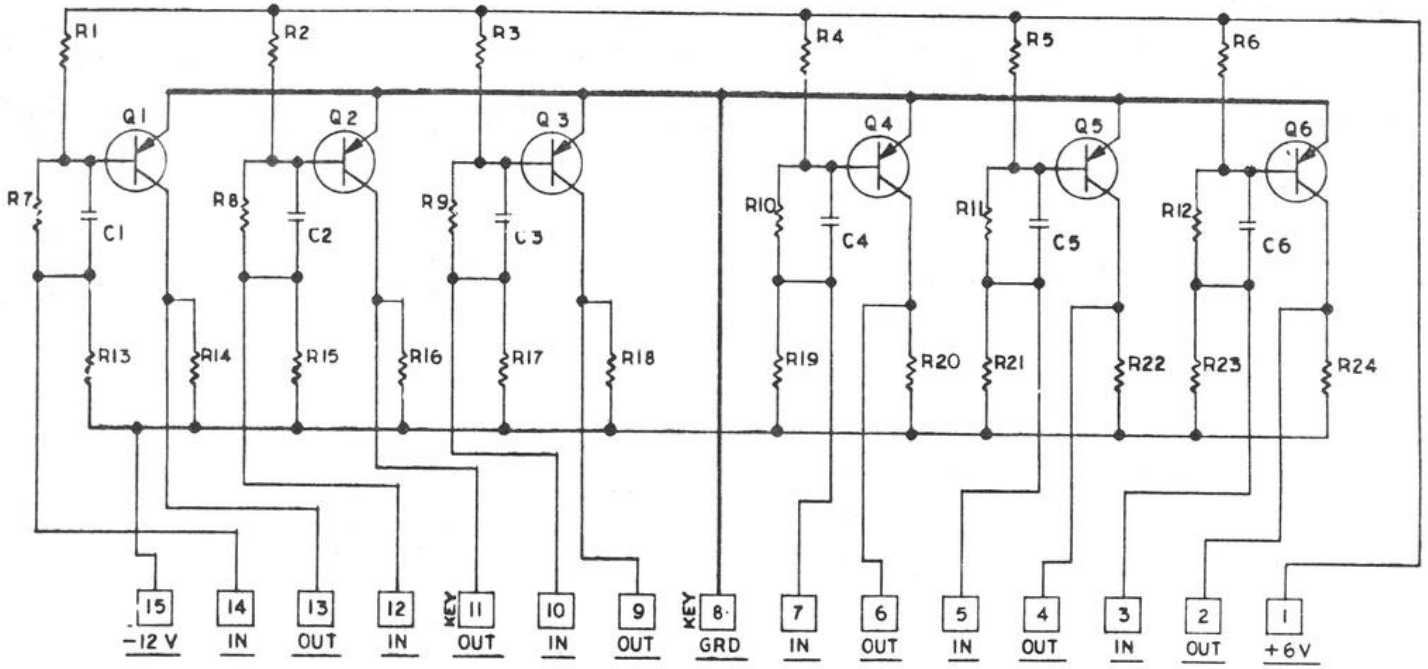


Figure 5-17. T1-3 Schematic and Parts List

Part Description	Reference Designator	PBC Part No.	Qty Per Assy
Capacitor, 25μf, ±10%, 100V	C1 — 12	503097-250	12
Capacitor, 15μf, ±20%, 20V	C13	503220-04-156	1
Resistor, 33k, ±5%, 1/4w	R1 — 12	503100-333	12
Resistor, 4.7k, ±5%, 1/4w	R13 — 24	503100-472	12
Resistor, 2.2k, ±5%, 1/4w	R25 — 36	503100-222	12
Resistor, 5.6k, ±5%, 1/4w	R37 — 63	503100-562	17
Transistor, 2N1500	Q1 — 12	503003	12

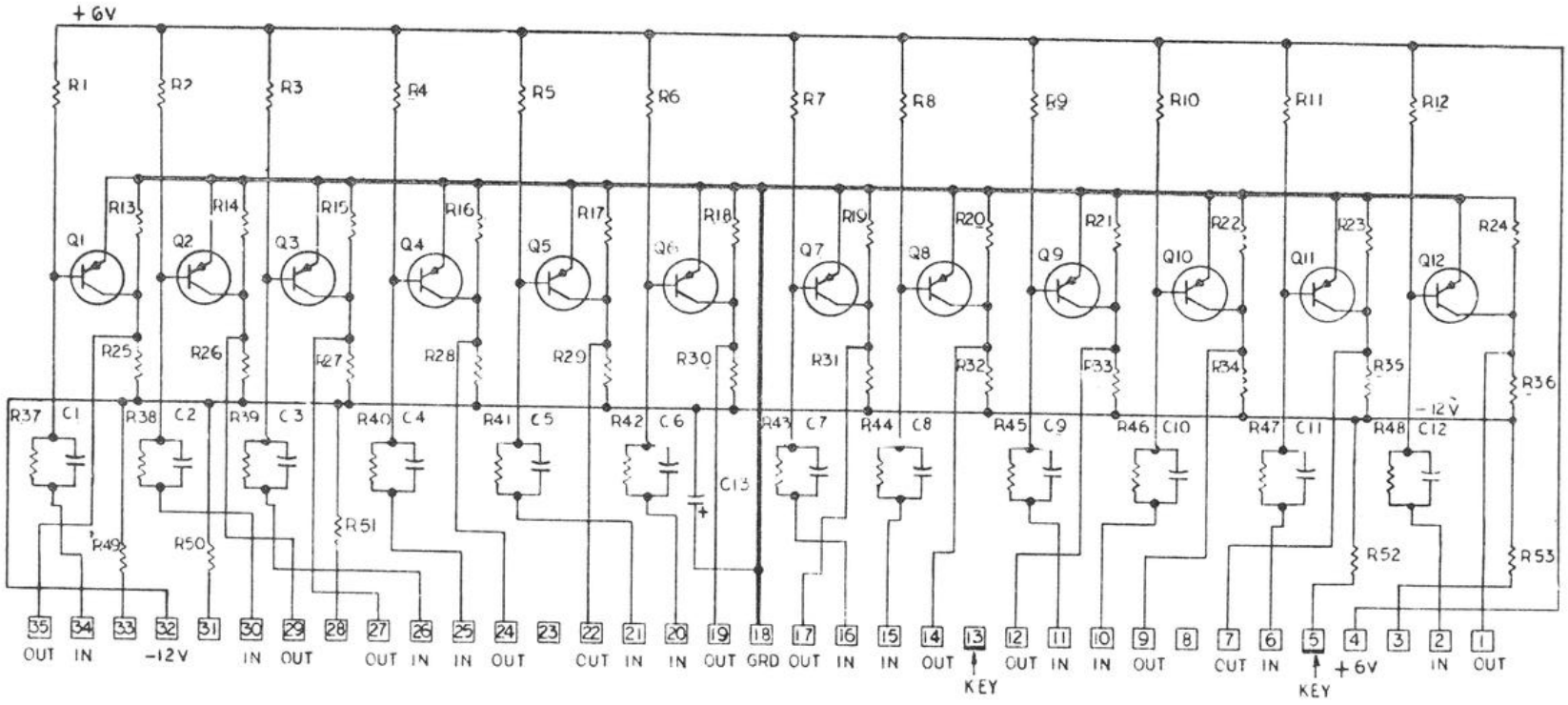


Figure 5-18. TI-100 Schematic and Parts List

Part Description	Reference Designator	PBC Part No.	Qty Per Assy.
Capacitor, 500μμf, ±10%, 1000V	C1 — 6	503204-501	6
Capacitor, 15μf, ±20%, 20V	C7	503840-156	1
Diode	CR1, 2	503051	2
Resistor, 5k, ±10%, .25w	R11, 16	503213-502	2
Resistor, 5.6kΩ ±5%, 1/2w	R5, 6	503101-562	2
Resistor, 560Ω ±5%, 1/2w	R12 — 15	503101-561	4
Resistor, 1.8kΩ, ±5%, 1/2w	R3, 4	503101-182	2
Resistor, 15kΩ ±5%, 1/2w	R1, 2	503101-153	2
Resistor, 39kΩ ±5%, 1/2w	R9, 10	503101-393	2
Resistor, 3.3kΩ ±5%, 1/2w	R7, 8	503101-332	2
Resistor, 10Ω ±5%, 1/2w	R17	503101-100	1
Transistor, PNP 2N1305	Q1 — 4	503748	4

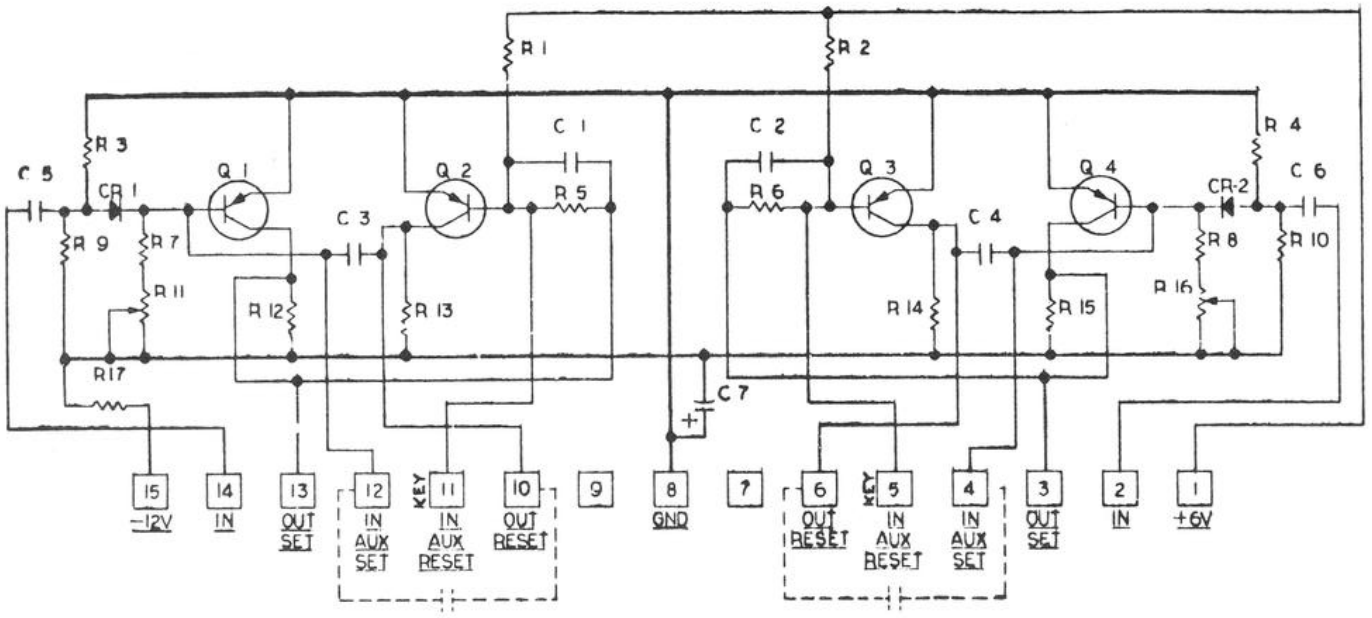


Figure 5-19. TO-3 Schematic and Parts List

Part Description	Reference Designation	PBC Part No.	Qty Per Assy.
Capacitor, ±10%, 1000V	C2	503204	1
Capacitor, .01μf, ±10%, 150V	C8	503203-103	1
Capacitor, .001μf, ±10%, 1000V	C6	503204-102	1
Capacitor, 100μμf, ±10%, 1000V	C7	503204-101	1
Capacitor, 15μμf, ±10%, 1000V	C4	503204-150	1
Capacitor, 25μμf, ±10%, 75V	C5	503207-250	1
Capacitor, 50μμf, ±10%, 75V	C1, 3	503207-500	2
Capacitor, 15μf, ±20%, 20V	C10	503220-4-156	1
Crystal, 2 mc	Y1	503221-2	1
Diode	CR1 — 4	503050	4
Inductor, 1 mh, ±5%	L1, 2	503044-102	2
Resistor, 47k Ω ±5%, 1/4w	R1	503100-473	1
Resistor, .12k Ω ±5%, 1/4w	R5	503100-121	1
Resistor, 1k Ω ±5%, 1/4w	R3, 4, 11	503100-102	3
Resistor, 1.2k Ω ±5%, 1/4w	R9	503100-122	1
Resistor, 1.5k Ω ±5%, 1/4w	R13	503100-152	1
Resistor, 1.8k Ω ±5%, 1/4w	R6, 8	503100-182	2
Resistor, 2.2k Ω ±5%, 1/4w	R14, 17	503100-222	2
Resistor, 4.7k Ω ±5%, 1/4w	R15	503100-472	1
Resistor, 5.6k Ω ±5%, 1/4w	R2, 12	503100-562	2
Resistor, 8.2k Ω ±5%, 1/4w	R7	503100-822	1
Resistor, 33k Ω ±5%, 1/4w	R16	503100-333	1
Transistor, 2N604	Q1, 2, 4, 6	503002	4
Transistor, 2N1500	Q3, 5	503003	2
Trimit, 2k Ω ±10%, 1/4w	R10	503213-202	1

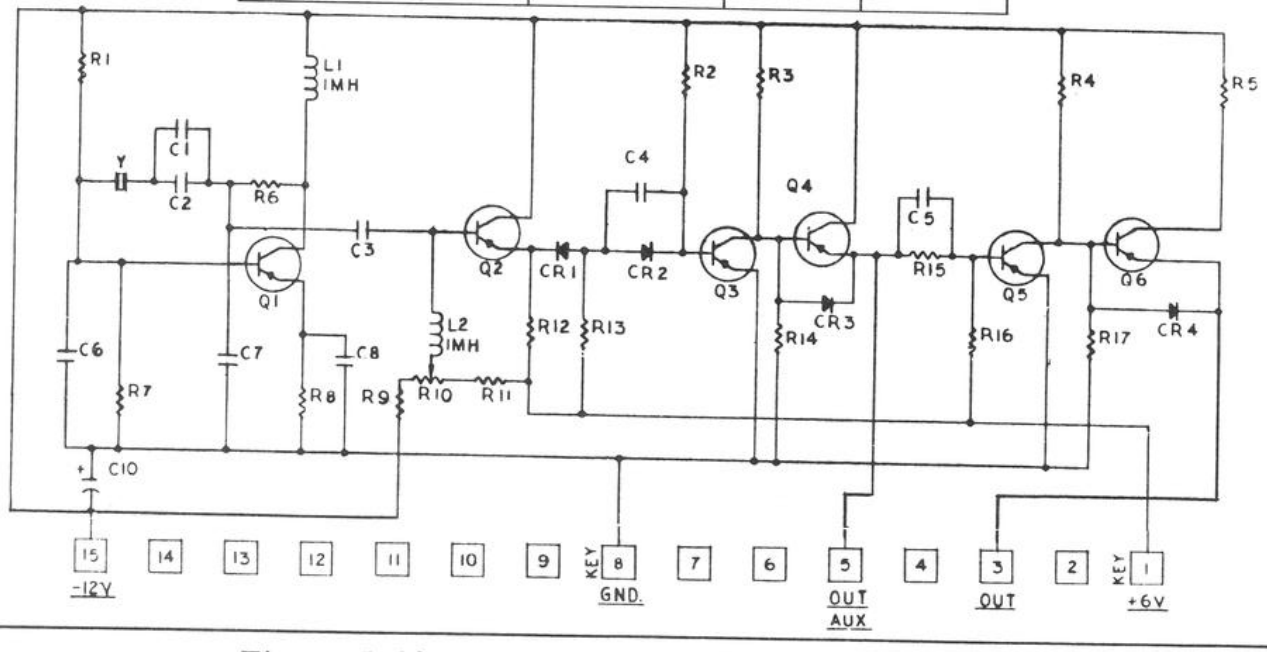


Figure 5-20. XCG-1 Schematic and Parts List

6. GLOSSARY AND LOGIC EQUATIONS

A. SCOPE OF SECTION

This section contains a glossary of terms and signals used within the TRICE system and complete set of logic equations for the individual units, excluding the TRICE computing modules. Refer to section 3 for logic equations of individual TRICE computing modules.

B. GLOSSARY

Individual signals used within the TRICE system are listed alphabetically and defined within Table 6-1.

C. LOGIC EQUATIONS

Logic equations for buffer register, control unit, converter scaler register, converter scaler control and reader punch are listed within this section.

Table 6-1.

GLOSSARY

Term	Definition
A	Character input mode flip-flop, on for address and punch-out modes
A1	Converter scaler mode flip-flop, on for binary shift and decimal exponent and register length conversion
A2	Converter scaler mode flip-flop, on for end around shift and scale exponent and register length conversion
A3	Converter scaler mode flip-flop, on for exponent conversion
A4	Converter scaler mode flip-flop, on for output (binary-to-decimal) conversion and punch output
A5	Converter scaler mode flip-flop, or for trailing zero input and clear
Ab	Address register input marker, on for block digit
Ain	Input to least significant end of decimal register
At	Address register input marker, on for tens digit
Au	Address register input marker, on for units digit
B1 - B6	Bits of character input code (B1 lowest bit)
$\overline{B1}$ - $\overline{B8}$	Decoded block address
Bc0 - Bc9	Decoded B1 - B4 (digit part of character input code)
Bes, Be7 - Be1	Scale (binary) exponent register
Bec	Shift clock for scale exponent register
Bi	Buffer register control flip-flop, on for bit input

Bic	Bit input code to buffer register
Bin	Binary bit input to most significant end of decimal register
Bip	Bit input pulse to buffer register
Boc	Bit output code from buffer register
Bop	Bit output control pulse to buffer register
Bp	Clock pulse of character input
C	Single cycle control flip-flop
C1 - C9	Most significant non-zero digit marker in decimal register
C2	Common contact signal of keyboard, goes false when key closes normally open contact
Cb	Reader or keyboard character input busy (interlock) flip-flop
Cd	Correct divide, correct signal for binary right shift in decimal register
Cin	Initial input to marker register C1 - C9
Ck	Right shift signal in marker register C1 - C9
Cℓ	(Converter-scaler) Left shift signal in marker register C1 - C9
Cℓ	(Control unit) "Single cycle" input from patchboard
Cℓ1	TRICE (3 Mc) clock
Cℓ2	PB250 (2 Mc) clock
Cℓa	Shift clock in address register
Cℓd	Shift clock in binary data register

Cm	Correct multiply, correct signal for binary left shift in decimal register
Co	Zero in marker register stages C2 - C9
Coc	Binary bit output code from converter scaler
Cop	Binary bit output control pulse from converter scaler
Cp	Reader or keyboard character input clock pulse
Cpg	PB250 character output clock pulse (PTU clock)
Cre	Converter reset
Cri	Converter read-in (transfer buffer-to-counter)
Cro	Converter read-out (transfer counter-to-buffer)
Cs	Converter read-out shift gate
Csc	Converter read-out shift clock
(Ct)	Common contact signal from KEYBOARD key
CV	Converter read-out data signal
Cvc	Convert clock
D	Character input mode flip-flop, on for display and punch-out modes
D18 - D11 ⋮ D98 - D91	Decimal register stages, D18 most significant bit of most significant digit
Db1 - Db4	Data digit input register
Des, De6 - Del	Decimal exponent register
Dec	Shift clock in decimal exponent register
Dip	Display pulse, initiates display cycle

Dp	Digit input clock pulse		
Dpa	Address digit input clock pulse		
Dpd	Data digit input clock pulse		
Ds	Sign of decimal register		
E1 - E6	Digit output register (output of converter scaler-to-punch)		
Ec	Shift clock in digit output register		
Ep	Character input clock pulse (A-I)		
Es	Block serial input-output enable signal in buffer register		
F_{ℓ}	Reader control input in reader punch		
Fp	Character input clock pulse (space, J-R)		
Fp0	Decoded character input pulse	space	= DATA
Fp1	"	J	= CONVERT DECIMAL EXPONENT
Fp2	"	K	= CONVERT SCALE EXPONENT
Fp3	"	L	= CONVERT REGISTER LENGTH
Fp5	"	N	= CONVERT INPUT
Fp6	"	O	= CONVERT OUTPUT
Fp7	"	P	= PUNCH OUTPUT
Fs	Serial fill gate (fill of TRICE modules)		
G	Compute on signal		

G1	Computing mode control timing
G2	Computing mode control interlock
Gc	Compute on flip-flop
Gdg	PB250 block serial output data signal
Gℓ	"Integrate" input from patchboard
Gp	Character input clock pulse ($, S-Z)
Gsg	PB250 block serial output shift gate
H	Computing mode control flip-flop, on for integrate and halt
Hdg	PB250 block serial input data signal
Hℓ	"Halt" input from patchboard
Hsg	PB250 block serial input shift gate
I	Computing mode control flip-flop, on for integrate and reset
If	Fill data signal
Iℓ	"Reset" input from patchboard
(IY)	TRICE module read-out data signal
K	Converter scaler control flip-flop, enables all sequential operations
(K1) - (K6)	Keyboard code contacts
Kb	Keyboard busy flip-flop
Kc	Any keyboard code on signal
L1 - L5	PB250 character output code (PTU code)

Lp	Clock pulse for patchboard input
M1 - M8	Punch input code (only M1- M6 used in TRICE)
Mc	Digit input register (Db1 - Db4) shift clock
Mc1, Mc2	Digit input register shift counter
Md	Digit input register shift control
Mℓ	Punch control input
Mm	Punch motor on
Mo	Punch logic on
Mp	Punch register set clock
N1 - N8	Punch register
Nc	Internal clock one shot in reader punch
Nd	Delay one shot (reader punch)
Nm	Motor start delay one shot (reader punch)
Np	Reader step, punch pulse one shot
Nr	Punch coil enable signal
Ns	Clear punch mechanism
Nt	Reader punch clock
Of1 - Of8	Overflow in TRICE block 1-8
Ofa	Analog computer overflow
Ofc	Converter overflow
Ofm	TRICE module or converter overflow
Oft	TRICE module overflow

P	Punch on flip-flop
P1, P4, P16	Decoded pulse times of T counter (TRICE word timing)
P30	End-of-word pulse
Pe	Even parity signal of input character decoding
Po	Odd parity signal of input character decoding
Pp	Punch pulse, pulse initiating preparation of a new output character in the converter scaler
Ppc	Same as Pp with T5 clock added
R	Reset timing flip-flop
R1 - R8	Reader code (only R1 - R6 used in TRICE)
Ra1 - Ra9	Address register
Rb	Reader punch busy
Rd1 - Rd32	Binary data buffer register
Rdc	Bit input flip-flop in buffer register
Rℓ	Reader control input
Rℓ5 - Rℓ1	Register length register
Rℓc	Shift clock in register length register
Rm	Reader motor on
Ro	Reader logic on
Rp	Patched reset signal
Rpc	Patched reset control flip-flop
Rs	Selected reset signal
Rsc	Selected reset control flip-flop

Rt	Total reset signal
Rtc	Total reset control flip-flop
S	Integrate slow control flip-flop
Ⓢ	Start internal clock in reader punch
Sb	Scaling bit flip-flop in converter scaler
Sc	Converter read-out shift control
Sd	Shift divide, right shift signal in decimal register
Sg	Shift gate flip-flop, controls any shift at the TRICE clock frequency in the buffer register
Si	Shift input flip-flop, controls filling from buffer-to-modules
Sm	Shift multiply, left shift signal in decimal register
So	Shift output flip-flop, controls read-out from modules to buffer
Sop	Shift output control pulse, initiates read-out
Sp	Sign input clock pulse
Spa	Address sign input clock pulse
Spd	Data sign input clock pulse
Sr	100 cps multivibrator
Ⓣ	KEYBOARD key signal direct to control mode flip-flop
T1 - T5	Pulse time counter, counts down the TRICE clock to form TRICE word timing
T51, T52	Countdown T5 for digit input timing
Te	Independent variable existence flip-flop

$T\ell$	"Keyboard" input from patchboard
Ts	Independent variable sign flip-flop
Tsc	Independent variable sign control flip-flop
U	Control mode flip-flop, on for reader and computer mode
Uo	Operation counter (U counter) zero signal
U1 - U8	Operation counter in converter scaler
$\overline{U0}$ - $\overline{U15}$	Decoded unit address
Ube	Operation counter equal to scale exponent
Uc	Operation counter clock
$Uc\ell$	Operation counter clear (clocked with T5)
Ude	Operation counter equal to decimal exponent
$U\ell$	"Reader" input from patchboard
Ur	End of operation
$Ur\ell$	Operation counter equal to register length
Us	Sign of operation counter, determines direction of operation
$V\ell$	"Computer" input from patchboard
W	Control mode flip-flop, on for computer and patchboard mode
$Y\ell$	"Patched reset" input from patchboard
$Z\ell$	"Compute off" input from patchboard

BUFFER REGISTER

$C\ell 1$ = TRICE (3 Mc) clock

$C\ell 2$ = PB250 (2 Mc) clock

Es = $(A\overline{D})(UW)$

$C\ell d$ = Es Gsg $C\ell 2$ + Es Hsg $C\ell 2$ + Sg $C\ell 1$

$C\ell a$ = Es Gsg $C\ell 2$

Si = $\overline{Si}$ Ep Bc6

Si

oSi = Si Sg

So = $\overline{So}$ Sop

So

oSo = So Sg

bi = $\overline{Bi}$ Bip $C\ell 1$

Bi

obi = Bi Sg P30 $C\ell 1$

Sg = $\overline{Sg}$ $C\ell 1$ [P30 Si + P1 So $\overline{Ra1}$ + P16(So Ra1) + P30 Bi]
+ P16 $C\ell 1$ Bop $\overline{Es}$

Sg

oSg = Sg $C\ell 1$ [P30 Si + P1 So $\overline{Ra1}$ + P16(So Ra1) + P30 Bi]
+ Sg $C\ell 1$ Bop

Sc = $\overline{Sc}$ $C\ell 1$ P1 Cro

Sc

oSc = Sc $C\ell 1$ P16

Fs = Si $\overline{Ra1}$ Sg

$$Cs = Si\ Ra1\ Sg + Sc$$

$$Cro = (So\ Ra1)\ Sg\ \overline{Sc}$$

$$Csc = Cs\ C\ell 1$$

$$Cri = Rt\ Ra1$$

$$Cre = Rt\ Ra1$$

$$Cvc = (GG2)\ T5\ T4\ \overline{T3}\ \overline{T2}$$

$$(CV) = DA1 + DA2 + DA3 + DA4 + DA5 + DA6 + AD1 + AD2 + AD3 + AD4 + AD5 + AD6$$

$$(I\text{-}Y) = \overline{Ra9}\ (Y1 + Y2 + Y3 + Y4 + Y5 + Y6 + Y7 + Y8) + Ra9\ (I1 + I2 + I3 + I4 + I5 + I6 + I7 + I8)$$

$$rdc = \overline{Rdc}\ Csc\ (CV) + Bi\ Sg\ C\ell 1\ Rd30 + Bi\ \overline{Sg}\ P30\ C\ell 1\ Bic + (So\ Ra1)\ P1\ C\ell 1$$

Rdc

$$ordc = Rdc\ Csc\ \overline{(CV)} + Bi\ Sg\ C\ell 1\ \overline{Rd30} + \overline{Sg}\ P1\ C\ell 1$$

$$rd1 = \overline{Rd1}\ C\ell d\ [Es\ Gsg\ Ra9 + So\ \overline{Ra1}\ (I\text{-}Y) + Sc\ Rdc + Bi\ Rdc + Bop\ Rd30]$$

Rd1

$$ord1 = Rd1\ C\ell d\ \overline{[Es\ Gsg\ Ra9 + So\ \overline{Ra1}\ (I\text{-}Y) + Sc\ Rdc + Bi\ Rdc + Bop\ Rd30]}$$

Rd2
⋮ Shift register, shift clock $C\ell d$
Rd29

$$rd30 = \overline{Rd30}\ C\ell d\ Rd29$$

Rd30

$$ord30 = Rd30\ C\ell d\ \overline{Rd29}$$

$$If = Rd30\ Si\ Sg$$

$$Boc = Rd1$$

$$Hdg = Rd30\ Hsg$$

$$Spa = Sp(A\overline{D})$$

$$Dpa = Dp(A\overline{D})$$

$$ab = \overline{Ab}\ Spa$$

Ab

$$oab = Ab\ Dpa$$

$$at = \overline{At}\ Dpa\ Ab$$

At

$$oat = At\ Dpa + Spa$$

$$au = \overline{Au}\ Dpa\ At$$

Au

$$oau = Au\ Dpa + Spa$$

$$ra1 = \overline{Ra1}\ C\ell a\ Gdg + Spa\ B1$$

Ra1

$$ora1 = Ra1\ C\ell a\ \overline{Gdg} + Spa\ \overline{B1}$$

$$ra2 = \overline{Ra2}\ C\ell a\ Ra1 + Ab\ Dpa\ B3$$

Ra2

$$ora2 = Ra2\ C\ell a\ \overline{Ra1} + Spa$$

$$ra3 = \overline{Ra3}\ C\ell a\ Ra2 + Ab\ Dpa\ B2$$

Ra3

$$ora3 = Ra3\ C\ell a\ \overline{Ra2} + Spa$$

$$ra4 = \overline{Ra4}\ C\ell a\ Ra3 + Ab\ Dpa\ B1$$

Ra4

$$ora4 = Ra4\ C\ell a\ \overline{Ra3} + Spa$$

$$ra5 = \overline{Ra5}\ C\ell a\ Ra4 + At\ Dpa\ B1$$

Ra5

$$ora5 = Ra5\ C\ell a\ \overline{Ra4} + Spa$$

$$ra6 = \overline{Ra6}\ C\ell a\ Ra5 + Au\ Dpa\ B3$$

Ra6

$$ora6 = Ra6\ C\ell a\ \overline{Ra5} + Spa$$

$$ra7 = \overline{Ra7}\ C\ell a\ Ra6 + Au\ Dpa\ B2$$

Ra7

$$ora7 = Ra7\ C\ell a\ \overline{Ra6} + Spa$$

$$ra8 = \overline{Ra8}\ C\ell a\ Ra7 + Au\ Dpa\ B1$$

Ra8

$$ora8 = Ra8\ C\ell a\ \overline{Ra7} + Spa$$

$$ra9 = \overline{Ra9}\ C\ell a\ Ra8 + (\overline{Ab}\ \overline{At}\ \overline{Au})\ Dpa\ B1$$

Ra9

$$ora9 = Ra9\ C\ell a\ \overline{Ra8} + (\overline{Ab}\ \overline{At}\ \overline{Au})\ Dpa\ \overline{B1}$$

$$\overline{B1} = Ra2 + Ra3 + \overline{Ra4}$$

$$\overline{B2} = Ra2 + \overline{Ra3} + Ra4$$

$$\overline{B3} = Ra2 + \overline{Ra3} + \overline{Ra4}$$

$$\overline{B4} = \overline{Ra2} + Ra3 + Ra4$$

$$\overline{B5} = \overline{Ra2} + Ra3 + \overline{Ra4}$$

$$\overline{B6} = \overline{Ra2} + \overline{Ra3} + Ra4$$

$$\overline{B7} = \overline{Ra2} + \overline{Ra3} + \overline{Ra4}$$

$$\overline{B8} = Ra2 + Ra3 + Ra4$$

$$\overline{U0} = Ra5 + Ra6 + Ra7 + Ra8$$

$$\overline{U1} = Ra5 + Ra6 + Ra7 + \overline{Ra8}$$

$$\overline{U2} = Ra5 + Ra6 + \overline{Ra7} + Ra8$$

$$\overline{U3} = Ra5 + Ra6 + \overline{Ra7} + \overline{Ra8}$$

$$\overline{U4} = Ra5 + \overline{Ra6} + Ra7 + Ra8$$

$$\overline{U5} = Ra5 + \overline{Ra6} + Ra7 + \overline{Ra8}$$

$$\overline{U6} = Ra5 + \overline{Ra6} + \overline{Ra7} + Ra8$$

$$\overline{U7} = Ra5 + \overline{Ra6} + \overline{Ra7} + \overline{Ra8}$$

$$\overline{U8} = \overline{Ra5} + Ra6 + Ra7 + Ra8$$

$$\overline{U9} = \overline{Ra5} + Ra6 + Ra7 + \overline{Ra8}$$

$$\overline{U10} = \overline{Ra5} + Ra6 + \overline{Ra7} + Ra8$$

$$\overline{U11} = \overline{Ra5} + Ra6 + \overline{Ra7} + \overline{Ra8}$$

$$\overline{U12} = \overline{Ra5} + \overline{Ra6} + Ra7 + Ra8$$

$$\overline{U13} = \overline{Ra5} + \overline{Ra6} + Ra7 + \overline{Ra8}$$

$$\overline{U14} = \overline{Ra5} + \overline{Ra6} + \overline{Ra7} + Ra8$$

$$\overline{U15} = \overline{Ra5} + \overline{Ra6} + \overline{Ra7} + \overline{Ra8}$$

$$t1 = \overline{\overline{T1}}\, C\ell 1$$

T1

$$ot1 = T1\, C\ell 1$$

$$t2 = \overline{\overline{T2}}\, C\ell 1 (T1\, \overline{P16})$$

T2

$$ot2 = T2\, C\ell 1 (T1\, \overline{P16})$$

$$t3 = \overline{\overline{T3}}\, C\ell 1 (T2\, T1)$$

T3

$$ot3 = T3\, C\ell 1 (T2\, T1)$$

$$t4 = \overline{\overline{T4}}\, C\ell 1 (T3\, T2\, T1)$$

T4

$$ot4 = T4\, C\ell 1\, (T3\, T2\, T1)$$

$$t5 = \overline{\overline{T5}}\, C\ell 1 (T4\, T3\, T2\, T1)$$

T5

$$ot5 = T5\, C\ell 1 (T4\, T3\, T2\, T1)$$

$$P30 = \overline{P30}\ C\ell 1 (T5\ T4\ T3\ T2\ \overline{T1})$$

P30

$$oP30 = P30\ C\ell 1$$

$$P1 = \overline{P1}\ C\ell 1\ P30$$

P1

$$oP1 = P1\ C\ell 1$$

$$P4 = \overline{P4}\ C\ell 1 (\overline{T5}\ \overline{T4}\ \overline{T3}\ T2\ \overline{T1})$$

P4

$$oP4 = P4\ C\ell 1$$

$$P16 = \overline{T5}\ T4\ T3\ T2\ T1$$

CONTROL UNIT

$$u = \overline{U}\ Lp\ V\ell + Gp\ Bc4 + Gp\ Bc5 + \overline{U}\ Lp\ U\ell$$

U

$$ou = U\ Gp\ Bc3 + Gp\ Bc6 + \textcircled{T}$$

$$w = \overline{W}\ Gp\ Bc5 + Gp\ Bc6$$

W

$$ow = W\ Gp\ Bc3 + Gp\ Bc4 + Lp\ U\ell + Lp\ T\ell + \textcircled{T}$$

$$a = \overline{A}\ Ep\ Bc1 + Fp\ Bc7$$

A

$$oa = A\ Ep\ Bc4 + Fp\ Bc0$$

$$d = \overline{D}\ Ep\ Bc4 + Fp\ Bc7$$

D

$$od = D\ Ep\ Bc1 + Fp\ Bc0$$

$$p = \overline{P}\ Fp\ Bc7$$

P

$$op = P\ Ep\ Bc1$$

$$kb = \overline{Kb}\ \textcircled{C2}\ \textcircled{Ct}$$

Kb

$$okb = Kb\ Kc$$

$$Kc = \textcircled{K1} + \textcircled{K2} + \textcircled{K3} + \textcircled{K4} + \textcircled{K5} + \textcircled{K6}$$

$$cp = \overline{Cp}\ T5\,(Kb\ \overline{Cb}\ \overline{U} + \overline{Rb}\ U\overline{W} + \overline{Rb}\ P\ A4\ \overline{Kb})$$

Cp

$$ocp = Cp\ T5$$

$$cb = \overline{Cb}\ T5\ Cp$$

Cb

$$ocb = Cb\ T5\ \overline{Kb}$$

$$Pp = Cp\ AD$$

$$Bp = \overline{W}\ Cp + UW\ Cpg$$

$$B1 = \overline{U}\,\overline{W}\ (K1) + U\overline{W}\ R1 + UW\ L1$$

$$B2 = \overline{U}\,\overline{W}\ (K2) + U\overline{W}\ R2 + UW\ L2$$

$$B3 = \overline{U}\,\overline{W}\ (K3) + U\overline{W}\ R3 + UW\ L3$$

$$B4 = \overline{U}\,\overline{W}\ (K4) + U\overline{W}\ R4 + UW\ L4$$

$$B5 = \overline{U}\,\overline{W}\ (K5) + U\overline{W}\ R5 + UW\ L5$$

$$B6 = \overline{U}\,\overline{W}\ (K6) + U\overline{W}\ R6 + UW$$

$$Bc0 = \overline{B4}\ \overline{B3}\ \overline{B2}\ \overline{B1}$$

$$Bc1 = \overline{B4}\ \overline{B3}\ \overline{B2}\ B1$$

$$Bc2 = \overline{B4}\ \overline{B3}\ B2\ \overline{B1}$$

$$Bc3 = \overline{B4}\ \overline{B3}\ B2\ B1$$

$$Bc4 = \overline{B4}\ B3\ \overline{B2}\ \overline{B1}$$

$$Bc5 = \overline{B4}\ B3\ \overline{B2}\ B1$$

$$Bc6 = \overline{B4}\ B3\ B2\ \overline{B1}$$

$$Bc7 = \overline{B4}\ B3\ B2\ B1$$

$$Bc8 = B4\ \overline{B3}\ \overline{B2}\ \overline{B1}$$

$$Bc9 = B4\ \overline{B3}\ \overline{B2}\ B1$$

$$Pe = Bc3 + Bc5 + Bc6 + Bc9$$

$$Po = Bc1 + Bc2 + Bc4 + Bc7 + Bc8$$

$$Dp = Bp\,(\overline{B6}\ \overline{B5}\ Po + \overline{B6}\ B5\ Pe + B6\ \overline{B5}\ Bco)$$

$$Ep = Bp\,(B6\ \overline{B5}\ Po + B6\ B5\ Pe)$$

$$Fp = Bp(\overline{B6}\ B5\ Po + \overline{B6}\ \overline{B5}\ Pe + \overline{B6}\ B5\ Bco)$$

$$Gp = Bp(B6\ B5\ Po + B6\ \overline{B5}\ Pe)$$

$$Sp = Bp\ \overline{B6}\ B5\ B4\ B3\ B2$$

$$Lp = \overline{U}W\ T5$$

$$Sop = Ep\ Bc5 + Dip$$

$$Dpd = Dp\ \overline{A}\,\overline{D}$$

$$Spd = Sp\ \overline{A}\,\overline{D}$$

$$md = \overline{Md}\ Dpd$$

Md

$$omd = Md\ Mc2$$

$$t51 = \overline{T51}\ T5$$

T51

$$ot51 = T51\ T5$$

$$t52 = \overline{T52}\ T51$$

T52

$$ot52 = T52\ T51$$

$$Mc = Md\ T51\ T52$$

$$mc1 = \overline{Mc1}\ Mc$$

Mc1

$$omc1 = Mc1\ Mc + \overline{Dpd}$$

$$mc2 = \overline{Mc2}\ Mc1$$

Mc2

$$omc2 = Mc2\ Mc1 + \overline{Dpd}$$

$$db1 = Dpd\ B1$$

Db1

$$odb1 = Db1\ Mc + \overline{Dpd}$$

$db2 = \overline{\overline{Db2}}\ Mc\ Db1 + Dpd\ B2$

Db2

$0db2 = Db2\ Mc\ \overline{\overline{Db1}} + \overline{\overline{Dpd}}$

$db3 = \overline{\overline{Db3}}\ Mc\ Db2 + Dpd\ B3$

Db3

$odb3 = Db3\ Mc\ \overline{\overline{Db2}} + \overline{\overline{Dpd}}$

$db4 = \overline{\overline{Db4}}\ Mc\ Db3 + Dpd\ B4$

Db4

$odb4 = Db4\ Mc\ \overline{\overline{Db3}} + \overline{\overline{Dpd}}$

$Bic = Db4\ Md + Coc$

$Bip = (\overline{\overline{Mc1}}\ \overline{\overline{Mc2}})\ Mc + Cop$

$M1 = AD\ E1 + (\overline{\overline{AD}})\ B1$

$M2 = AD\ E2 + (\overline{\overline{AD}})\ B2$

$M3 = AD\ E3 + (\overline{\overline{AD}})\ B3$

$M4 = AD\ E4 + (\overline{\overline{AD}})\ B4$

$M5 = AD\ E5 + (\overline{\overline{AD}})\ B5$

$M6 = AD\ E6 + (\overline{\overline{AD}})\ B6$

Sr 100 cps multivibrator

$dip = \overline{\overline{Dip}}\ Sr(D\overline{A})$

Dip

$odip = Dip\ T5$

$h = \overline{H}\ Lp\ H\ell + \overline{H}\ Lp\ G\ell + Ep\ Bc8 + Ep\ Bc7$

H

$oh = H\ Lp\ Z\ell + H\ Lp\ I\ell + Ep\ Bc9 + Gp\ Bc9$

$i = \overline{I}\ Lp\ G\ell + \overline{I}\ Lp\ I\ell + Ep\ Bc9 + Ep\ Bc7$

I

$oi = I\ Lp\ Z\ell + I\ Lp\ H\ell + Ep\ Bc8 + Gp\ Bc9$

$$s = \overline{S}\ Gp\ Bc2$$

S

$$os = S\ T5\ \overline{H} + Ep\ Bc8$$

$$c = \overline{C}\ Lp\ C\ell + Ep\ Bc3 + Sr\ S$$

C

$$oc = C\ T5\ Te$$

$$te = \overline{\overline{Te}}\ T5\ C + \overline{\overline{Te}}\ T5\ HI$$

Te

$$ote = Te\ T5\ (\overline{\overline{HI}})$$

$$tsc = \overline{\overline{Tsc}}\ Sp\ \overline{A}\ D\ \overline{\overline{B1}}$$

Tsc

$$otsc = Tsc\ Sp\ \overline{A}\ D\ B1$$

$$ts = \overline{\overline{Ts}}\ T5\ Tsc$$

Ts

$$ots = Ts\ T5\ \overline{\overline{Tsc}}$$

$$gc = \overline{\overline{Gc}}\ T5\ H$$

Gc

$$ogc = Gc\ T5\ \overline{H}$$

$$g1 = \overline{\overline{G1}}\ \overline{R} + \overline{\overline{G1}}\ T5\ H\ Gc$$

G1

$$og1 = G1\ T5\ \overline{H}\ G2 + G1\ T5\ G2(Rsc + Rpc + Rtc)$$

$$G = Gc\ \overline{R}$$

$$g2 = \overline{\overline{G2}}\ T5\ G1$$

G2

$$og2 = G2\ T5\ \overline{\overline{G1}}$$

$$rsc = \overline{\overline{Rsc}}\ Gp\ Bc7$$

Rsc

$$orsc = Rsc(G2\ R)$$

$$rpc = \overline{\overline{Rpc}}\ Gp\ Bc8 + \overline{R}\ Lp\ Y\ell$$

Rpc

$$orpc = Rpc\ (G2\ R)$$

$$rtc = \overline{\overline{Rtc}}\ Ep\ Bc9 + \overline{R}\ Lp\ I\ell$$

Rtc

$$ortc = Rtc\ (G2\ R)$$

$$r = \overline{R}\ T5\ \overline{\overline{G1}}\ (Rsc + Rpc + Rtc)$$

R

$$or = R\ T5\ \overline{\overline{G1}}$$

$$Rs = Rsc\ R$$

$$Rp = Rpc\ R$$

$$Rt = Rtc\ R$$

$$Oft = Of1 + Of2 + Of3 + Of4 + Of5 + Of6 + Of7 + Of8$$

$$Ofm = Oft + Ofc$$

Keyboard Lights

keyboard	$= \overline{U}\,\overline{W}$	compute off	$= \overline{\overline{HI}}$
reader	$= U\overline{W}$	reset	$= \overline{HI}$
computer	$= UW$	halt	$= \overline{\overline{HI}}$
patchboard	$= \overline{U}W$	integrate	$= HI$
address	$= A\overline{D}$	integrate slow	$= S$
display	$= \overline{A}D$	+	$= Tsc$
data	$= \overline{A}\,\overline{D}$	−	$= \overline{\overline{Tsc}}$
punch out	$= AD$		

CONVERTER SCALER REGISTER

$$d18 = \overline{D18}\ T5\,[\,Sd\ D91\ \overline{C1}\,(\overline{A3}\ A2) + Sm\ D14\,(\overline{C\ell\ C2}) + Cm\ D14\ D12 + Cm\ D14\ D11\,] + Sb\ Sd\ T5\ Bin$$

D18

$$od18 = D18\ T5\,[\,Sd\ \overline{D91}\,(\overline{A3}\ A2) + Sd\ C1\,(\overline{A3}\ A2) + Sm\ \overline{D14} + Cd\ \overline{D14}\ \overline{D12} + Cd\ \overline{D14}\ \overline{D11} + (C\ell\ C2)\,] + Sb\ Sd\ T5\ \overline{Bin}$$

$$d14 = \overline{D14}\ T5\,[Sd\ D18 + Sm\ D12\,(\overline{C\ell\ C2}) + Cd\ D18\ \overline{D14}\ \overline{D12} + Cd\ D18\ \overline{D14}\ \overline{D11} + Cm\ D18\ D11]$$

D14

$$od14 = D14\ T5\,[Sd\ \overline{D18} + Sm\ \overline{D12} + Cd\ D18\ D14 + Cm\ D14\ D12 + Cm\ D14\ D11 + (C\ell\ C2)\,]$$

$$d12 = \overline{D12}\ T5\,[Sd\ D14 + Sm\ D11\,(\overline{C\ell\ C2}) + Cd\ D18\ \overline{D12}\ D11 + Cm\ D18\ \overline{D11}]$$

D12

$$od12 = D12\ T5\,[Sd\ \overline{D14} + Sm\ \overline{D11} + Cd\ D18\ D12\ D11 + Cm\ D14\ D12\ \overline{D11} + (C\ell\ C2)\,]$$

$$d11 = \overline{D11}\ T5\,[\,Sd\ D12 + Sm\ D28 + Cd\ D18\ \overline{D11} + Cm\ D14\ D12\ \overline{D11} + Cm\ D18\ \overline{D11}\,]$$

D11

$$od11 = D11\ T5\,[\,Sd\ \overline{D12} + Sm\ \overline{D28} + Cd\ D18\ D11 + Cm\ D18\ D11 + Cm\ D14\ D11 + \overline{Sm}\ (C\ell\ C2)\,]$$

Decade 1

CONVERTER SCALER REGISTER

$$d28 = \overline{D28}\ T5\ [Sd\ D11\ \overline{C2} + Sm\ D24\ (\overline{C\ell\ C3}) + Cm\ D24\ D22 + Cm\ D24\ D21]$$

D28

$$od28 = D28\ T5\ [Sd\ \overline{D11} + Sd\ C2 + Sm\ \overline{D24} + Cd\ \overline{D24}\ \overline{D22} + Cd\ \overline{D24}\ \overline{D21} + (C\ell\ C3)]$$

$$d24 = \overline{D24}\ T5\ [Sd\ D28 + Sm\ D22\ (\overline{C\ell\ C3}) + Cd\ D28\ \overline{D24}\ \overline{D22} + Cd\ D28\ \overline{D24}\ \overline{D21} + Cm\ D28\ D21]$$

D24

$$od24 = D24\ T5\ [Sd\ \overline{D28} + Sm\ \overline{D22} + Cd\ D28\ D24 + Cm\ D24\ D22 + Cm\ D24\ D21 + (C\ell\ C3)]$$

$$d22 = \overline{D22}\ T5\ [Sd\ D24 + Sm\ D21\ (\overline{C\ell\ C3}) + Cd\ D28\ \overline{D22}\ D21 + Cm\ D28\ \overline{D21}]$$

D22

$$od22 = D22\ T5\ [Sd\ \overline{D24} + Sm\ \overline{D21} + Cd\ D28\ D22\ D21 + Cm\ D24\ D22\ \overline{D21} + (C\ell\ C3)]$$

$$d21 = \overline{D21}\ T5\ [Sd\ D22 + Sm\ D38 + Cd\ D28\ \overline{D21} + Cm\ D24\ D22\ \overline{D21} + Cm\ D28\ \overline{D21}]$$

D21

$$od21 = D21\ T5\ [Sd\ \overline{D22} + Sm\ \overline{D38} + Cd\ D28\ D21 + Cm\ D28\ D21 + Cm\ D24\ D21 + \overline{Sm}\ (C\ell\ C3)]$$

Decade 2 (typical 2-8)

CONVERTER SCALER REGISTER

$$d98 = \overline{D98}\ T5\ [Sd\ D81\ \overline{C9} + Sm\ D94(\overline{C\ell\ C1}) + Cm\ D94\ D92 + Cm\ D94\ D91]$$

D98

$$od98 = D98\ T5\ [Sd\ \overline{D81} + Sd\ C9 + Sm\ \overline{D94} + Cd\ \overline{D94}\ \overline{D92} + Cd\ \overline{D94}\ \overline{D91} + (C\ell\ C1)]$$

$$d94 = \overline{D94}\ T5\ [Sd\ D98 + Sm\ D92(\overline{C\ell\ C1}) + Cd\ D98\ \overline{D94}\ \overline{D92} + Cd\ D98\ \overline{D94}\ \overline{D91} + Cm\ D98\ D91]$$

D94

$$od94 = D94\ T5\ [Sd\ \overline{D98} + Sm\ \overline{D92} + Cd\ D98\ D94 + Cm\ D94\ D92 + Cm\ D94\ D91 + (C\ell\ C1)]$$

$$d92 = \overline{D92}\ T5\ [Sd\ D94 + Sm\ D91(\overline{C\ell\ C1}) + Cd\ D98\ \overline{D92}\ D91 + Cm\ D98\ \overline{D91}]$$

D92

$$od92 = D92\ T5\ [Sd\ \overline{D94} + Sm\ \overline{D91} + Cd\ D98\ D92\ D91 + Cm\ D94\ D92\ \overline{D91} + (C\ell\ C1)]$$

$$d91 = \overline{D91}\ T5\ [Sd\ D92 + Sm\ Ain + Cd\ D98\ \overline{D91} + Cm\ D94\ D92\ \overline{D91} + Cm\ D98\ \overline{D91}]$$

D91

$$od91 = D91\ T5\ [Sd\ \overline{D92} + Sm\ \overline{Ain} + Cd\ D98\ D91 + Cm\ D98\ D91 + Cm\ D94\ D91 + \overline{Sm}(C\ell\ C1)]$$

Decade 9

CONVERTER SCALER REGISTER

$$c1 = \overline{C1}\,(T5\ C\ell)\ C2 + (T5\ Ck)\ C9 + Cin\ T5$$

C1

$$oc1 = C1\ T5\ (C\ell + Ck) + C1\ T5\ \overline{A2}$$

$$c2 = \overline{C2}\,(T5\ C\ell)\ C3 + (T5\ Ck)\ C1$$

C2

$$oc2 = C2\ T5\,(C\ell + Ck)$$

$$c3 = \overline{C3}\ (T5\ C\ell)\ C4 + (T5\ Ck)\ C2$$

C3

$$oc3 = C3\ T5\ (C\ell + Ck)$$

$$c4 = \overline{C4}\,(T5\ C\ell)\ C5 + (T5\ Ck)\ C3$$

C4

$$oc4 = C4\ T5\ (C\ell + Ck)$$

$$c5 = \overline{C5}\,(T5\ C\ell)\ C6 + (T5\ Ck)\ C4$$

C5

$$oc5 = C5\ T5\ (C\ell + Ck)$$

$$c6 = \overline{C6}\,(T5\ C\ell)\ C7 + (T5\ Ck)\ C5$$

C6

$$oc6 = C6\ T5\ (C\ell + Ck)$$

$$c7 = \overline{C7}\,(T5\ C\ell)\ C8 + (T5\ Ck)\ C6$$

C7

$$oc7 = C7\ T5\ (C\ell + Ck)$$

$$c8 = \overline{C8}\,(T5\ C\ell)\ C9 + (T5\ Ck)\ C7$$

C8

$$oc8 = C8\ T5\ (C\ell + Ck)$$

$$c9 = \overline{C9}\,(T5\ C\ell)\ C1 + (T5\ Ck)\ C8$$

C9

$$oc9 = C9\ T5\ (C\ell + Ck)$$

CONVERTER SCALER REGISTER

$$C_{\ell} = (Sm\ D18\ C1) + (Sm\ D28\ C2) + (Sm\ D38\ C3) + (Sm\ D48\ C4) + (Sm\ D58\ C5) + (Sm\ D68\ C6) + (Sm\ D78\ C7) + (Sm\ D88\ C8) + (Sm\ D98\ C9) + \overline{C1}\ \overline{Co}\ \overline{A2}$$

$$Ck = Sd\ [(\overline{D18}\ \overline{D14}\ \overline{D12}\ C1) + (\overline{D28}\ \overline{D24}\ \overline{D22}\ C2) + (\overline{D38}\ \overline{D34}\ \overline{D32}\ C3) + (\overline{D48}\ \overline{D44}\ \overline{D42}\ C4) + (\overline{D58}\ \overline{D54}\ \overline{D52}\ C5) + (\overline{D68}\ \overline{D64}\ \overline{D62}\ C6) + (\overline{D78}\ \overline{D74}\ \overline{D72}\ C7) + (\overline{D88}\ \overline{D84}\ \overline{D82}\ C8) + (\overline{D98}\ \overline{D94}\ \overline{D92}\ C9)]$$

$$Co = \overline{C2}\ \overline{C3}\ \overline{C4}\ \overline{C5}\ \overline{C6}\ \overline{C7}\ \overline{C8}\ \overline{C9}$$

CONVERTER SCALER CONTROL

$$del = \overline{De1}\ Dec\ De2$$

De1

$$ode1 = De1\ Dec\ \overline{De2}$$

$$de2 = \overline{De2}\ Dec\ De3$$

De2

$$ode2 = De2\ Dec\ \overline{De3}$$

$$de3 = \overline{De3}\ Dec\ De4$$

De3

$$ode3 = De3\ Dec\ \overline{De4}$$

$$de4 = \overline{De4}\ Dec\ De5$$

De4

$$ode4 = De4\ Dec\ \overline{De5}$$

$$de5 = \overline{De5}\ Dec\ De6$$

De5

$$ode5 = De5\ Dec\ \overline{De6}$$

$$de6 = \overline{De6}\ Dec\ D91$$

De6

$$ode6 = De6\ Dec\ \overline{D91}$$

$$des = \overline{Des}\ Fp1\ Ds$$

Des

$$odes = Des\ Fp1\ \overline{Ds}$$

$$bel = \overline{Be1}\ Bec\ Be2$$

Bel

$$obel = Bel\ Bec\ \overline{Be2}$$

be2 = $\overline{\text{Be2}}$ Bec Be3
Be2
obe2 = Be2 Bec $\overline{\text{Be3}}$

be3 = $\overline{\text{Be3}}$ Bec Be4
Be3
obe3 = Be3 Bec $\overline{\text{Be4}}$

be4 = $\overline{\text{Be4}}$ Bec Be5
Be4
obe4 = Be4 Bec $\overline{\text{Be5}}$

be5 = $\overline{\text{Be5}}$ Bec Be6
Be5
obe5 = Be5 Bec $\overline{\text{Be6}}$

be6 = $\overline{\text{Be6}}$ Bec Be7
Be6
obe6 = Be6 Bec $\overline{\text{Be7}}$

be7 = $\overline{\text{Be7}}$ Bec D91
Be7
obe7 = Be7 Bec $\overline{\text{D91}}$

bes = $\overline{\text{Bes}}$ Fp2 Ds
Bes
obes = Bes Fp2 $\overline{\text{Ds}}$

rℓ1 = $\overline{\text{R}\ell\text{1}}$ Rℓc Rℓ2
Rℓ1
orℓ1 = Rℓ1 Rℓc $\overline{\text{R}\ell\text{2}}$

rℓ2 = $\overline{\text{R}\ell\text{2}}$ Rℓc Rℓ3
Rℓ2
orℓ2 = Rℓ2 Rℓc $\overline{\text{R}\ell\text{3}}$

rℓ3 = $\overline{\text{R}\ell\text{3}}$ Rℓc Rℓ4
Rℓ3
orℓ3 = Rℓ3 Rℓc $\overline{\text{R}\ell\text{4}}$

$r\ell 4 = \overline{R\ell 4}\ R\ell c\ R\ell 5$

Rℓ4

$or\ell 4 = R\ell 4\ R\ell c\ \overline{R\ell 5}$

$r\ell 5 = R\ell 5\ R\ell c\ D91$

Rℓ5

$or\ell 5 = R\ell 5\ R\ell c\ \overline{D91}$

$u1 = \overline{U1}\ Uc$

U1

$ou1 = U1\ Uc + Uc\ell$

$u2 = \overline{U2}\ Uc\ U1$

U2

$ou2 = U2\ Uc\ U1 + Uc\ell$

$u3 = \overline{U3}\ Uc(U1\ U2)$

U3

$ou3 = U3\ Uc(U1\ U2) + Uc\ell$

$u4 = \overline{U4}\ Uc\ (U1\ U2\ U3)$

U4

$ou4 = U4\ Uc\ (U1\ U2\ U3) + Uc\ell$

$u5 = \overline{U5}\ Uc(U1\ U2\ U3\ U4)$

U5

$ou5 = U5\ Uc(U1\ U2\ U3\ U4) + Uc\ell$

$u6 = \overline{U6}\ Uc(U1\ U2\ U3\ U4\ U5)$

U6

$ou6 = U6\ Uc(U1\ U2\ U3\ U4\ U5) + Uc\ell$

$u7 = \overline{U7}\ Uc(U1\ U2\ U3\ U4\ U5\ U6)$

U7

$ou7 = U7\ Uc(U1\ U2\ U3\ U4\ U5\ U6) + Uc\ell$

$u8 = \overline{U8}\ Uc(U1\ U2\ U3\ U4\ U5\ U6\ U7)$

U8

$ou8 = U8\ Uc(U1\ U2\ U3\ U4\ U5\ U6\ U7) + Uc\ell$

```
    e1 = /E1 Ec D18 + Fp7 Ds
E1
   oe1 = E1 Ec /D18 + Fp7 /Ds

    e2 = /E2 Ec E1 + Fp7
E2
   oe2 = E2 Ec /E1

    e3 = /E3 Ec E2 + Fp7
E3
   oe3 = E3 Ec /E2

    e4 = /E4 Ec E3 + Fp7
E4
   oe4 = E4 Ec /E3

    e5 = /E5 Ec(D18 /E6) + Fp7
E5
   oe5 = E5 Ec D18 + Ppc

    e6 = /E6 Ppc
E6
   oe6 = E6 Ec D18 + Fp7

   Fp0 = Fp Bco T5 + Dip

   Fp1 = Fp Bc1

   Fp2 = Fp Bc2

   Fp3 = Fp Bc3

   Fp5 = Fp Bc5 T5

   Fp6 = Fp Bc6 T5 + (D/A)(/A2 /A1) Uc1

   Fp7 = Fp Bc7 T5

   Dec = A3(/A2 A1) U1 T5

   Bec = A3(A2 /A1) U1 T5
```

$$R\ell c = A3\,(A2\;A1)\;U1\;T5$$

$$Ec = A4\,(\overline{A2}\;\overline{A1})\;K\;T5$$

$$Uc\ell = Ur\;T5$$

$$Uc = \overline{Ur}\;T5\;[(A1 + A2) + (\overline{A1}\;\overline{A2})\;K + (\overline{A1}\;\overline{A2})\;Mc + A5\;(\overline{A2}\;\overline{A1})]$$

$$Ppc = Pp\;T5$$

$$\begin{aligned} Ube = {} & (U2\;Be1 + \overline{U2}\;\overline{Be1})(U3\;Be2 + \overline{U3}\;\overline{Be2})(U4\;Be3 + \overline{U4}\;\overline{Be3}) \\ & (U5\;Be4 + \overline{U5}\;\overline{Be4})(U6\;Be5 + \overline{U6}\;\overline{Be5})(U7\;Be6 + \overline{U7}\;\overline{Be6}) \\ & (U8\;Be7 + \overline{U8}\;\overline{Be7}) \end{aligned}$$

$$\begin{aligned} Ude = {} & (U3\;De1 + \overline{U3}\;\overline{De1})(U4\;De2 + \overline{U4}\;\overline{De2})(U5\;De3 + \overline{U5}\;\overline{De3}) \\ & (U6\;De4 + \overline{U6}\;\overline{De4})(U7\;De5 + \overline{U7}\;\overline{De5})(U8\;De6 + \overline{U8}\;\overline{De6}) \end{aligned}$$

$$\begin{aligned} Ur\ell = {} & (U2\;R\ell 1 + \overline{U2}\;\overline{R\ell 1})(U3\;R\ell 2 + \overline{U3}\;\overline{R\ell 2})(U4\;R\ell 3 + \overline{U4}\;\overline{R\ell 3}) \\ & (U5\;R\ell 4 + \overline{U5}\;\overline{R\ell 4})(U6\;R\ell 5 + \overline{U6}\;\overline{R\ell 5}) \end{aligned}$$

$$\begin{aligned} Ur = {} & A3\,(\overline{A2}\;A1)\;U4\;U3\;\overline{U2}\;\overline{U1} + A3\,(A2\;\overline{A1})\;U4\;U3\;U2\;\overline{U1} \\ & + A3\,(A2\;A1)\;U4\;\overline{U3}\;U2\;\overline{U1} + (\overline{A2}\;\overline{A1})\;U6\;\overline{U5}\;\overline{U4}\;U3\;\overline{U2}\;\overline{U1} \\ & + \overline{A3}\,(\overline{A2}\;A1)\;U6\;U5\;U4\;\overline{U3}\;U2\;\overline{U1} + \overline{A3}\,(A2\;A1)\;Ube \\ & + \overline{A3}\,(A2\;\overline{A1})\;Ude + Fp1 + Fp2 + Fp3 \end{aligned}$$

$$\begin{aligned} \overline{US} = {} & \overline{A3}\,[\overline{A4}\,(\overline{A2}\;A1) + \overline{A4}\,(A2\;A1)\;\overline{BeS} + \overline{A4}\,(A2\;\overline{A1})\;\overline{DeS} \\ & + (\overline{A2}\;\overline{A1}) + A4\,(A2\;A1)\;BeS + A4\,(A2\;\overline{A1})\;DeS] \end{aligned}$$

$$Uo = \overline{U8}\;\overline{U7}\;\overline{U6}\;\overline{U5}\;\overline{U4}\;\overline{U3}\;\overline{U2}\;\overline{U1}$$

$$Bop = A4\ \overline{A3}\ (\overline{A2}\ A1)\ \overline{U1}$$

$$Cop = \overline{A4}\ \overline{A3}\ (\overline{A2}\ A1)\ \overline{U1}$$

$$Sd = US\ (A1 + A3)\ K\ U1 + US\ (\overline{A1}\ \overline{A3})\ K$$

$$Cd = US\ (A1 + A3)\ K\ \overline{U1}$$

$$Cm = \overline{US}\ A1\ K\ U1$$

$$Sm = \overline{US}\ A1\ K\ \overline{U1} + \overline{US}\ \overline{A1}\ K + (\overline{A2}\ \overline{A1})\ Mc$$

$$k = \overline{K}\ T5\ A5 + (\overline{A2}\ \overline{A1})\ Ppc + \overline{K}\ (A1 + A2)\ Uo\ Uc$$

K

$$ok = K\ Uc\ell + \overline{A3}\ \overline{A4}\ (\overline{A2}\ A1)\ Ur\ell\ T5 + \overline{A5}\ (\overline{A2}\ \overline{A1})\ U2\ U1\ T5$$

$$a1 = \overline{A1}\ T5\ Fpi + \overline{A4}\ (\overline{A2}\ \overline{A1})\ C1\ T5 + \overline{A1}\ T5\ Fp3 + Fp5 + Fp6$$

A

$$oa1 = A1\ Uc\ell\ \overline{A4} + A4\ (A2\ A1)\ Uc\ell + Fpo$$

$$a2 = \overline{A2}\ T5\ Fp2 + \overline{A2}\ T5\ Fp3 + A4\ (\overline{A2}\ A1)\ Uc\ell + Fp5$$

A2

$$oa2 = A2\ Uc\ell\ \overline{A1} + A3\ A2\ Uc\ell + Fpo$$

$$a5 = \overline{A5}\ Fpo$$

A5

$$oa5 = A5\ Uc\ell$$

$$a3 = A3\ T5\ Fp1 + A3\ T5\ Fp2 + A3\ T5\ Fp3$$

A3

$$oa3 = A3\ Uc\ell$$

$$a4 = \overline{A4}\ Fp6 + Fp7$$

A4

$$oa4 = A4\ Uc\ell\ (\overline{A2}\ \overline{A1}) + (\overline{A2}\ \overline{A1})\ C1\ T5$$

$$sb = \overline{Sb}\ T5\left[\overline{A4}\ (\overline{A2}\ A1)\ U1\ Ur\ell\right] + A4\ (\overline{A2}\ A1)\ U1\ Boc\ T5$$

Sb

$$osb = Sb\ T5\ \overline{A4} + A4\ (\overline{A2}\ A1)\ Uc\ell$$

$$Coc = Cop \left[DS\ U0 + D18\ \overline{DS}\ K + \overline{D18}\ DS\ K + Sb \right]$$

$$dS = \overline{DS}\ Spd\ B1 + Fp6\ Boc$$

DS

$$odS = DS\ Spd\ B1 + Fp6\ Boc$$

$$Ain = D18\ \overline{A3}\ A2 + Db4\ \overline{A4}\ \overline{A5}\ (\overline{A2}\ \overline{A1})$$

$$Bin = Boc\ \overline{DS} + \overline{Boc}\ DS$$

$$Cin = \overline{A3}\ (A2\ A1)\ Uo$$

READER PUNCH

Control

$Ro = R\ell + F\ell + (\text{Reader ON})$

$Rm = Ro + (\text{Reader Motor ON})$ Reader Motor Relay Coil

$Mo = M\ell + (\text{Punch ON})$

$Mo' = Mo + (\text{CLEAR}) + (\text{Leader})$

$Mm = Mo' + (\text{Punch Motor ON})$ Punch Motor Relay Coil

$Nm\ nm = \overline{Rm} + \overline{Mm}$ 200msec

$Np\ np = Nt + (Ns)(S)$ 4.5msec

$Nd\ nd = Np$ 12.5μsec

$Nc\ nc = Nd$ 20msec

$\overline{Rb} = \overline{Np}\ \overline{Nd}\ \overline{Nm}$

$Nt = Cp(\text{Clock Ext}) + Nc(\text{Clock On})$

$(S) = (\text{Start}) + (\text{Leader})$